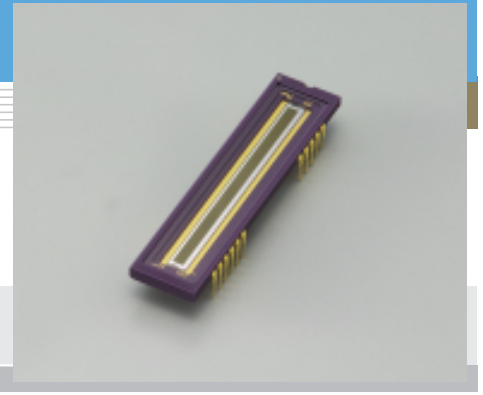


# NMOS linear image sensor S3901-1024Q, S3904-2048Q

Large active area with 51.2 mm detection length



NMOS linear image sensors are self-scanning photodiode arrays designed specifically as detectors for multichannel spectroscopy. The scanning circuit is made up of N-channel MOS transistors, operates at low power consumption and is easy to handle. Each photodiode has a large active area, high UV sensitivity yet very low noise, delivering a high S/N even at low light levels. The current output type NMOS linear image sensors also feature excellent output linearity and wide dynamic range. S3901-1024Q uses photodiodes with a height of 2.5 mm, arrayed at a spacing of 50  $\mu\text{m}$ . S3904-2048Q has photodiodes with a height of 2.5 mm, arrayed at a spacing of 25  $\mu\text{m}$ . The photodiode arrays are available in 2 different pixel quantities, 1024 (S3901-1024Q) and 2048 (S3904-2048Q). Quartz glass is the standard window material. Dedicated driver circuit C7615 (sold separately) is also provided.

### Features

- Large active area, long detection length  
Pixel pitch: 50  $\mu\text{m}$  (S3901-1024Q)  
25  $\mu\text{m}$  (S3904-2048Q)  
Pixel height: 2.5 mm  
Active area length: 51.2 mm
- High UV sensitivity with good stability
- Low dark current and large saturation charge allow long integration time and a wide dynamic range at room temperature
- Excellent output linearity and sensitivity spatial uniformity
- Low power consumption: 1 mW Max.
- Start pulse and clock pulses are CMOS logic compatible

### Applications

- Multichannel spectrophotometry
- Image readout system

Figure 1 Equivalent circuit

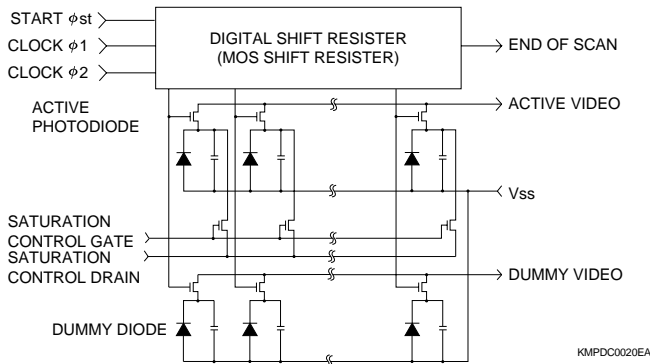
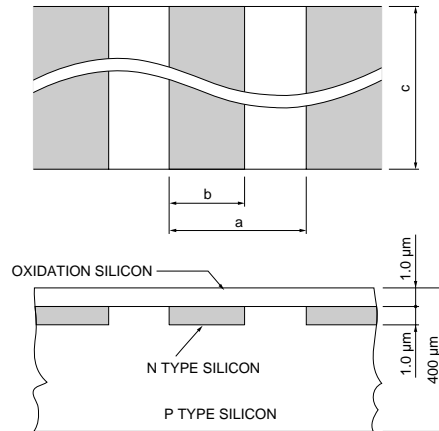


Figure 2 Active area structure



S3901-1024Q: a=50  $\mu\text{m}$ , b=45  $\mu\text{m}$ , c=2.5 mm  
S3904-2048Q: a=25  $\mu\text{m}$ , b=20  $\mu\text{m}$ , c=2.5 mm

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### ■ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Input pulse ( $\phi_1$ , $\phi_2$ , $\phi_{st}$ ) voltage	$V_\phi$	15	V
Power consumption *1	P	1	mW
Operating temperature *2	$T_{opr}$	-40 to +65	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-40 to +85	$^\circ\text{C}$

\*1:  $V_\phi=5.0\text{ V}$

\*2: No condensation

■ Shape specifications

Parameter	S3901-1024Q	S3904-2048Q	Unit
Number of pixels	1024	2048	-
Package length	65.0		mm
Number of pin	22		-
Window material *3	Quartz		-
Weight	8.5		g

\*3: Fiber optic plate is available.

■ Specifications (Ta=25 °C)

Parameter	Symbol	S3901-1024Q			S3904-2048Q			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Pixel pitch	-	-	50	-	-	25	-	μm
Pixel height	-	-	2.5	-	-	2.5	-	mm
Spectral response range (10 % of peak)	$\lambda$	200 to 1000			200 to 1000			nm
Peak sensitivity wavelength	$\lambda_p$	-	600	-	-	600	-	nm
Photodiode dark current *4	$I_D$	-	0.2	0.6	-	0.1	0.3	pA
Photodiode capacitance *4	$C_{ph}$	-	20	-	-	10	-	pF
Saturation exposure *4, *5	$E_{sat}$	-	180	-	-	180	-	$mJ \cdot s$
Saturation output charge *4	$Q_{sat}$	-	50	-	-	25	-	pC
Photo response non-uniformity *6	PRNU	-	-	±3	-	-	±3	%

\*4: Vb=2.0 V, Vφ=5.0 V

\*5: 2856 K, tungsten lamp

\*6: 50 % of saturation, excluding the start pixel and last pixel

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Condition	S3901-1024Q			S3904-2048Q			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock pulse (φ1, φ2) voltage	High	Vφ1, Vφ2 (H)	4.5	5	10	4.5	5	10	V
	Low	Vφ1, Vφ2 (L)	0	-	0.4	0	-	0.4	V
Start pulse (φst) voltage	High	Vφs (H)	4.5	Vφ1	10	4.5	Vφ1	10	V
	Low	Vφs (L)	0	-	0.4	0	-	0.4	V
Video bias voltage *7	Vb		1.5	Vφ - 3.0	Vφ - 2.5	1.5	Vφ - 3.0	Vφ - 2.5	V
Saturation control gate voltage	Vscg		-	0	-	-	0	-	V
Saturation control drain voltage	Vscd		-	Vb	-	-	Vb	-	V
Clock pulse (φ1, φ2) rise/fall time *8	trφ1, trφ2 tfφ1, tfφ2		-	20	-	-	20	-	ns
Clock pulse (φ1, φ2) pulse width	tpwφ1, tpwφ2		200	-	-	200	-	-	ns
Start pulse (φst) rise/fall time	trφs, tfφs		-	20	-	-	20	-	ns
Start pulse (φst) pulse width	tpwφs		200	-	-	200	-	-	ns
Start pulse (φst) and clock pulse (φ2) overlap	tφov		200	-	-	200	-	-	ns
Clock pulse space *8	X1, X2		trf - 20	-	-	trf - 20	-	-	ns
Data rate *9	f		0.1	-	2000	0.1	-	2000	kHz
Video delay time	tvd	50 % of saturation *9, *10	-	200	-	-	250	-	ns
Clock pulse (φ1, φ2) line capacitance	Cφ	5 V bias	-	134	-	-	200	-	pF
Saturation control gate (Vscg) line capacitance	Cscg	5 V bias	-	63	-	-	87	-	pF
Video line capacitance	Cv	2 V bias	-	45	-	-	60	-	pF

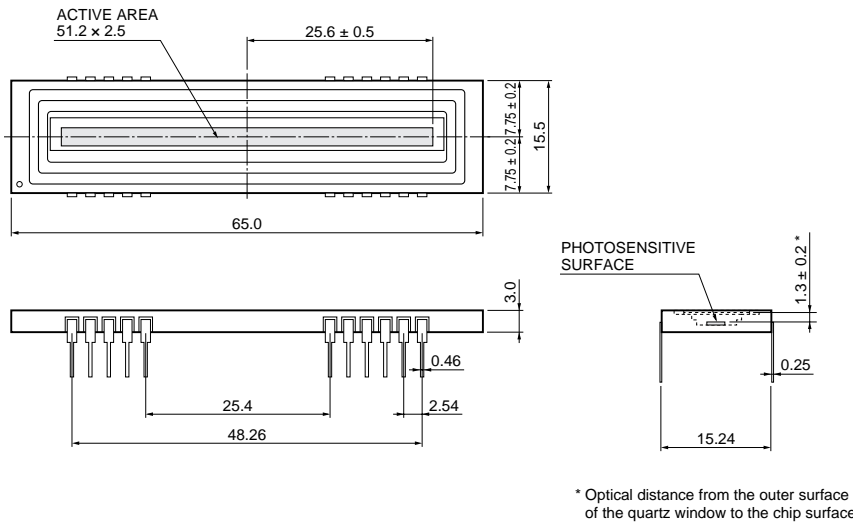
\*7: Vφ is input pulse voltage (refer to figure 8) .

\*8: trf is the clock pulse rise or fall time. A clock pulse space of "rise time/fall time - 20" ns (nanoseconds) or more should be input if the clock pulse rise or fall time is longer than 20 ns (refer to figure 7) .

\*9: Vb=2.0 V, Vφ=5.0 V

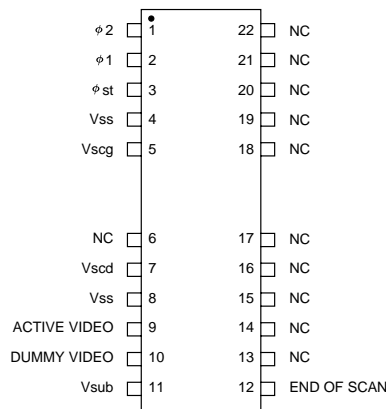
\*10: Measured with C7883 driver circuit.

Figure 3 Dimensional outline (unit: mm)



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Figure 4 Pin connection

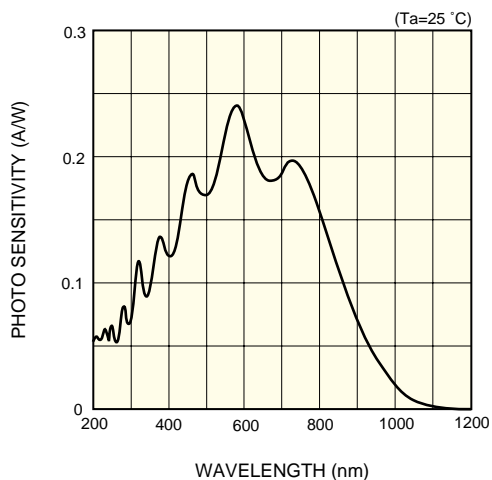


Vss, Vsub and NC should be grounded.

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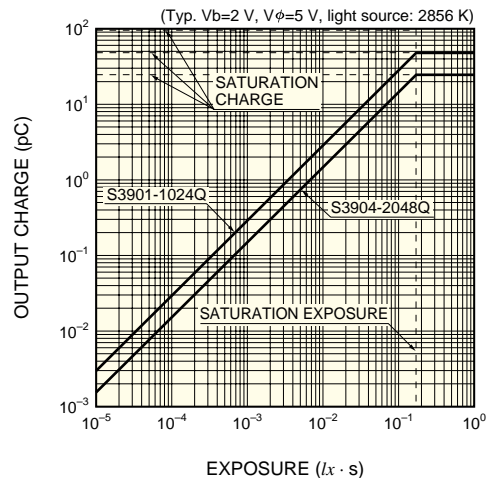
Terminal	Input or output	Description
φ1, φ2	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. The video data rate is equal to the clock pulse frequency since the video output signal is obtained synchronously with the rise of φ2 pulse.
φst	Input (CMOS logic compatible)	Pulse for starting the MOS shift register operation. The time interval between start pulses is equal to the signal accumulation time.
Vss	-	Connected to the anode of each photodiode. This should be grounded.
Vscg	Input	Used for restricting blooming. This should be grounded.
Vscd	Input	Used for restricting blooming. This should be biased at a voltage equal to the video bias voltage.
Active video	Output	Video output signal. Connects to photodiode cathodes when the address is on. A positive voltage should be applied to the video line in order to use photodiodes with a reverse voltage. When the amplitude of φ1 and φ2 is 5 V, a video bias voltage of 2 V is recommended.
Dummy video	Output	This has the same structure as the active video, but is not connected to photodiodes, so only spike noise is output. This should be biased at a voltage equal to the active video or left as an open-circuit when not needed.
Vsub	-	Connected to the silicon substrate. This should be grounded.
End of scan	Output (CMOS logic compatible)	This should be pulled up at 5 V by using a 10 kΩ resistor. This is a negative going pulse that appears synchronously with the φ2 timing right after the last photodiode is addressed.
NC	-	Should be grounded.

Figure 5 Spectral response (typical example)



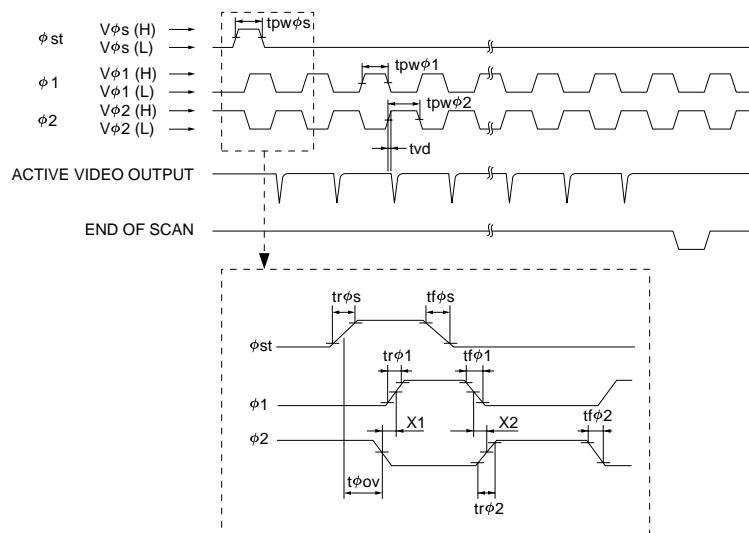
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Figure 6 Output charge vs. exposure



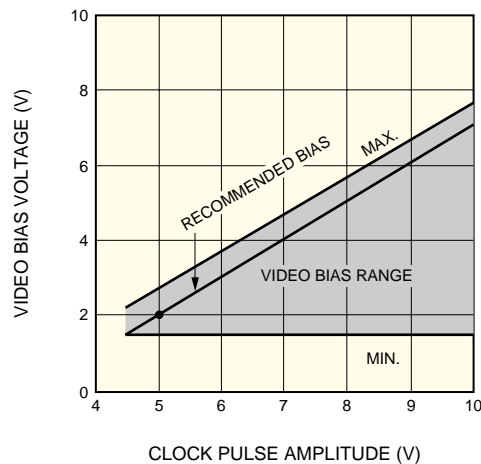
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Figure 7 Timing chart



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Figure 8 Video bias voltage margin



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