

Features

- TSOP I Package Configurable as 1M x 16 or 2M x 8 SRAM
- Very High Speed: 45 ns
- Temperature Ranges
 - Industrial: -40°C to +85°C
 - Automotive-A: -40°C to +85°C
- Wide Voltage Range: 2.20V to 3.60V
- Ultra Low Standby Power
 - Typical standby current: 1.5 μ A
 - Maximum standby current: 12 μ A
- Ultra Low Active Power
 - Typical active current: 2.2 mA at f = 1 MHz
- Easy Memory Expansion with $\overline{CE}_1$, CE_2 , and $\overline{OE}$ Features
- Automatic Power Down when Deselected
- CMOS for Optimum Speed and Power
- Offered in Pb-free 48-Ball VFBGA and 48-Pin TSOP I Packages

Functional Description

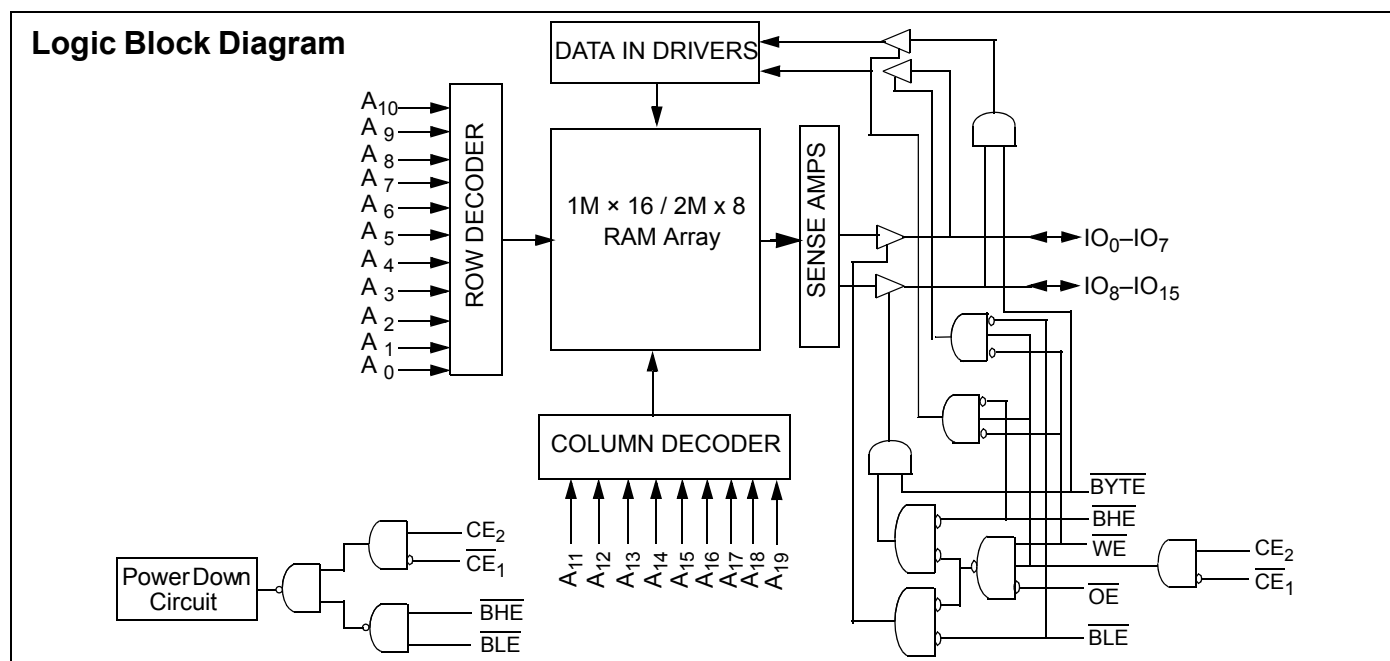
The CY62167EV30 is a high performance CMOS static RAM organized as 1M words by 16 bits or 2M words by 8 bits. This device features an advanced circuit design that provides an ultra

low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption by 99 percent when addresses are not toggling. Place the device into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both BHE and BLE are HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when: the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW, CE_2 HIGH and WE LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₉). If Byte High Enable (BHE) is LOW, then data from the I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₉).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the "Truth Table" on page 9 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).



Pin Configuration

Figure 1. 48-Ball VFBGA (6 x 7 x 1mm) / (6 x 8 x 1mm) Top View [1, 2, 3]

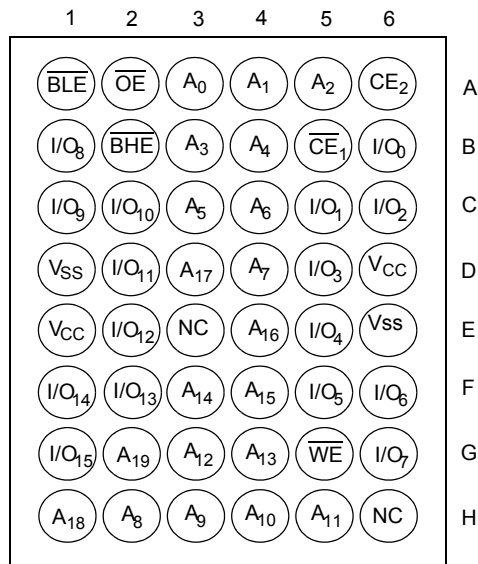
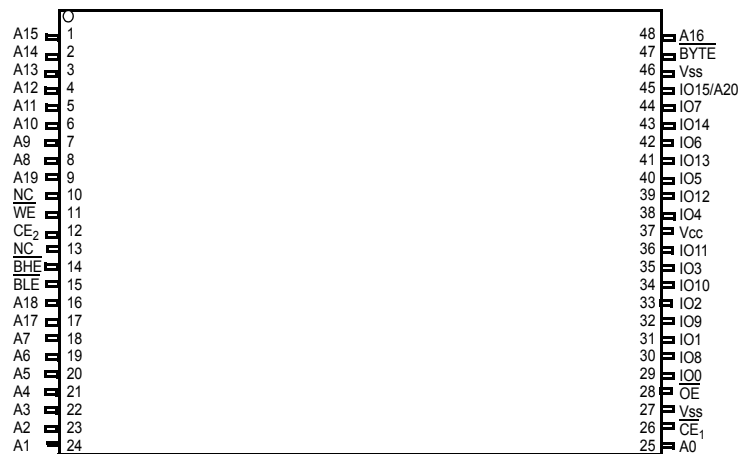


Figure 2. 48-Pin TSOP I Top View [3, 4]



Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
						f = 1 MHz		f = f _{max}			
		Min	Typ ^[5]	Max		Typ ^[5]	Max	Typ ^[5]	Max	Typ ^[5]	Max
CY62167EV30LL	Industrial/Auto-A	2.2	3.0	3.6	45	2.2	4.0	25	30	1.5	12

Notes

- The information related to 6 x 7 x 1 mm VFBGA package is preliminary.
- Ball H6 for the VFBGA package can be used to upgrade to a 32M density.
- NC pins are not connected on the die.
- The BYTE pin in the 48-TSOP package has to be tied to V_{CC} to use the device as a 1M X 16 SRAM. The 48-TSOP package can also be used as a 2M X 8 SRAM by tying the BYTE signal to V_{SS}. In the 2M x 8 configuration, Pin 45 is A20, while BHE, BLE and IO₈ to IO₁₄ pins are not used.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ), T_A = 25°C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to + 150°C

Ambient Temperature with
Power Applied -55°C to + 125°C

Supply Voltage to Ground
Potential -0.3V to 3.9V $V_{CC(max)} + 0.3V$

DC Voltage Applied to Outputs
in High Z State^[6, 7] -0.3V to 3.9V $V_{CC(max)} + 0.3V$

DC Input Voltage^[6, 7] -0.3V to 3.9V ($V_{CC(max)} + 0.3V$)

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(MIL-STD-883, Method 3015)

Latch up Current >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} ^[8]
CY62167EV30LL	Industrial/ Auto-A	-40°C to +85°C	2.2V to 3.6V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Industrial/Auto-A)			Unit
			Min	Typ ^[5]	Max	
V_{OH}	Output HIGH Voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OH} = -0.1 \text{ mA}$	2.0		V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OH} = -1.0 \text{ mA}$	2.4		V
V_{OL}	Output LOW Voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OL} = 0.1 \text{ mA}$		0.4	V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OL} = 2.1 \text{ mA}$		0.4	V
V_{IH}	Input HIGH Voltage	$2.2 \leq V_{CC} \leq 2.7$		1.8	$V_{CC} + 0.3V$	V
		$2.7 \leq V_{CC} \leq 3.6$		2.2	$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage	$2.2 \leq V_{CC} \leq 2.7$		-0.3	0.6	V
		$2.7 \leq V_{CC} \leq 3.6$ For VFBGA package	-0.3		0.8	V
		$2.7 \leq V_{CC} \leq 3.6$ For TSOP I package	-0.3		0.7 ^[9]	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$ $V_{CC} = V_{CC(max)}$		25	30	mA
		$f = 1 \text{ MHz}$ $I_{OUT} = 0 \text{ mA}$ CMOS levels		2.2	4.0	mA
I_{SB1}	Automatic CE Power Down Current—CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$, $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE, WE, BHE and BLE), $V_{CC} = 3.60V$		1.5	12	μA
I_{SB2} ^[10]	Automatic CE Power Down Current—CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = 3.60V$		1.5	12	μA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$,	10	pF
C_{OUT}	Output Capacitance	$V_{CC} = V_{CC(typ)}$	10	pF

Notes

- $V_{IL(min)} = -2.0V$ for pulse durations less than 20 ns.
- $V_{IH(max)} = V_{CC} + 0.75V$ for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V_{CC} (min) and 200 μs wait time after V_{CC} stabilization.
- Under DC conditions the device meets a V_{IL} of 0.8V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7V. This is applicable to TSOP I package only.
- Only chip enables ($\overline{CE}_1$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ must be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating

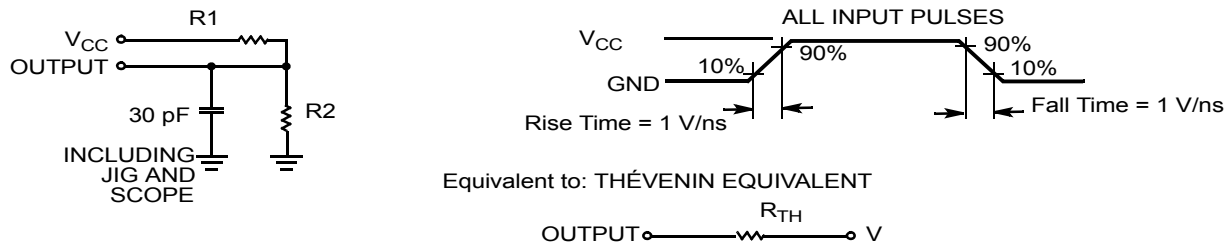
Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	VFBGA (6 x 7 x 1mm)	VFBGA (6 x 8 x 1mm)	TSOP I	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	27.74	55	60	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		9.84	16	4.3	°C/W

Shaded areas contain preliminary information.

Figure 3. AC Test Loads and Waveforms



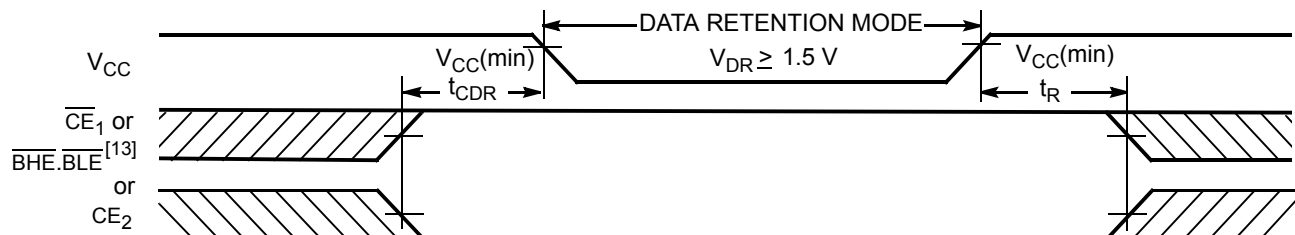
Parameters	2.2V to 2.7V	2.7V to 3.6V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[5]	Max	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
$I_{CCDR}^{[10]}$	Data Retention Current	$V_{CC} = 1.5V$ to $3.0V$, $CE_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Industrial/ Auto-A	-45ZXI (TSOP I)	8	μA
		$V_{CC} = 1.5V$, $CE_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Industrial	-45BAXI/ -45BVXI/ -45BVI (VFBGA)	10	μA
$t_{CDR}^{[11]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[12]}$	Operation Recovery Time		t_{RC}			ns

Figure 4. Data Retention Waveform



Notes

11. Tested initially and after any design or process changes that may affect these parameters.

12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC}(\min) \geq 100 \mu s$ or stable at $V_{CC}(\min) \geq 100 \mu s$.

13. BHE.BLE is the AND of both BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling both BHE and BLE.

Switching Characteristics

Over the Operating Range^[14, 15]

Parameter	Description	45 ns (Industrial/Auto-A)		Unit
		Min	Max	
READ CYCLE				
t _{RC}	Read Cycle Time	45		ns
t _{AA}	Address to Data Valid		45	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Data Valid		45	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		22	ns
t _{LZOE}	$\overline{OE}$ LOW to LOW Z ^[16]	5		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[16, 17]		18	ns
t _{LZCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Low Z ^[16]	10		ns
t _{HZCE}	$\overline{CE}_1$ HIGH and CE ₂ LOW to High Z ^[16, 17]		18	ns
t _{PU}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Power Up	0		ns
t _{PD}	$\overline{CE}_1$ HIGH and CE ₂ LOW to Power Down		45	ns
t _{DBE}	BLE / BHE LOW to Data Valid		45	ns
t _{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z ^[16]	10		ns
t _{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HIGH Z ^[16, 17]		18	ns
WRITE CYCLE ^[18]				
t _{WC}	Write Cycle Time	45		ns
t _{SCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Write End	35		ns
t _{AW}	Address Setup to Write End	35		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Setup to Write Start	0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	35		ns
t _{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	35		ns
t _{SD}	Data Setup to Write End	25		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	$\overline{WE}$ LOW to High-Z ^[16, 17]		18	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low-Z ^[16]	10		ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of $V_{CC}(typ)/2$, input pulse levels of 0 to $V_{CC}(typ)$, and output loading of the specified I_{OL}/I_{OH} as shown in "AC Test Loads and Waveforms" on page 4.
15. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note AN13842 for further clarification.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

Switching Waveforms

Figure 5 shows address transition controlled read cycle waveforms.^[19, 20]

Figure 5. Read Cycle No. 1

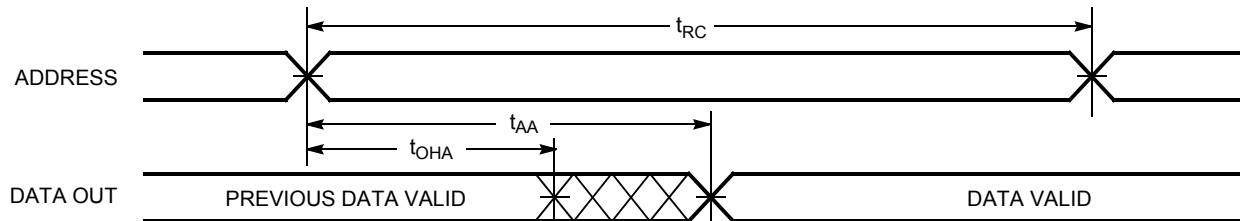
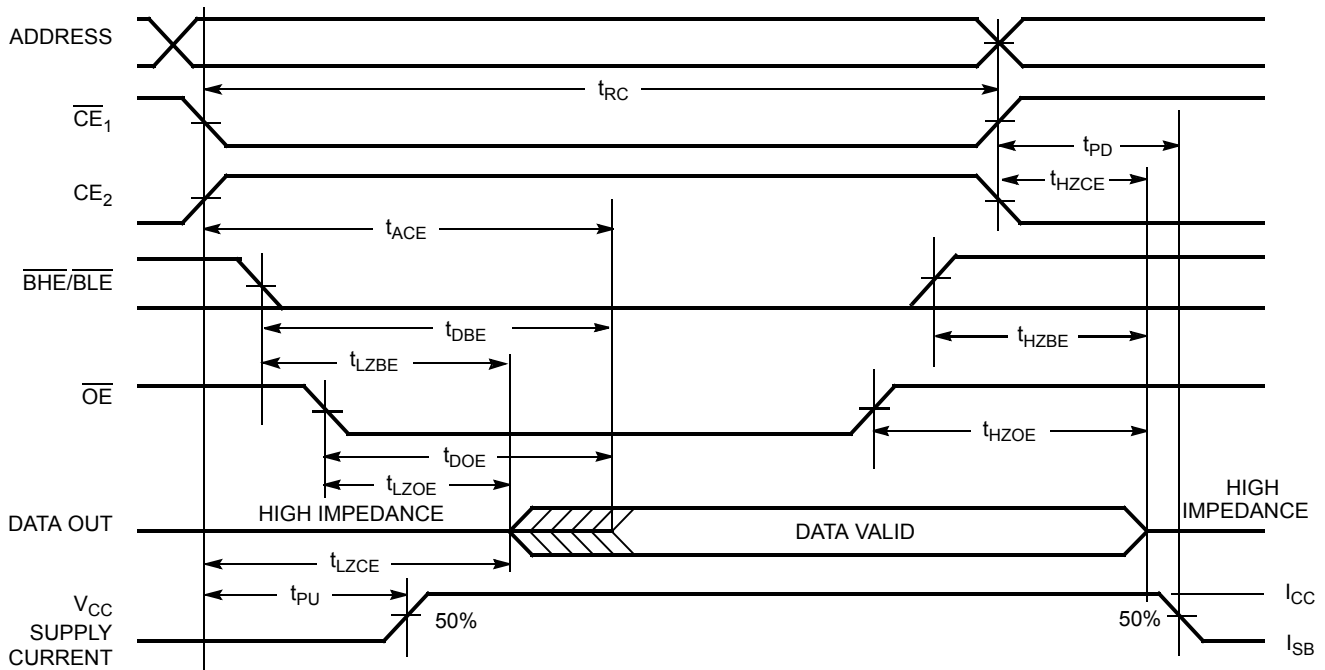


Figure 6 shows $\overline{OE}$ controlled read cycle waveforms.^[20, 21]

Figure 6. Read Cycle No. 2



Notes

19. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL} , and $CE_2 = V_{IH}$.

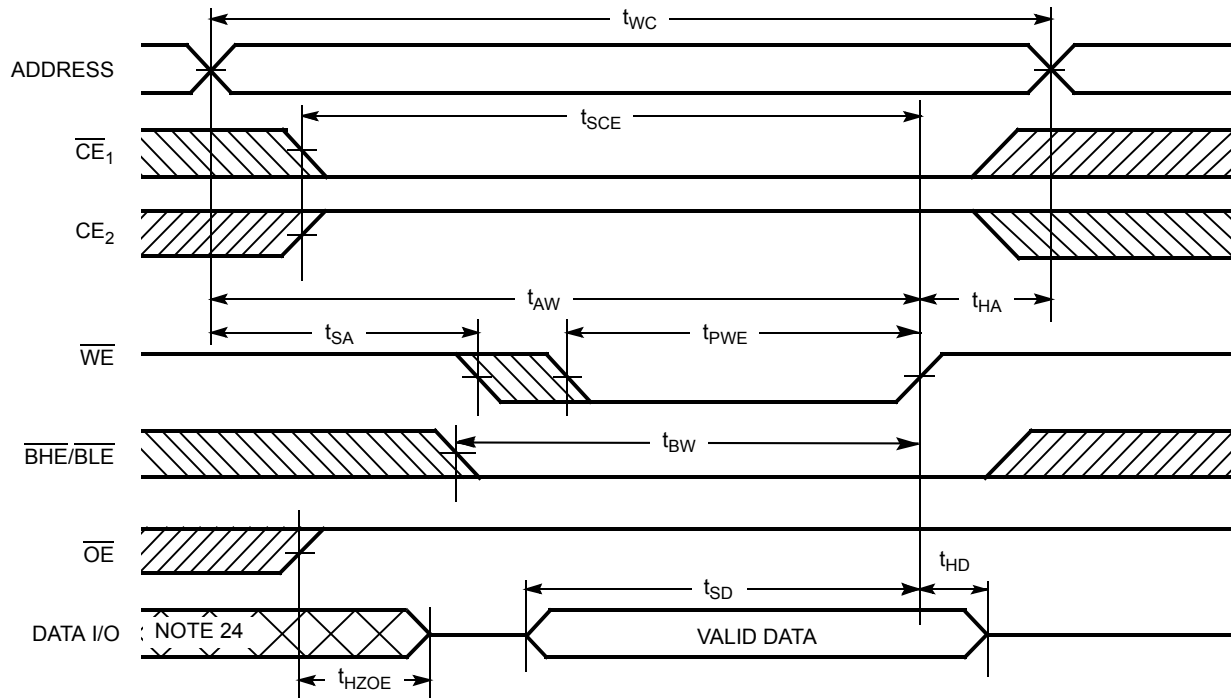
20. $\overline{WE}$ is HIGH for read cycle.

21. Address valid before or similar to $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 7 shows $\overline{WE}$ controlled write cycle waveforms.^[18, 22, 23]

Figure 7. Write Cycle No. 1



Notes

22. Data IO is high impedance if $\overline{OE} = V_{IH}$.

23. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

24. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8 shows $\overline{CE}_1$ or CE_2 controlled write cycle waveforms.^[18, 22, 23]

Figure 8. Write Cycle No. 2

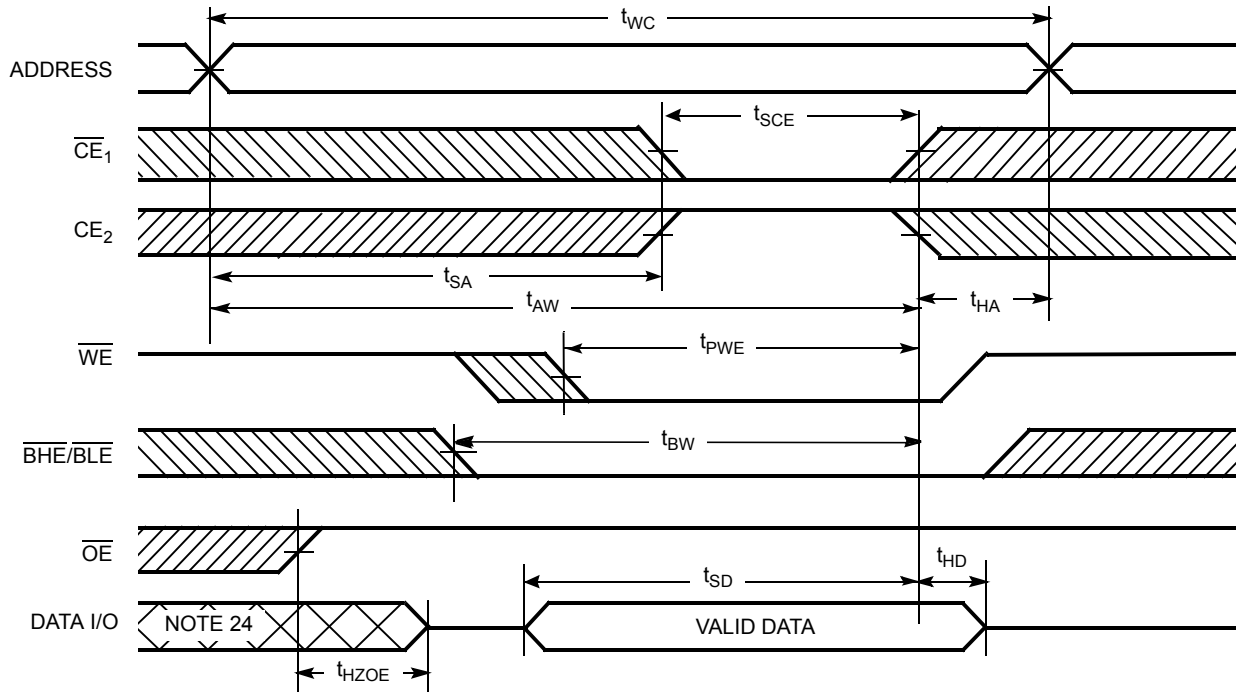
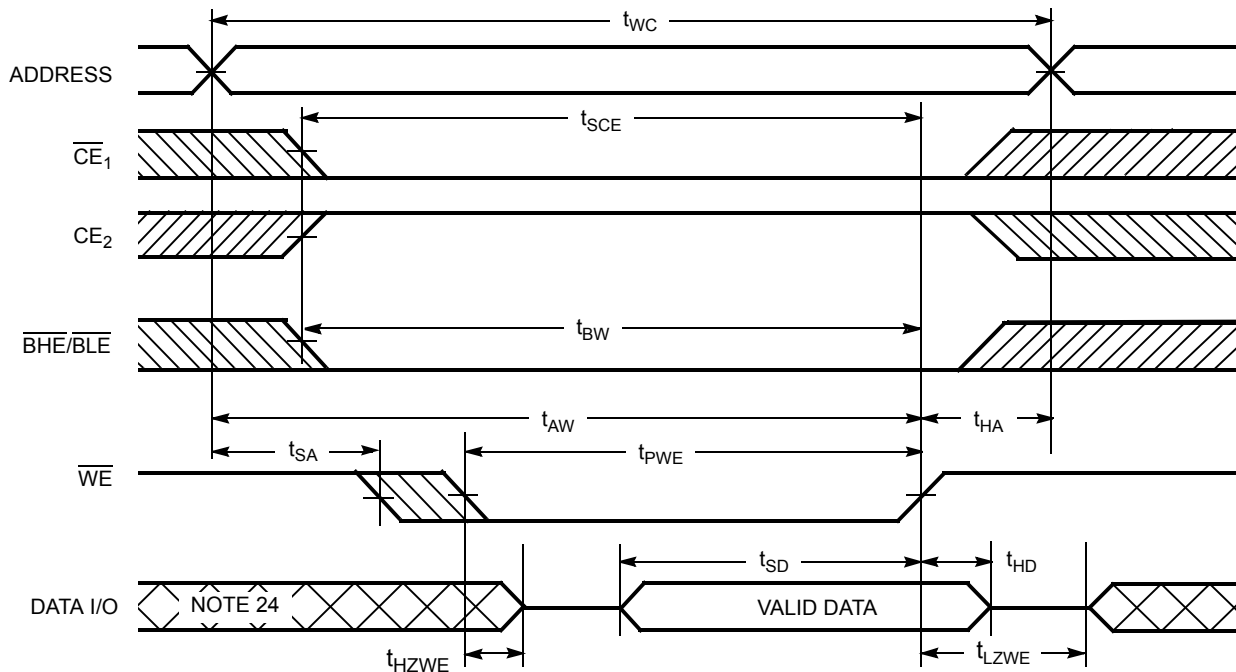


Figure 9 shows $\overline{WE}$ controlled, $\overline{OE}$ LOW write cycle waveforms.^[23]

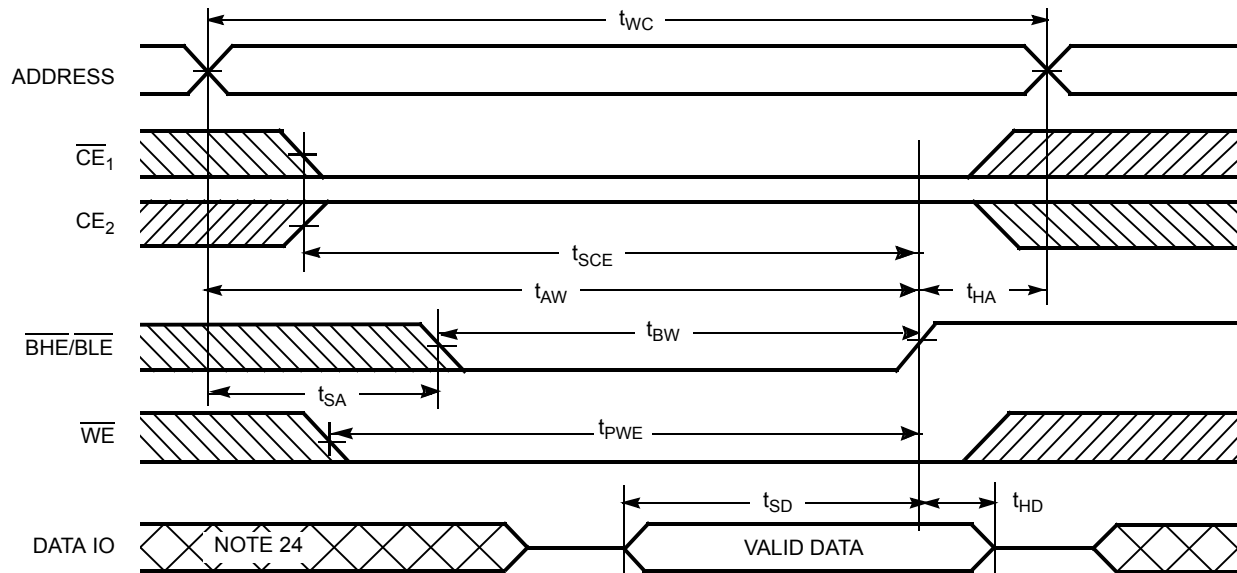
Figure 9. Write Cycle No. 3



Switching Waveforms (continued)

Figure 10 shows $\overline{\text{BHE}}/\overline{\text{BLE}}$ controlled, $\overline{\text{OE}}$ LOW write cycle waveforms.^[23]

Figure 10. Write Cycle No. 4



Truth Table

$\overline{\text{CE}}_1$	CE_2	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect / Power Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect / Power Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect / Power Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0 – I/O_7); Data Out (I/O_8 – I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0 – I/O_7); Data In (I/O_8 – I/O_{15})	Write	Active (I_{CC})

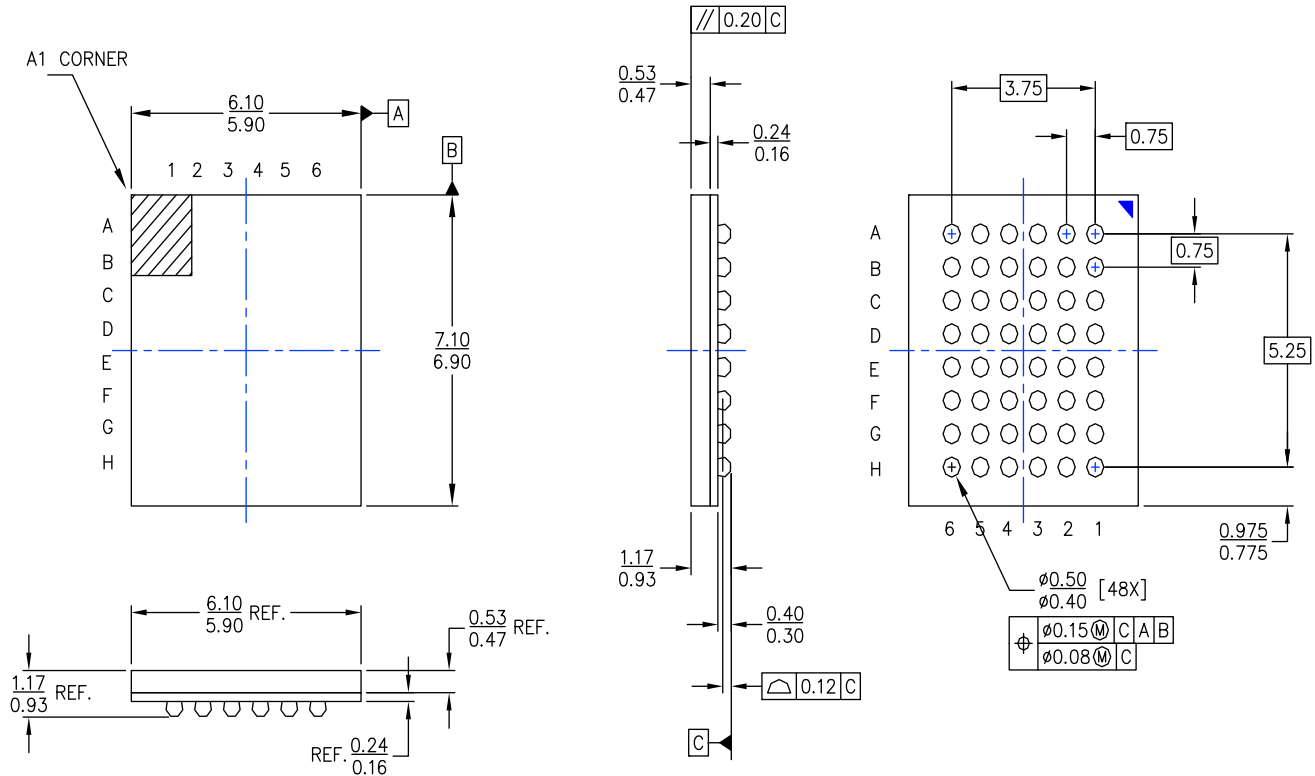
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167EV30LL-45BAXI	001-13297	48-ball VFBGA (6 x 7 x 1 mm) (Pb-free)	Industrial
	CY62167EV30LL-45BVI	51-85150	48-ball VFBGA (6 x 8 x 1 mm)	
	CY62167EV30LL-45BVXI	51-85150	48-ball VFBGA (6 x 8 x 1 mm) (Pb-free)	
	CY62167EV30LL-45ZXI	51-85183	48-pin TSOP I (Pb-free)	
	CY62167EV30LL-45BVXA	51-85150	48-ball VFBGA (6 x 8 x 1 mm) (Pb-free)	Automotive-A
	CY62167EV30LL-45ZXA	51-85183	48-pin TSOP I (Pb-free)	

Shaded areas contain preliminary information. Contact your local Cypress sales representative for availability of these parts.

Package Diagrams

Figure 11. 48-Ball VFBGA (6 x 7 x 1 mm), 001-13297

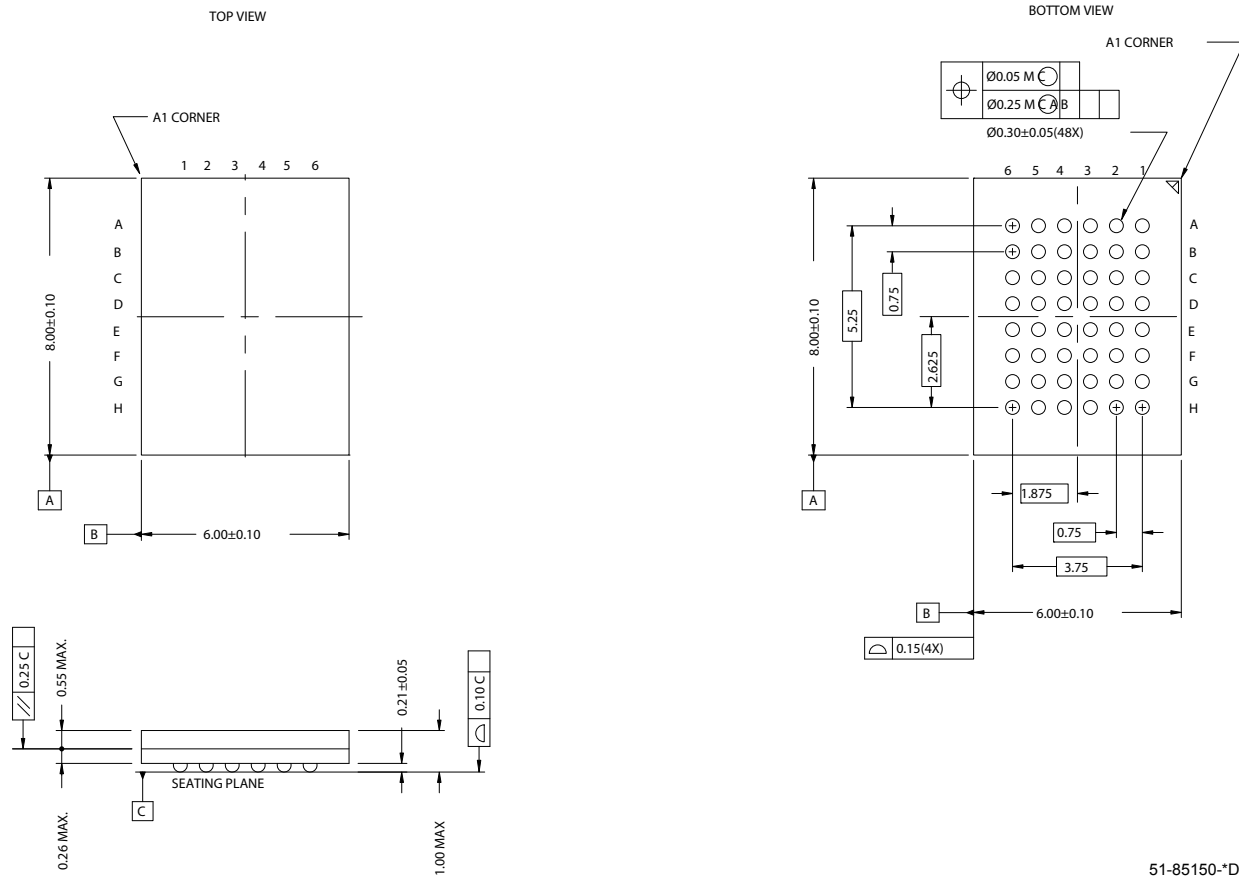


NOTES:
 1. ALL DIMENSION ARE IN MM [MAX/MIN]
 2. JEDEC REFERENCE : MO-216
 3. PACKAGE WEIGHT : 0.03g

001-13297-A

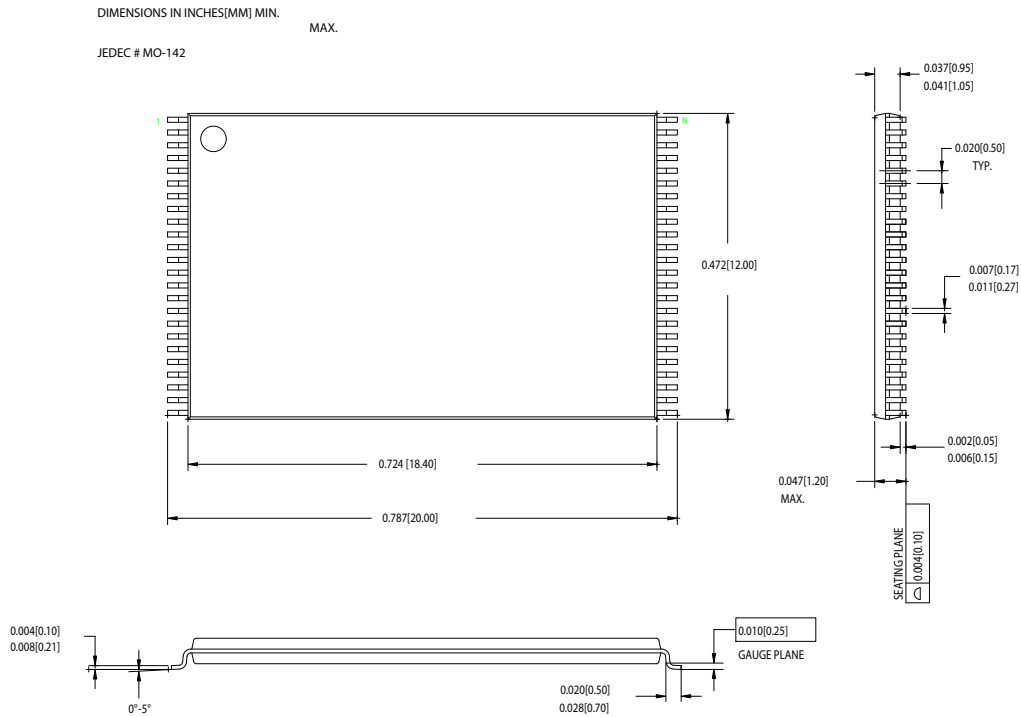
Package Diagrams (continued)

Figure 12. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150



Package Diagrams (continued)

Figure 13. 48-Pin TSOP I (12 mm x 18.4 mm x 1.0 mm), 51-85183



51-85183-*A

Document History Page

Document Title: CY62167EV30 MoBL® 16-Mbit (1M x 16 / 2M x 8) Static RAM Document Number: 38-05446				
REV.	ECN NO.	Orig. of Change	Submission Date	Description of Change
**	202600	AJU	01/23/2004	New Data Sheet
*A	463674	NXR	See ECN	Converted from Advance Information to Preliminary Removed 'L' bin and 35 ns speed bin from product offering Modified Data sheet to include x8 configurability. Changed ball E3 in FBGA pinout from DNU to NC Changed the $I_{SB2(Typ)}$ value from 1.3 μA to 1.5 μA Changed the $I_{CC(Max)}$ value from 40 mA to 25 mA Changed Vcc stabilization time in footnote #9 from 100 μs to 200 μs Changed the AC Test Load Capacitance value from 50 pF to 30 pF Corrected typo in Data Retention Characteristics (t_R) from 100 μs to t_{RC} ns Changed t_{OHA} , t_{LZCE} , t_{LZBE} , and t_{LZWE} from 6 ns to 10 ns Changed t_{LZOE} from 3 ns to 5 ns. Changed t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} from 15 ns to 18 ns Changed t_{SCE} , t_{AW} , and t_{BW} from 40 ns to 35 ns Changed t_{PE} from 30 ns to 35 ns Changed t_{SD} from 20 ns to 25 ns Updated 48 ball FBGA Package Information. Updated the Ordering Information table
*B	469169	NSI	See ECN	Minor Change: Moved to external web
*C	1130323	VKN	See ECN	Converted from preliminary to final Changed I_{CC} max spec from 2.8 mA to 4.0 mA for $f=1MHz$ Changed I_{CC} typ spec from 22 mA to 25 mA for $f=f_{max}$ Changed I_{CC} max spec from 25 mA to 30 mA for $f=f_{max}$ Added V_{IL} spec for TSOP I package and footnote# 9 Added footnote# 10 related to I_{SB2} and I_{CCDR} Changed I_{SB1} and I_{SB2} spec from 8.5 μA to 12 μA Changed I_{CCDR} spec from 8 μA to 10 μA Added footnote# 15 related to AC timing parameters
*D	1323984	VKN/AESA	See ECN	Modified I_{CCDR} spec for TSOP I package Added 48-Ball VFBGA (6 x 7 x 1mm) package Added footnote# 1 related to VFBGA (6 x 7 x 1mm) package Updated Ordering Information table
*E	2678799	VKN/PYRS	03/25/2009	Added Automotive-A information
*F	2720234	VKN/AESA	06/17/2009	Included -45BVXA part in the Ordering information table

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com

© Cypress Semiconductor Corporation, 2004-2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.