

TPD7S019 7-Channel Integrated ESD Solution for VGA Port with Integrated Level-Shifter and Matching Impedance

1 Features

- 7-Channel ESD Protection Includes ESD Protection, Level-Shifting, Buffering and Sync Impedance Matching
- Exceeds IEC61000-4-2 (Level 4) ESD Protection to Requirements on the External Pins
 - ±8-kV IEC 61000-4-2 Contact Discharge
- Very Low Loading Capacitance from ESD Protection Diodes on VIDEO Lines (2.5 pF)
- 5-V Drivers for HSYNC and VSYNC Lines
- Integrated Impedance Matching Resistors on Sync Lines
- Bidirectional Level-Shifting N-Channel FETs Provided for DDC_CLK and DDC_DATA Channels
- Flow-Through Single-In-Line Pin Mapping Ensures no Additional Board Layout Burden While Placing the ESD Protection Chip Near the Connector

2 Applications

- End Equipment:
 - Desktop and Notebook PCs
 - Set Top Boxes
 - TVs
- Interfaces:
 - VGA
 - DVI-I

3 Description

The TPD7S019 device is an integrated electrostatic discharge (ESD) circuit protection solution for VGA and DVI-I connectors. It integrates transient voltage suppression (TVS) protection diodes for VIDEO, DDC and SYNC signals and meets the IEC61000-4-2 standard for ±8-kV contact ESD protection. The TVS diodes only add low capacitances to help signals run at high-speed. It also provides level-shifting for the DDC signals saving external level-shifters. Two noninverting drivers on HSYNC and VSYNC convert TTL input levels to CMOS output levels and each buffer has a series termination resistor connected to the SYNC_OUT pin, eliminating the external termination resistors. Three supply lines control the power rails of the VIDEO, DDC and SYNC channels to facilitate interfacing with low voltage video controller ICs in mixed supply-voltage environments. The TPD7S019 comes with two package options. The 16-pin RSV is compact and space-saving. The 16-pin DBQ package and pinout are optimized for easy board layout.

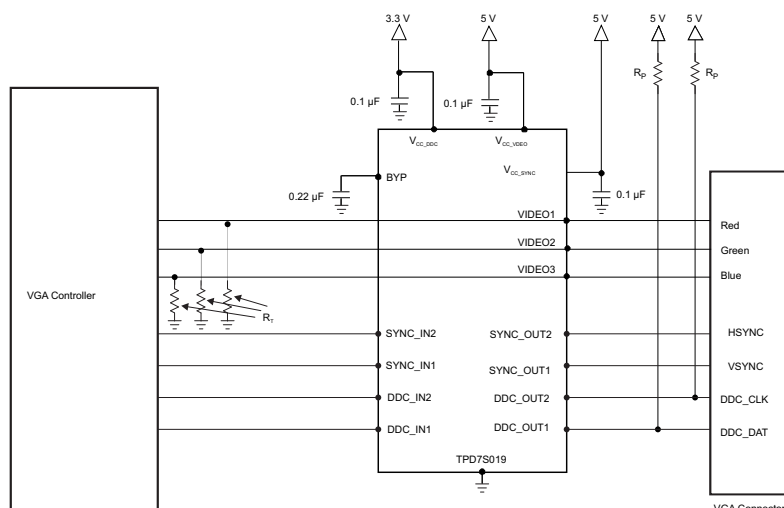
This ESD protection product is a good solution to protect the VGA and DVI-I ports for desktop and laptop PCs, set top boxes, TVs and monitors.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD7S019	SSOP (16)	4.90 mm × 3.90 mm
	UQFN (16)	2.60 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



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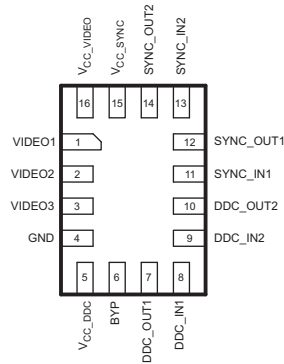
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

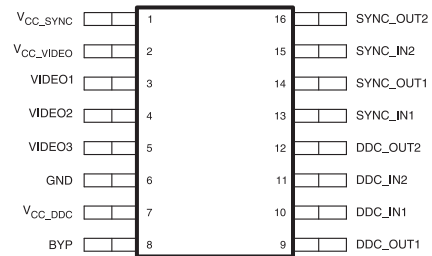
Changes from Revision D (April 2016) to Revision E	Page
• Updated Figure 6	10
Changes from Revision C (November 2015) to Revision D	Page
• Updated the Functional Block Diagram	8
Changes from Revision B (December 2012) to Revision C	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
Changes from Original (August 2010) to Revision A	Page
• Removed PREVIEW status from the RSV package.....	3
Changes from Revision A (March 2012) to Revision B	Page
• Removed non released part descriptions from the datasheet.....	1

5 Pin Configuration and Functions

**RSV Package
16-Pin UQFN
Top View**



**DBQ Package
16-Pin SSOP
Top View**



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBQ	RSV		
BYP	8	6	Power	Bypass pin. Using a 0.2-μF bypass capacitor increases the ESD robustness of the system
DDC_IN1	10	8	I	DDC signal input. Connects to the VGA controller side of one of the sync lines
DDC_IN2	11	9		
DDC_OUT1	9	7	O	DDC signal output. Connects to the video connector side of one of the sync lines
DDC_OUT2	12	10		
GND	6	4	—	Ground
SYNC_IN1	13	11	I	Sync signal buffer input. Connects to the VGA controller side of one of the sync lines
SYNC_IN2	15	13		
SYNC_OUT1	14	12	O	Sync signal buffer output. Connects to the video connector side of one of the sync lines
SYNC_OUT2	16	14		
V _{CC_DDC}	7	5	Power	Isolated supply input for the DDC_1 and DDC_2 level-shifting N-FET gates
V _{CC_SYNC}	1	15	Power	Isolated supply input for the SYNC_1 and SYNC_2 level-shifters and their associated ESD protection circuits
V _{CC_VIDEO}	2	16	Power	Supply pin specifically for the VIDEO_1, VIDEO_2 and VIDEO_3 ESD protection circuits
VIDEO1	3	1	ESD	High-speed ESD clamp input
VIDEO2	4	2		
VIDEO3	5	3		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

				MIN	MAX	UNIT
Supply voltage	V _{CC_VIDEO}			−0.5	6	V
	V _{CC_DDC}			−0.5	6	
	V _{CC_SYNC}			−0.5	6	
IO voltage	V _{IO(VIDEO)}	VIDEOx pins		−0.5	V _{CC_VIDEO}	V
Input voltage	V _{I(SYNC)}	SYNC pins		−0.5	V _{CC_SYNC}	V
	V _{I(DDC)}	DDC_INx pins		−0.5	6	V
Output voltage	V _{O(DDC)}	DDC_INx pins		−0.5	6	V
Input clamp current	I _{IK}	SYNC_INx, DDC_INx, VIDEOx	V _I < 0	−50		mA
Output clamp current	I _{OK}	SYNC_OUTx, DDC_OUTx	V _O < 0	−50		mA
Continuous output current	I _O	SYNC_OUTx		−24	24	mA
		DDC_INx to DDC_OUTx		−5	5	mA
Continuous current through supply pins		V _{CC_VIDEO} , V _{CC_SYNC} , V _{CC_DDC}		−50	50	mA
Storage temperature	T _{stg}			−55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT	
TPD7S019 in RSV Package					
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins except 1, 2, 3, 4, 7, 10, 12, and 14	±2000	V
			Pins 1, 2, 3, 7, 10, 12, and 14	±15000	
			Pin 4	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1000	
		IEC 61000-4-2 contact discharge	Pins 1, 2, 3, 7, 10, 12, and 14	±8000	
TPD7S019 in DBQ Package					
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins except 3, 4, 5, 6, 9, 12, 14, and 16	±2000	V
			Pins 3, 4, 5, 9, 12, 14, and 16	±15000	
			Pin 6	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1000	
		IEC 61000-4-2 contact discharge	Pins 3, 4, 5, 9, 12, 14, and 16	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage	V_{CC_VIDEO}		0	5.5	V
	V_{CC_DDC}		0	5.5	
	V_{CC_SYNC}		0	5.5	
IO voltage	$V_{IO(VIDEO)}$	VIDEOx pins	0	V_{CC_VIDEO}	V
Input voltage	$V_{I(SYNC)}$	SYNC pins	0	V_{CC_SYNC}	V
	$V_{I(DDC)}$	DDC_INx pins	0	5.5	V
Output voltage	$V_{O(DDC)}$	DDC_INx Pins	0	5.5	V
Operating temperature	T_A		–40	85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD7S019		UNIT
		DBQ (SSOP)	RSV (UQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	124.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67	52.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.3	53.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.9	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.9	53.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC_VIDEO}	V_{CC_VIDEO} supply current	$V_{CC_VIDEO} = 5\text{ V}$, VIDEO inputs at V_{CC_VIDEO} or GND		1	10	μA
I_{CC_DDC}	V_{CC_DDC} supply current	$V_{CC_DDC} = 5\text{ V}$		1	10	μA
I_{CC_SYNC}	V_{CC_SYNC} supply current	$V_{CC_SYNC} = 5\text{ V}$ SYNC inputs at GND or V_{CC_SYNC} , SYNC outputs unloaded		1	50	μA
		$V_{CC_SYNC} = 5\text{ V}$ SYNC inputs at 3 V; SYNC outputs unloaded			2	mA
I_{IO_VIDEO}	VIDEO input and output pins	$V_{IO_VIDEO} = 3\text{ V}$		0.01	1	μA
I_{OFF}	DDC pin power down leakage current	$V_{CC_DDC} \leq 0.4\text{ V}$, $V_{DDC_OUT} = 5\text{ V}$		0.01	1	μA
V_D	Diode forward voltage for lower clamp of VIDEO, DDC, SYNC output pins	$I_D = 8\text{ mA}$, lower clamp diode	–0.6	–0.8	–0.95	V
R_{DYN_VIDEO}	Dynamic resistance (VIDEO pins)	$I = 1\text{ A}$		1		Ω
V_{IH}	High-level SYNC logic input voltage	$V_{CC_SYNC} = 5\text{ V}$	2			V
V_{IL}	Low-level SYNC logic input voltage	$V_{CC_SYNC} = 5\text{ V}$			0.6	V
V_{OH}	High-level SYNC logic output voltage	$I_{OH} = 0\text{ mA}$, $V_{CC_SYNC} = 5\text{ V}$	4.85			V
V_{OH}	High-level SYNC logic output voltage	$I_{OH} = -24\text{ mA}$, $V_{CC_SYNC} = 5\text{ V}$	2			V
V_{OL}	Low-level SYNC logic output voltage	$I_{OL} = 0\text{ mA}$, $V_{CC_SYNC} = 5\text{ V}$			0.15	V
V_{OL}	Low-level SYNC logic output voltage	$I_{OL} = 24\text{ mA}$, $V_{CC_SYNC} = 5\text{ V}$			0.8	V
R_T	SYNC driver output resistance	$V_{CC_SYNC} = 5\text{ V}$, SYNC inputs at GND or 3 V		15		Ω
C_{IO_VIDEO}	IO capacitance of VIDEO pins	$V_{IO} = 2.5\text{ V}$, test frequency is 1 MHz		2.5	4	pF
t_{PLH}	SYNC driver L => H propagation delay	$C_L = 50\text{ pF}$; $V_{CC} = 5\text{ V}$, input t_R and $t_F \leq 5\text{ ns}$			12	ns
t_{PHL}	SYNC driver H => L propagation delay	$C_L = 50\text{ pF}$; $V_{CC} = 5\text{ V}$, input t_R and $t_F \leq 5\text{ ns}$			12	ns
t_R, t_F	SYNC driver output rise & fall times	$C_L = 50\text{ pF}$; $V_{CC} = 5\text{ V}$, input t_R and $t_F \leq 5\text{ ns}$		4		ns

TPD7S019

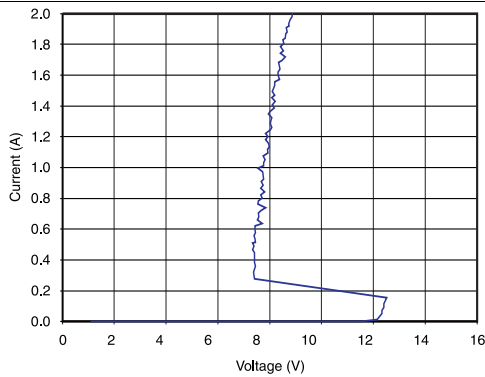
SLLSE33E –AUGUST 2010–REVISED DECEMBER 2016

www.ti.com**Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{BR}	VIDEO ESD diode break-down voltage	I _O = 1 mA	9			V

6.6 Typical Characteristics



$T_{rf} = 10$ ns

Figure 1. TPD7S019-xx TLP VID1 to GND, Barth

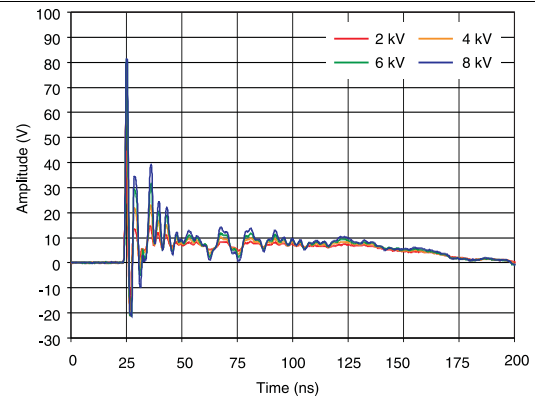


Figure 2. TPD7S019-xx IEC Clamping Waveforms Positive Contact

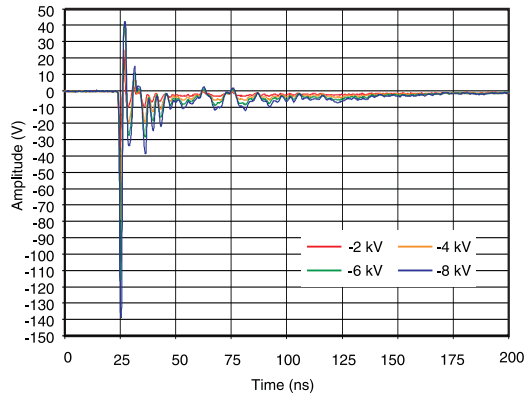
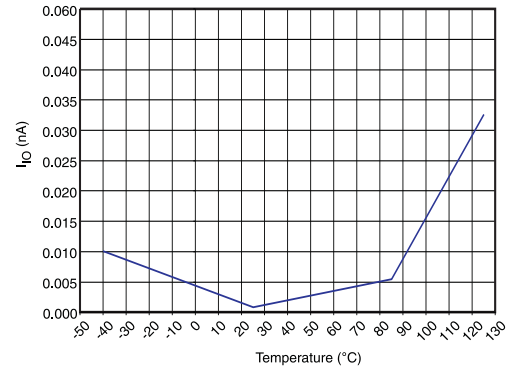
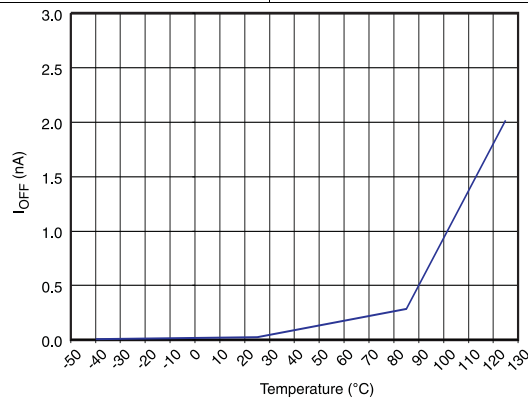


Figure 3. TPD7S019-xx IEC Clamping Waveforms Negative Contact



$V_{CC_VIDEO} = 5$ V

Figure 4. Leakage Current through VIDEO Pins



$V_{CC_DDC} = 0$ V

Figure 5. I_{OFF} (DDC_OUTx)

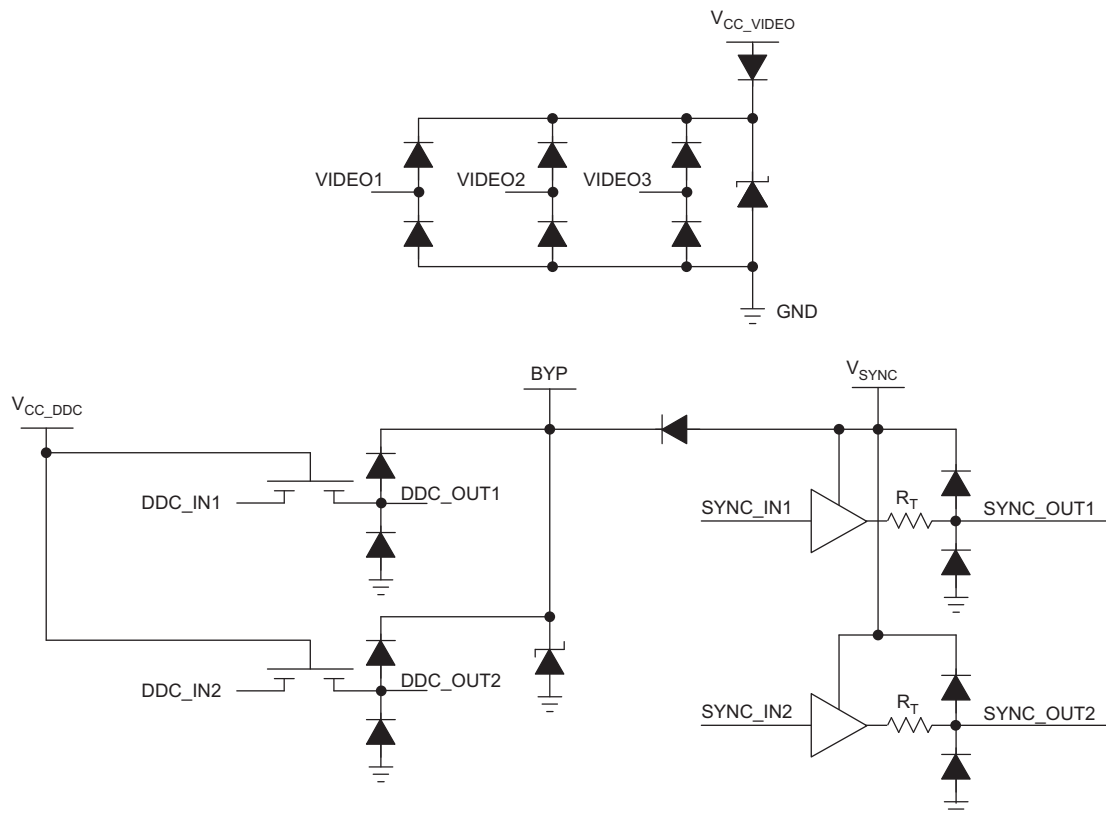
7 Detailed Description

7.1 Overview

The TPD7S019 is an integrated protection solution for VGA or DVI-I ports by providing high-speed ESD protection, level-shifting and signal buffering. The TVS protection diodes for VIDEO signals, DDC signals and SYNC signals provide robust ESD clamping that meets the IEC61000-4-2 standard for ± 8 -kV contact stress. The signals run at high speed is minimally affected by the low capacitance added to each signal line. The integrated level-shifters for the DDC signals help save external ICs. Two buffers on the HSYNC and VSYNC signals convert TTL input level to CMOS output level, and it saves external components by integrating series termination resistors connected to the SYNC_OUT pin. The TPD7S019 takes in three signal rails to make the signals compatible with different voltages on VIDEO, DDC and SYNC. The two package options provide the latitude to choose between either small board area or easier layout and better signal integrity.

The end applications of this device include desktop and laptop PCs, set top boxes, TVs, and monitors.

7.2 Functional Block Diagram



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7.3 Feature Description

The TPD7S019 is an integrated protection solution for VGA and DVI-I ports. It has the low capacitance ESD TVS diodes for the VIDEO signals to ensure high speed data transmission. Level-shifting on the DDC lines translate signals on the cable to the level can be processed by downstream ICs. Buffers on the SYNC lines condition the signal levels and quality. The integrated termination resistors help reduce external devices. The TPD7S019 exceeds IEC61000-4-2 (Level 4) ESD standard of ± 8 -kV contact discharge, making the system robust against system level ESD. The two package options provide the freedom to choose between a compact package or a flow through package.

7.4 Device Functional Modes

DDC level translators and SYNC signal buffers are active and the ESD cells on all the lines are untriggered when the recommended operating conditions are met. The bidirectional voltage-level translators provide noninverting level-shifting from the system side to the connector side. Each connector side pin has an ESD clamp that triggers when voltages are above V_{BR} or below the lower diode's V_f . During ESD events, voltages as high as ± 8 -kV (contact ESD) can be directed to ground through the internal diode network. Once the voltages on the protected line fall below these trigger levels (usually within 10s of nano-seconds), these pins revert to a non-conductive state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When a system contains a human interface connector, it becomes vulnerable to large system-level ESD strikes that standard ICs cannot survive. The TPD7S019 provides IEC61000-4-2 Level 4 Contact ESD rating to the VGA or DVI-I port. The integrated voltage level-shifting, buffering and termination reduce the board space needed to implement the control lines functions.

8.2 Typical Application

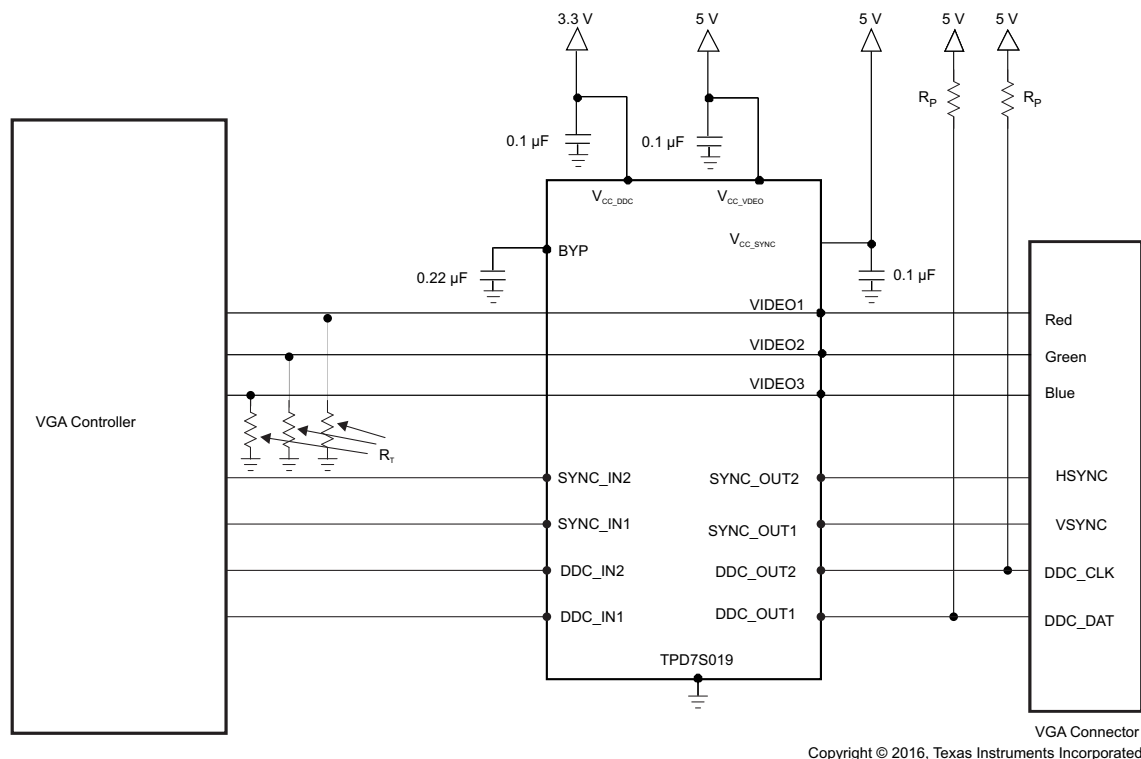


Figure 6. Typical Application Schematic with TPD7S019

8.2.1 Design Requirements

In this application, the TPD7S019 is used to protect the VGA port. [Table 1](#) lists the system parameters.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Pull-up resistors on DDC lines	1.5 kΩ to 2 kΩ
Termination resistors on VIDEO lines	50 Ω to 75 Ω
VIDEO signals data rate	24 MHz to 388 MHz
Required IEC 61000-4-2 ESD Protection	±8-kV Contact

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer must make sure:

- Voltage range on the protected line must not exceed the reverse standoff voltage of the TVS diode(s) (V_{RWM})
- Operating frequency is supported by the I/O capacitance C_{IO} of the TVS diode
- IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode

For this application, the DDC signals switch between 0 V and 5 V (with resistor pulling it up to 5-V power supply). The VIDEO and SYNC signal levels are between 0 V and $V_{CC_VIDEO} / V_{CC_SYNC}$. All signals are not exceeding the recommended values and the ESD cells on these pins stay untriggered.

Depending on the resolution and the refresh rate of the display, the VIDEO (RGB) signals' bandwidth can be from 24 MHz to 388 MHz. The line capacitances from the ESD cells are 2.5 pF typical which is only takes up a small portion of the total capacitance budget for the maximum frequency in this range.

±8-kV Contact ESD provided by the TPD7S019 meets the ESD design goal of ±8 kV contact.

Put 1.5-k Ω to 2-k Ω pullup resistor on the DDC lines to be compliant with the I²C standard. Termination resistors on VIDEO lines are 50 Ω to 75 Ω to match the impedance on board trace.

8.2.3 Application Curves

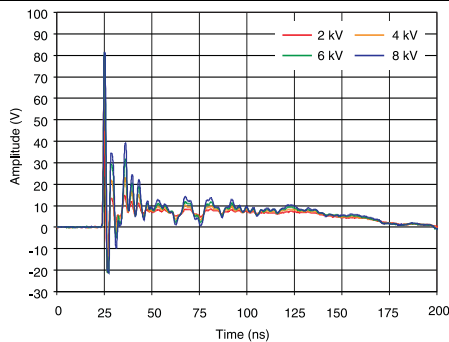


Figure 7. IEC 61000-4-2 Clamping Voltage, Positive Contact

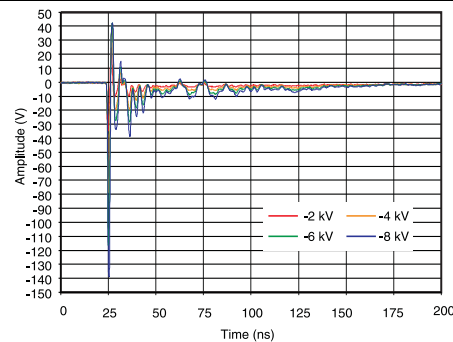


Figure 8. IEC 61000-4-2 Clamping Voltage, Negative Contact

9 Power Supply Recommendations

The TPD7S019 has three power supply pins: V_{CC_DDC} , V_{CC_SYNC} and V_{CC_VIDEO} . Depending on the system, the recommended voltage level of these three power supplies can be as high as 5.5 V.

10 Layout

10.1 Layout Guidelines

The optimum placement of this device is as close to the connector as possible. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. Therefore, the PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces as straight as possible.

Avoid using VIAs between the connector and an I/O protection pin on the TPD7S019.

Avoid 90° turns in traces since electric fields tend to build up on corners, increasing EMI coupling.

Minimize impedance on the path to GND for maximum ESD dissipation.

The capacitors on V_{CC_VIDEO} , V_{CC_DDC} and V_{CC_SYNC} must be placed close to their respective pins.

The VIDEO lines internal protection circuits are the same and thus these pins are interchangeable for routing.

10.2 Layout Example

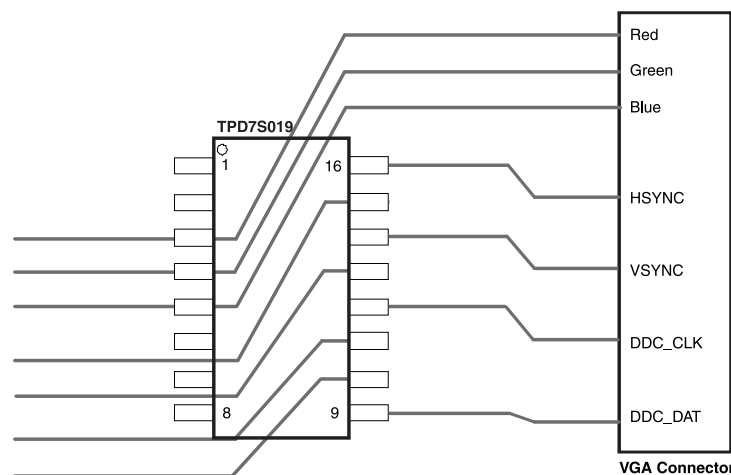


Figure 9. Simplified Layout with TPD7S019 (Only IO Lines are Shown)

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- [Reading and Understanding an ESD Protection Datasheet](#)
- [ESD Layout Guide](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD7S019-15DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PQ19-15	Samples
TPD7S019-15RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZUS	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

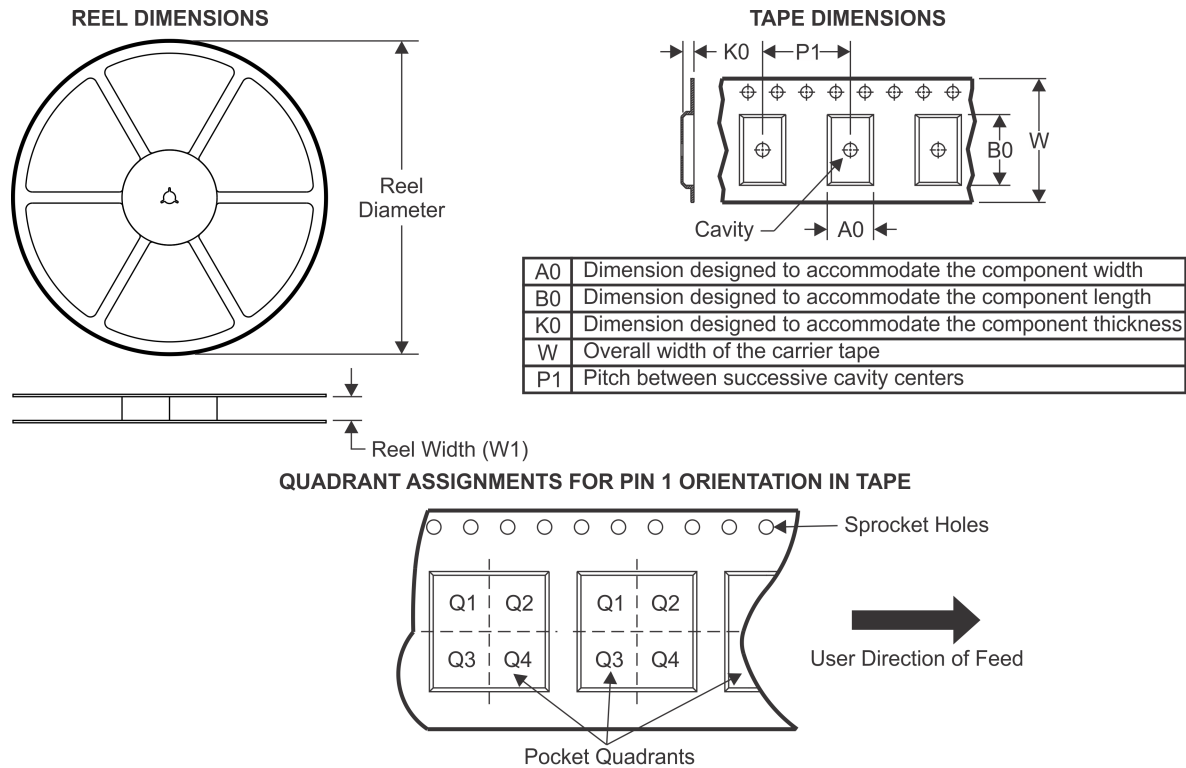
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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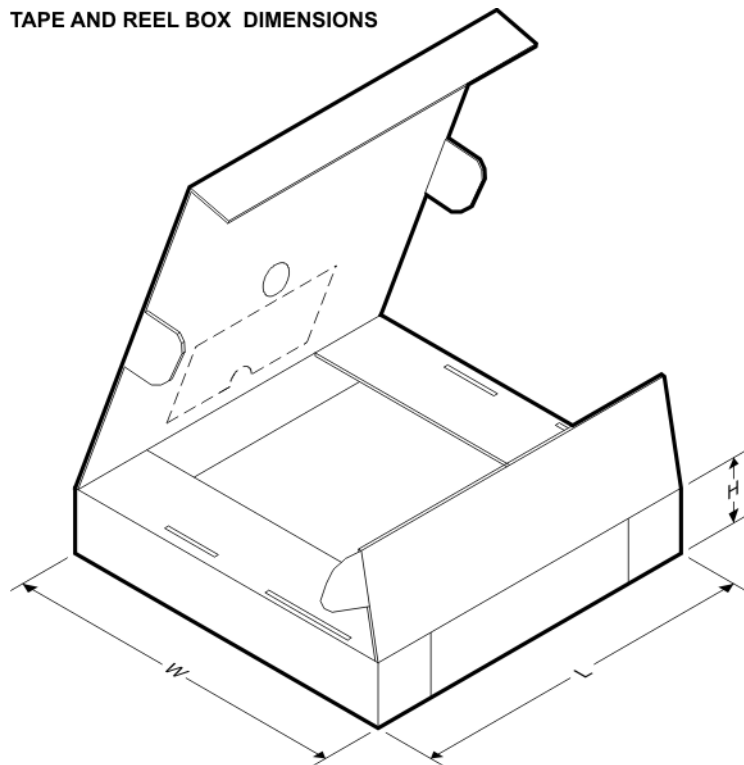
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD7S019-15DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPD7S019-15RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD7S019-15DBQR	SSOP	DBQ	16	2500	340.5	336.1	25.0
TPD7S019-15RSVR	UQFN	RSV	16	3000	183.0	183.0	20.0

UQFN - 0.55 mm max height

Figure 1: Mechanical drawing of the connector. The drawing includes three views: a top view, a side view, and a front view. The top view shows a rectangular component with a "PIN 1 INDEX AREA" indicated by a dashed line and a dot. Dimensions include 1.85 and 1.75 for the top width, and 2.65 and 2.55 for the height. The side view shows a profile with dimensions 0.55, 0.45, 0.05, and 0.00. A "SEATING PLANE" is indicated with a triangle symbol. The front view shows a symmetrical component with dimensions 2X 1.2, 5, 8, 4, 9, 15X 0.45, 15X 0.35, 12X 0.4, 1, 12, 16X 0.25, 16X 0.15, 0.07, 0.05, and 0.55. A "PIN 1 ID (45° X 0.1)" is indicated at the bottom. A table of material properties is provided at the bottom right.

⊕	0.07	M	C	A	B
	0.05	M			

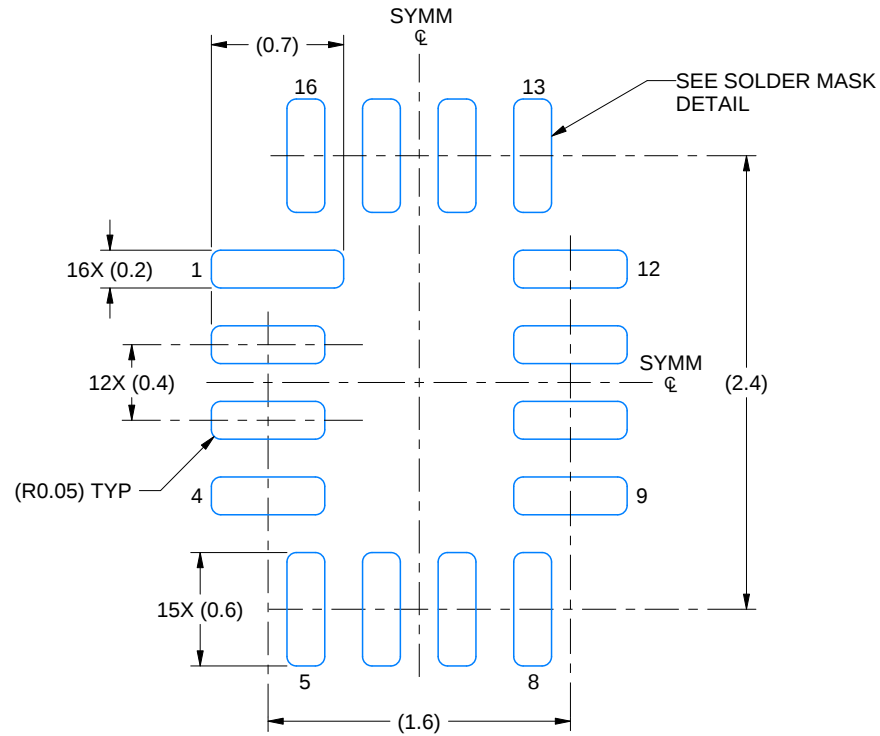
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

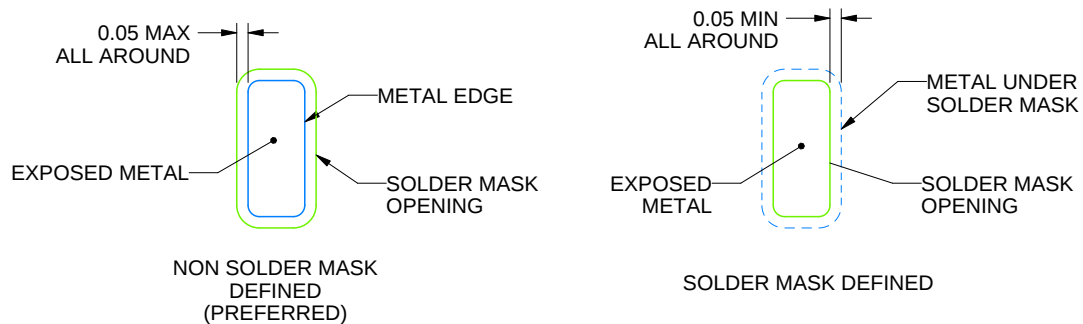
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

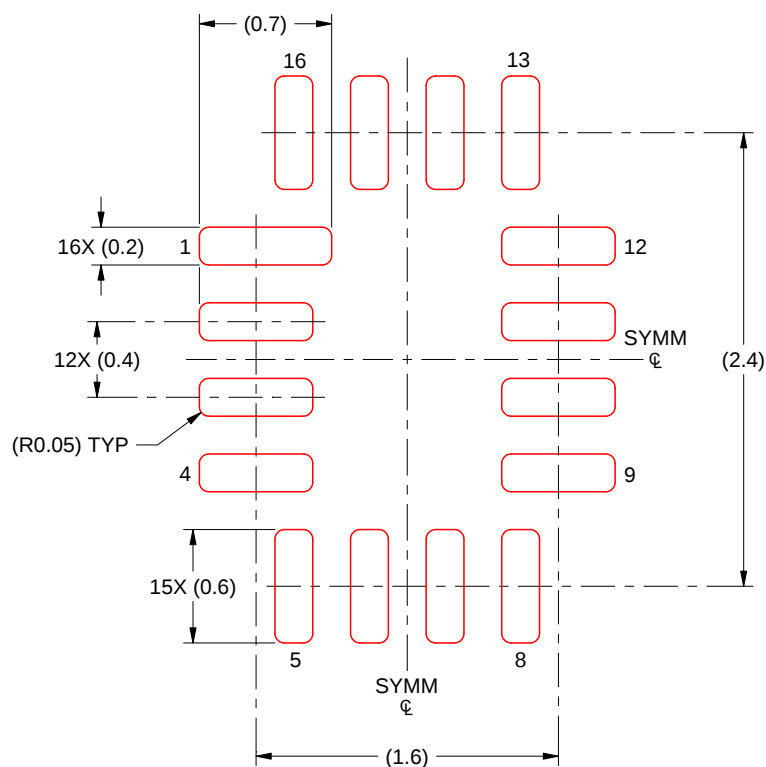
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).

EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

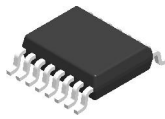


SOLDER PASTE EXAMPLE
 BASED ON 0.125 MM THICK STENCIL
 SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

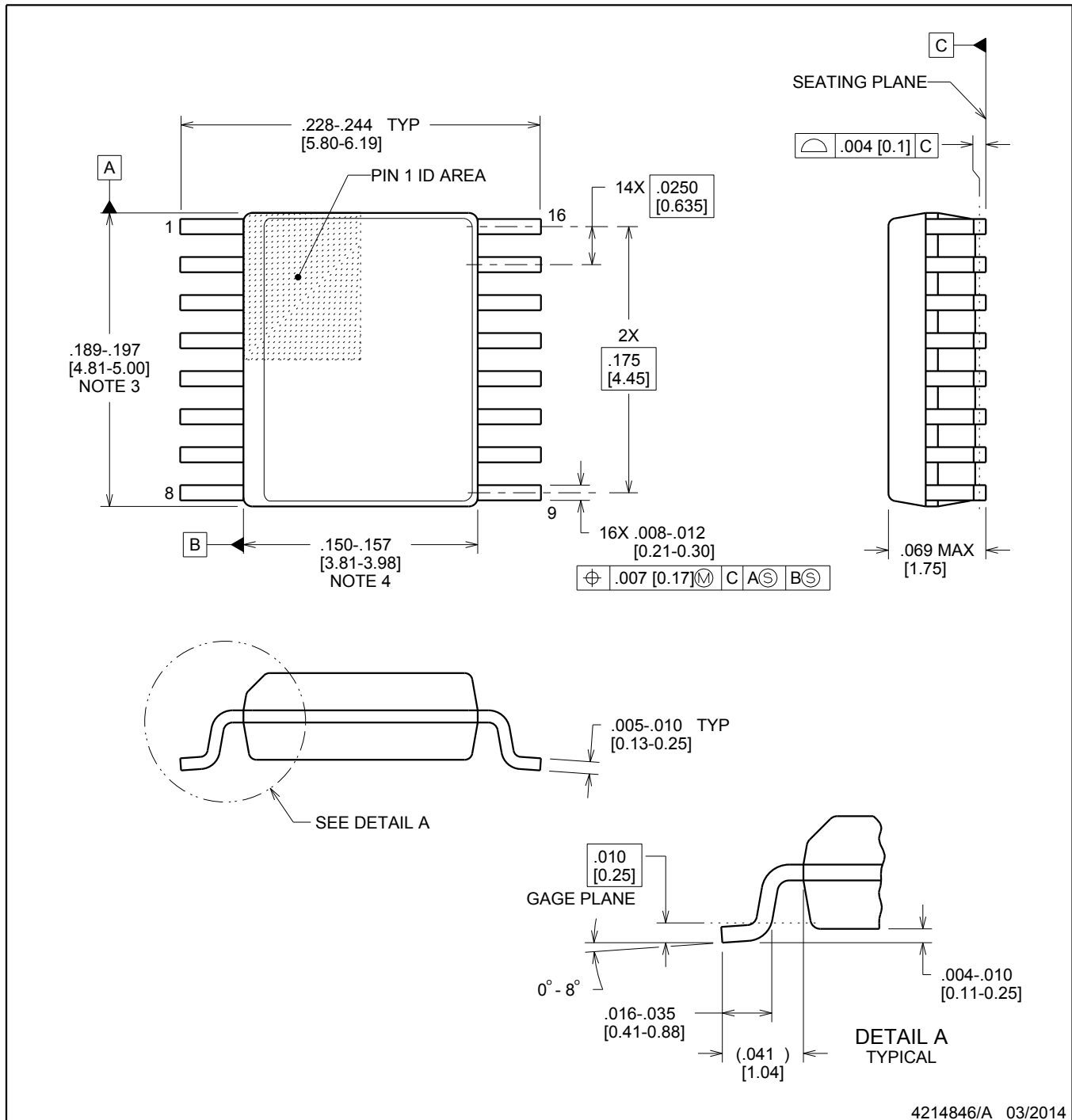


DBQ0016A

PACKAGE OUTLINE

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

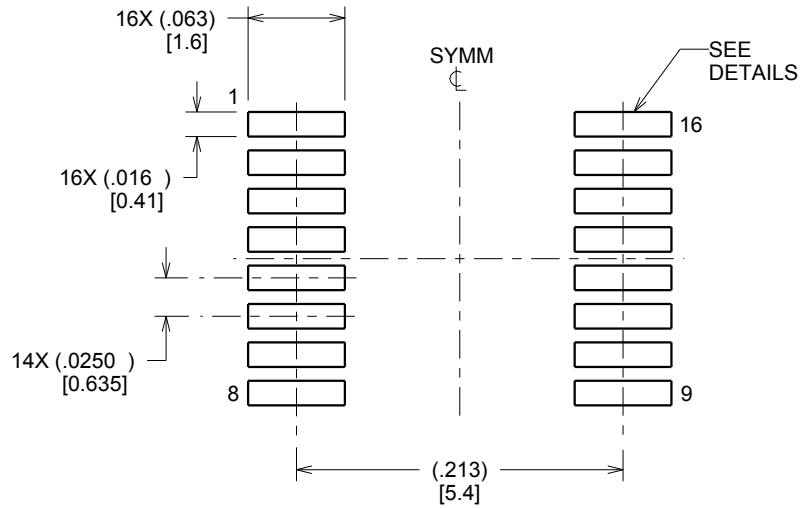
NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MO-137, variation AB.

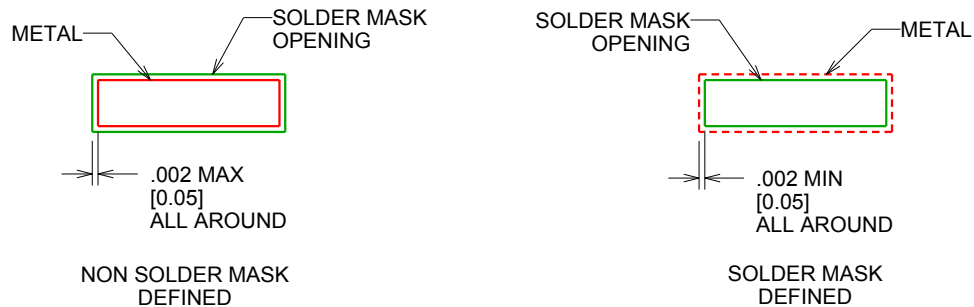
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

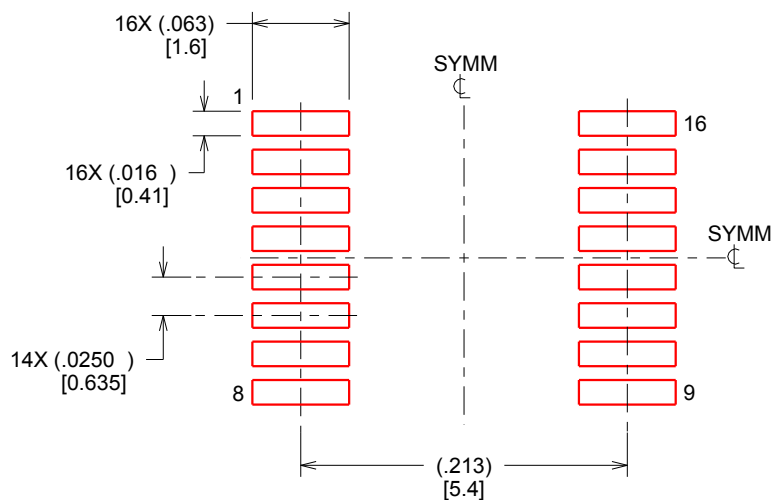
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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