350mA Dual Rail Linear Regulator

Check for Samples: LP5952

FEATURES

- **Excellent load transient response: ±15mV typical**
- **Excellent line transient response: ±1mV typical**
- **0.7V ≤ V_{IN} ≤ 4.5V**
- **2.5V ≤ V_{BATT} ≤ 5.5V**
- **0.5V ≤ V_{OUT} ≤ 2.0V**
- **For I_{LOAD} = 350mA:**
  - **V_{BATT} ≥ $V_{OUT(NOM)}$ + 1.5V or 2.5V whichever is higher**
- **For I_{LOAD} = 150mA:**
  - **V_{BATT} ≥ $V_{OUT(NOM)}$ + 1.3V or 2.5V whichever is higher**
- **50µA typical quiescent current from V_{BATT}**
- **10µA typical quiescent current from V_{IN}**
- **0.1µA typical quiescent current in shutdown**
- **Ensured 350mA output current**
- **Noise voltage = 100µV_{RMS} typical**
- **Operates from a single Li-Ion cell or 3 cell**
- **NiMH/NiCd batteries**
- **Only one or two tiny surface-mount external components required depending on application**
- **Small, thin 5-bump DSBGA package and 6-pin Chip On Lead USON package, lead free**
- **Thermal-overload and short-circuit protection**
- **-40°C to +125°C junction temperature range**

APPLICATIONS

- **Mobile Phones**
- **Hand-Held Radios**
- **Personal Digital Assistants**
- **Palm-Top PCs**
- **Portable Instruments**
- **Battery Powered Devices**

DESCRIPTION

The LP5952 is a Dual Supply Rail Linear Regulator optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries.

In the typical post regulation application V_{BATT} is directly connected to the battery (range 2.5V...5.5V) and V_{IN} is supplied by the output voltage of the DC-DC Converter (range 0.7V...4.5V).

The device offers superior dropout and transient features combined with very low quiescent currents. In shutdown mode (Enable pin pulled low) the device turns off and reduces battery consumption to 0.1µA (typ.).

The LP5952 also features internal protection against over-temperature, over-current and under-voltage conditions.

Performance is specified for a -40°C to 125°C junction temperature range.

Typical Application Circuit

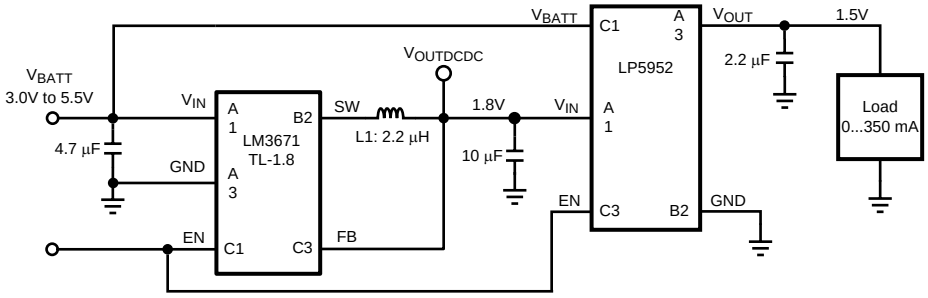


Figure 1. Typical Application Circuit with DC-DC Converter as Pre-Regulator for V_{IN}

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DESCRIPTION (CONTINUED)

The device is available in a tiny 5-bump DSBGA and a 6-pin Chip On Lead USON package, lead free.

The device is available in fixed output voltages in the range of 0.5V to 2.0V. For availability, please contact your local Texas Instruments sales office.

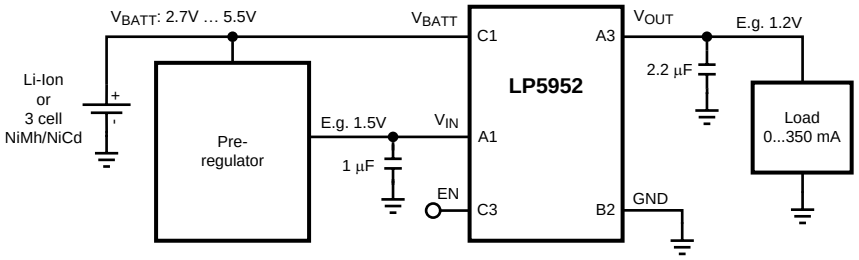


Figure 2. Typical Application Circuit

Connection Diagram

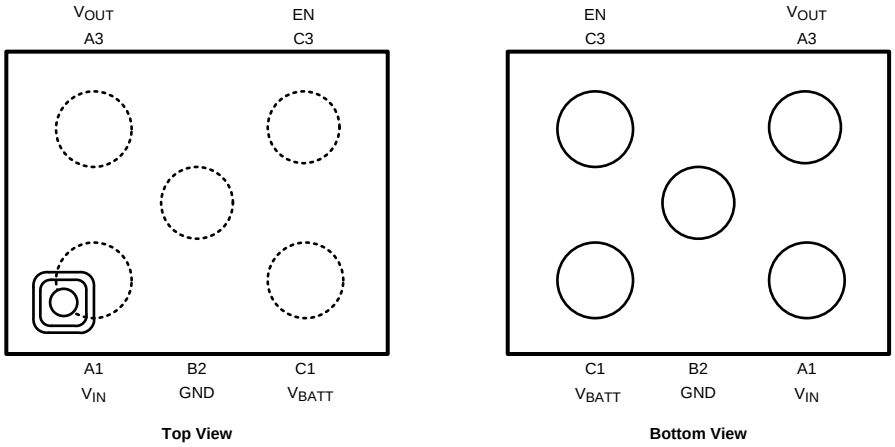


Figure 3. 5-Bump Thin DSBGA Package, Large Bump, 0.5mm Pitch
See Package Number YZR0005

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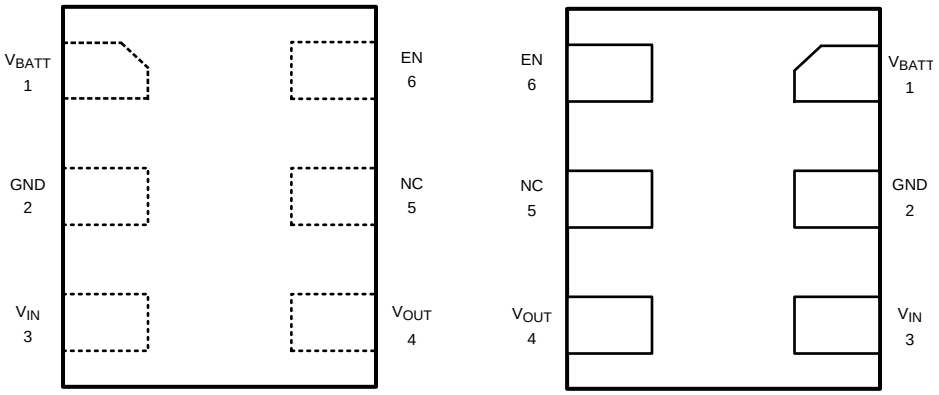


Figure 4. 6-Pin Chip On Lead USON package, 0.5mm pitch
See Package Number NKH0006B

PIN DESCRIPTIONS

Pin Number DSBGA	Pin Number USON	Pin Name	Description
A1	3	V_{IN}	Power input voltage; input range: 0.7V to 4.5V, $V_{IN} \le V_{BATT}$
A3	4	V_{OUT}	Regulated output voltage
B2	2	GND	Ground
C1	1	V_{BATT}	Bias input voltage; input range: 2.5V to 5.5V
C3	6	EN	Enable pin logic input: low = shutdown, high = active, normal operation. This pin should not be left floating. Tie to V_{BATT} if this function is not used.
	5	NC	Do not make connections to this pin

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2][3]

V_{IN}, V_{BATT} pins: Voltage to GND, $V_{IN} \le V_{BATT}$		-0.2V to 6.0V
V_{BATT} pin to V_{IN} pin		0.2V
EN pin, Voltage to GND		-0.2V to 6.0V
Continuous Power Dissipation[4]		Internally Limited
Junction Temperature (T_{J-MAX})		150°C
Storage Temperature Range		-65°C to + 150°C
Package Peak Reflow Temperature (Pb-free, 10-20 sec.)[5]		260°C
ESD Rating[6]	Human Body Mode	2.0kV
	Machine Model	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typ.) and disengages at T_J = 145°C (typ.).
(5) For detailed soldering specifications and information, please refer to Application Note 1112: DSBGA Wafer Level Chip Scale Package (SNVA009) and Application Note 1187: Leadless Leadframe Package (LLP) (SNOA401).
(6) The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. (MIL-STD-883 3015.7)

Operating Ratings

Input Voltage Range V_{IN}	0.7V to 4.5V
Input Voltage Range V_{BATT}	2.5V to 5.5V
V_{EN} Input Voltage	0 to V_{BATT}
Recommended Load Current	0mA to 350mA
Junction Temperature (T_J) Range	-40°C to + 125°C
Ambient Temperature (T_A) Range[1]	-40°C to + 85°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance(θ_{JA})	
YZR0005 package[1]	95°C/W
NKH0006B package[1]	150°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special attention must be paid to thermal dissipation issues in board design.

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Electrical Characteristics (1)(2)(3)

Typical values and limits appearing in standard typeface are for T_A = 25°C. Limits appearing in **boldface** type apply over the full operating temperature range: -40°C ≤ T_J ≤ +125°C. Unless otherwise noted, specifications apply to the typical application circuit with V_{IN} = $V_{OUT(NOM)}$ + 1.0V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5V or 2.5V, whichever is higher, I_{OUT} = 1mA, C_{VIN} = 1.0µF, C_{OUT} = 2.2µF, V_{EN} = V_{BATT}.

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
ΔV_{OUT} / V_{OUT}	Output Voltage Tolerance	V_{IN} = $V_{OUT(NOM)}$ + 0.3V		-1.5 **-2.0**	1.5 **2.0**	% %
ΔV_{OUT} / ΔV_{IN}	Line Regulation Error	V_{IN} = $V_{OUT(NOM)}$ + 0.3V to 4.5V, V_{BATT} = 4.5V	0.3		**1.0**	mV/V
ΔV_{OUT} / ΔV_{BATT}		V_{BATT} = $V_{OUT(NOM)}$ + 1.5V (≥ 2.5V) to 5.5V	0.5		**2.2**	
ΔV_{OUT} / ΔmA	Load Regulation Error	I_{OUT} = 1mA to 350mA, DSBGA package	15		**30**	µV/mA
		I_{OUT} = 1mA to 350mA, USON-6 package	43		**60**	µV/mA
I_{SC}	Output Current (short circuit)	V_{OUT} = 0V, V_{EN} = V_{IN} = V_{BATT} = $V_{OUT(NOM)}$ + 1.5V	500	**350**		mA
V_{DO_VBATT} (4)	Output Voltage Dropout V_{BATT} (5)	I_{OUT} = 350mA, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, DSBGA package	1.07		**1.5**	V
		I_{OUT} = 350mA, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, USON-6 package	1.08		**1.5**	V
		I_{OUT} = 150mA, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, DSBGA package	0.96		**1.3**	V
		I_{OUT} = 150mA, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, USON-6 package	0.97		**1.3**	V
V_{DO_VIN}	Output Voltage Dropout V_{IN}	I_{OUT} = 350mA, V_{BATT} = $V_{OUT(NOM)}$ + 1.5V or 2.5V, DSBGA package	88		**200**	mV
		I_{OUT} = 350mA, V_{BATT} = $V_{OUT(NOM)}$ + 1.5V or 2.5V, USON-6 package	128		**250**	mV
E_N	Output Noise	10Hz to 100kHz	100			μV_{RMS}
PSRR	Power Supply Rejection Ratio	Sine modulated V_{BATT} f = 10Hz f = 100Hz f = 1kHz	 70 65 45			 dB dB dB
		Sine modulated V_{IN} f = 10Hz f = 100Hz f = 1kHz f = 10kHz f = 100kHz	 80 90 95 85 64			 dB dB dB dB dB

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical (Typ) numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1.0V, V_{BATT}= $V_{OUT(NOM)}$ + 1.5V or 2.5V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option
(4) This specification does not apply if the battery voltage V_{BATT} needs to be decreased below the minimum operating limit of 2.5V during this test.
(5) Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100mV below the nominal output voltage.

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Electrical Characteristics Quiescent Currents(1)(2)(3)

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
I_{Q_VBATT}	Current into V_{BATT}	I_{LOAD} = 0...350mA	50		**100**	µA
I_{Q_VIN}	Current into V_{IN}	I_{LOAD} = 0	11		**28**	µA

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical (Typ) numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1.0V, V_{BATT}= $V_{OUT(NOM)}$ + 1.5V or 2.5V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option

Electrical Characteristics Shutdown Currents(1)(2)(3)

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
I_{Q_VBATT}	Current into V_{BATT}	V_{EN} = 0V	0.1		**1**	µA
I_{Q_VIN}	Current into V_{IN}	V_{EN} = 0V	0.1		**1**	µA

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical (Typ) numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1.0V, V_{BATT}= $V_{OUT(NOM)}$ + 1.5V or 2.5V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option

Electrical Characteristics Enable Control Characteristics(1)(2)(3)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
I_{EN}	Maximum Input Current at V_{EN} Input		0.01		**1**	µA
V_{IL}	Low Input Threshold (shutdown)				**0.4**	V
V_{IH}	High Input Threshold (enable)			**1.0**		V

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical (Typ) numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1.0V, V_{BATT}= $V_{OUT(NOM)}$ + 1.5V or 2.5V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option

Electrical Characteristics Thermal Protection(1)(2)(3)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
T_{SHDN}	Thermal-Shutdown Temperature		165			°C
ΔT_{SHDN}	Thermal-Shutdown Hysteresis		20			°C

(1) All voltages are with respect to the potential at the GND pin.
(2) $V_{OUT(NOM)}$ is the stated output voltage option
(3) Min and Max limits are ensured by design, test, or statistical analysis. Typical (Typ) numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1.0V, V_{BATT}= $V_{OUT(NOM)}$ + 1.5V or 2.5V, whichever is higher, T_A = 25°C.

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Electrical Characteristics Transient Characteristics(1)(2)(3)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
ΔV_{OUT}	Dynamic Line Transient Response V_{IN}	V_{IN} = $V_{OUT(NOM)}$ + 0.3V to $V_{OUT(NOM)}$ + 0.9V; tr, tf = 10µs	±1			mV
ΔV_{OUT}	Dynamic Line Transient Response V_{BATT}	V_{BATT} = $V_{OUT(NOM)}$ + 1.5V to $V_{OUT(NOM)}$ + 2.1V; tr, tf = 10µs	±15			mV
ΔV_{OUT}	Dynamic Load Transient Response	Pulsed load 0 ...300mA, di/dt = 300mA/1µs DSBGA package	±15			mV
		Pulsed load 0 ...300mA, di/dt = 300mA/1µs USON-6 package	-35/+15			mV
$T_{STARTUP}$	Startup Time	EN to 0.95 * V_{OUT}	70		**150**	µs

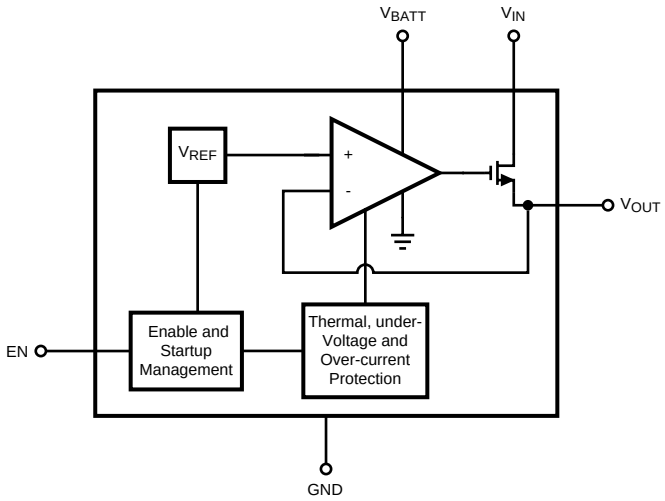
(1) All voltages are with respect to the potential at the GND pin.
(2) $V_{OUT(NOM)}$ is the stated output voltage option
(3) Min and Max limits are ensured by design, test, or statistical analysis. Typical (Typ) numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1.0V, V_{BATT}= $V_{OUT(NOM)}$ + 1.5V or 2.5V, whichever is higher, T_A = 25°C.

Electrical Characteristics Input and Output Capacitors, Recommended Specification(1)(2)(3)

Symbol	Parameter	Conditions	Nom	Limit		Units
				Min	Max	
C_{OUT}	Output Capacitance	Capacitance(4)	2.2	1.5	10	µF
		ESR		3	300	mΩ
C_{VIN}	Input Capacitance at V_{IN}	Capacitance(4), not needed in typ post regulation application, seeFigure 1	1	0.47		µF
		ESR		3	300	mΩ

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical (Typ) numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1.0V, V_{BATT}= $V_{OUT(NOM)}$ + 1.5V or 2.5V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option
(4) The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. The shown minimum limit represents real minimum capacitance, including all tolerances and must be maintained over temperature and dc bias voltage (See capacitor section in Applications Hints)

BLOCK DIAGRAM



Typical Performance Characteristics

Unless otherwise specified, C_{IN} = 1.0µF ceramic, C_{OUT} = 2.2µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5V, T_A = 25°C, Enable pin is tied to V_{BATT}. DSBGA package.

Load Transient Response, 0.7V Option

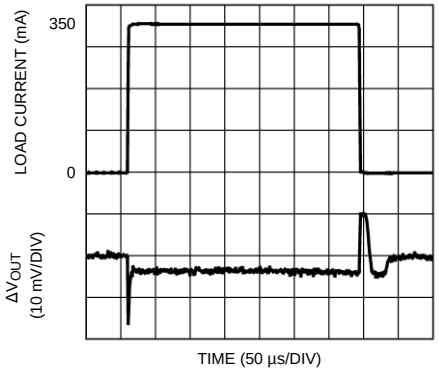


Figure 5.

Load Transient Response, 1.5V Option

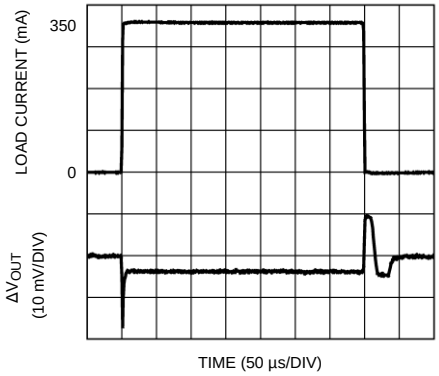


Figure 6.

Line Transient Response V_{IN}, 1.5V Option

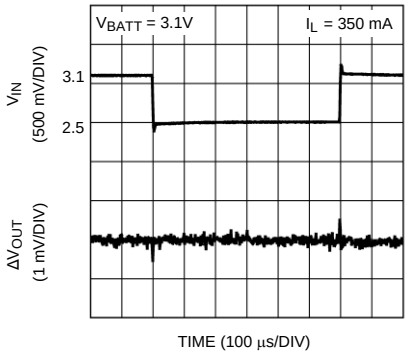


Figure 7.

Line Transient Response V_{BATT}, 1.5V Option

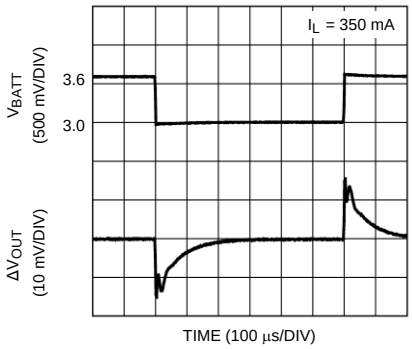


Figure 8.

Enable Start-up Time, 0.7V Option

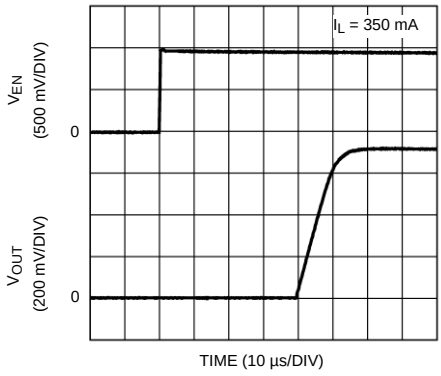


Figure 9.

Enable Start-up Time, 1.5V Option

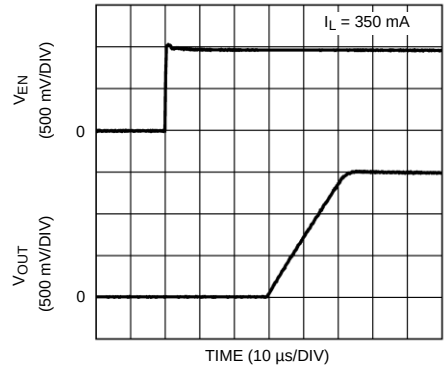


Figure 10.

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Typical Performance Characteristics (continued)

Unless otherwise specified, C_{IN} = 1.0µF ceramic, C_{OUT} = 2.2µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5V, T_A = 25°C, Enable pin is tied to V_{BATT}. DSBGA package.

Output Voltage Change vs Temperature

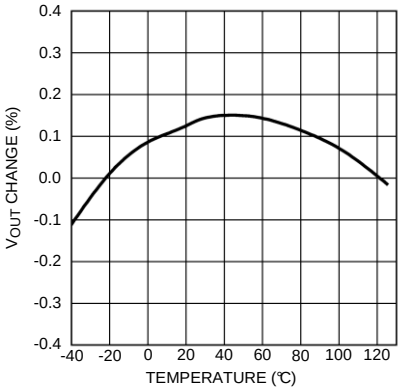


Figure 11.

Dropout V_{IN} vs Temperature, I_{LOAD} = 350mA

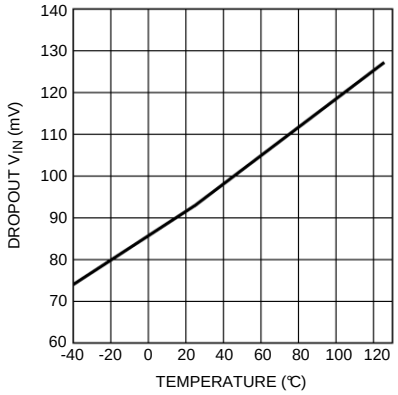


Figure 12.

Inrush Current V_{IN}, 1.5V Option

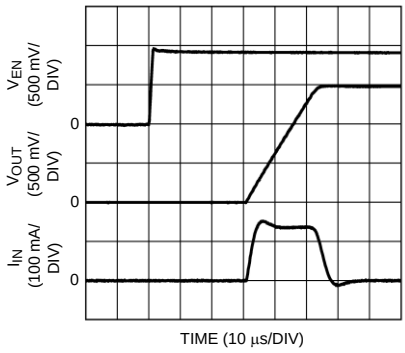


Figure 13.

Quiescent Current I_{Q_VBATT} vs V_{BATT}

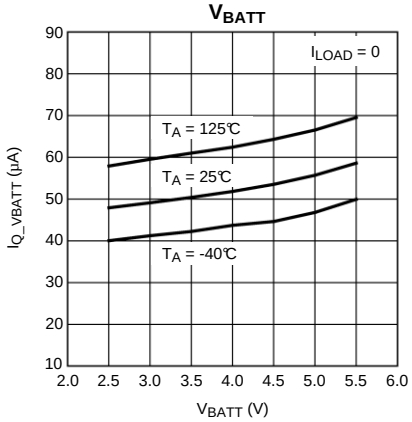


Figure 14.

Ground Current vs V_{BATT} / V_{IN}

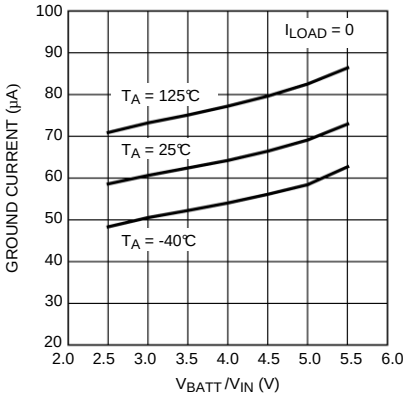


Figure 15.

Ground Current vs Load Current

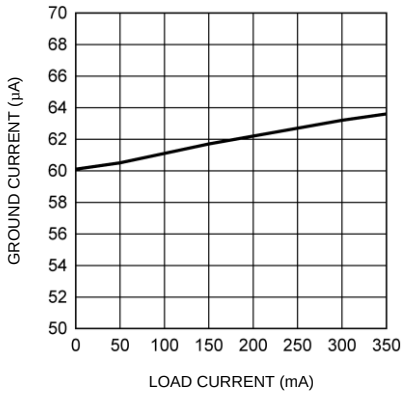


Figure 16.

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Typical Performance Characteristics (continued)

Unless otherwise specified, C_{IN} = 1.0µF ceramic, C_{OUT} = 2.2µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5V, T_A = 25°C, Enable pin is tied to V_{BATT}. DSBGA package.

Power Supply Rejection Ratio V_{IN}, 1.5V Option

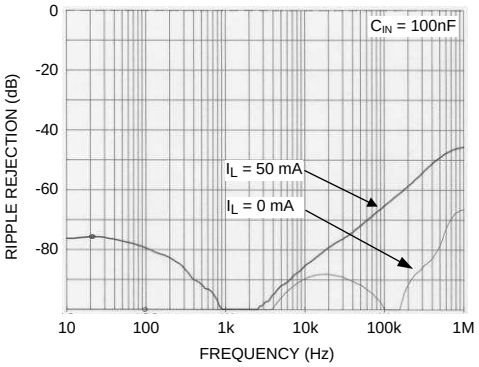


Figure 17.

Power Supply Rejection Ratio V_{BATT}, 1.5V Option

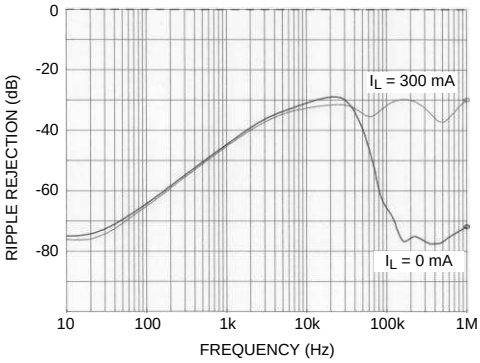


Figure 18.

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APPLICATION HINTS

DUAL RAIL SUPPLY

The LP5952 requires two different supply voltages:

- V_{IN}, the power input voltage, is regulated to the fixed output voltage
- V_{BATT}, the bias input voltage, supplies internal circuitry.

It's important that V_{IN} does not exceed V_{BATT} at any time. If the device is used in the typical post regulation application as shown in Figure 1, the sequencing of the two power supplies is not an issue as V_{BATT} supplies both, the DC-DC regulator and the LP5952. The output voltage of the DC-DC regulator will take some time to rise up and supply V_{IN} of LP5952. In this application V_{IN} will always ramp up more slowly than V_{BATT}.

In case V_{IN} is shorted to V_{BATT}, the voltages at the two supply pins will ramp up simultaneously causing no problem.

Only in applications with two independent supplies connected to the LP5952 special care must be taken to ensure that V_{IN} is always ≤ V_{BATT}.

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

As stated in the electrical specification section, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = (T_{J(MAX)} - T_A) / \theta_{JA} \quad (1)$$

With a θ_{JA} = 95°C/W, the device in the 5 bump DSBGA package returns a value of 1053mW with a maximum junction temperature of 125°C at T_A of 25°C or 421mW at T_A of 85°C.

The actual power dissipation across the device can be estimated by the following equation:

$$P_D = (V_{IN} - V_{OUT}) * I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application. As an example, to keep full load current capability of 350mA for a 1.5V output voltage option at a high ambient temperature of 85°C, V_{IN} has to be kept ≤ 2.7V (for DSBGA package):

$$V_{IN} \le P_D / I_{OUT} + V_{OUT} = 421mW / 350mA + 1.5V = 2.7V. \quad (3)$$

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Figure 19 shows the output current derating due to these considerations:

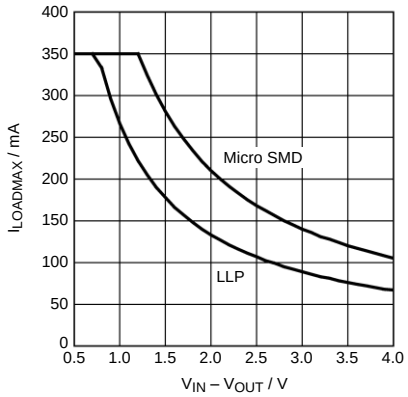


Figure 19. Maximum Load Current vs V_{IN} - V_{OUT}, T_A = 85°C, V_{OUT} = 1.5V, $\theta_{JA(DSBGA)}$ = 95°C/W, $\theta_{JA(USON)}$ = 150°C/W,

The typical contribution of the bias input voltage supply V_{BATT} to the power dissipation can be neglected:

$$P_{D_VBATT} = V_{BATT} * I_{QVBATT} = 5.5V * 50\mu A = 0.275mW \text{ typical.} \quad (4)$$

EXTERNAL CAPACITORS

As is common with most regulators, the LP5952 requires external capacitors to ensure stable operation. The LP5952 is specifically designed for portable applications requiring minimum board space and the smallest size components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

If the LP5952 is used stand alone, an input capacitor at V_{IN} is required for stability. It is recommended that a 1.0µF capacitor be connected between the LP5952 power voltage input pin V_{IN} and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the V_{IN} pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

A capacitor at V_{BATT} is not required if the distance to the supply does not exceed 5cm.

If the device is used in the typical application as post regulator after a DC-DC regulator, no input capacitors are required at all as the capacitors of the DC-DC regulator (C_{IN} and C_{OUT}) are sufficient if both components are mounted close to each other and a proper GND plane is used. If the distance between the output capacitor of the DC-DC regulator and the V_{IN} pin of the LP5952 is larger than 5cm, it's recommended to add the mentioned input capacitor at V_{IN}.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

The ESR (Equivalent Series Resistance) of the input capacitor should be in the range of 3mΩ to 300mΩ. The tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain ≥ 470nF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP5952 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X7R, Z5U, or Y5V) in the 2.2µF range (up to 10µF) and with an ESR between 3mΩ to 300mΩ is suitable as C_{OUT} in the LP5952 application circuit.

This capacitor must be located a distance of not more than 1cm from the V_{OUT} pin and returned to a clean analogue ground.

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It is also possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

CAPACITOR CHARACTERISTICS

The LP5952 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 1µF to 4.7µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1µF ceramic capacitor is in the range of 3mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP5952.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. The example shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.47/1.5µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

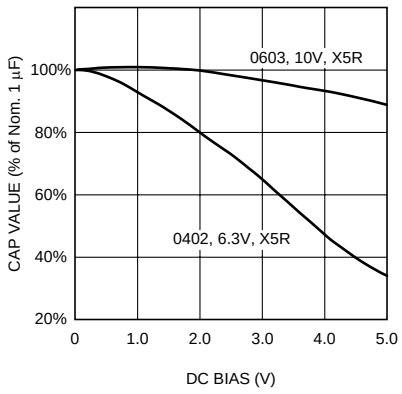


Figure 20. Graph Showing A Typical Variation In Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to +85°C. Many large value ceramic capacitors, larger than 1µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

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NO-LOAD STABILITY

The LP5952 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

ENABLE OPERATION

The LP5952 may be switched ON or OFF by a logic input at the Enable pin, V_{EN}. A logic high at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 0.1µA.

If the application does not require the Enable switching feature, the V_{EN} pin should be tied to V_{BATT} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under Enable Control Characteristics, V_{IL} and V_{IH}.

FAST TURN ON

Fast turn-on is ensured by an optimized architecture allowing a fast ramp of the output voltage to reach the target voltage while the inrush current is controlled low at 120mA typical (for a C_{OUT} of 2.2µF).

SHORT-CIRCUIT PROTECTION

The LP5952 is short circuit protected and in the event of a peak over-current condition, the output current through the NFET pass device will be limited.

If the over-current condition exists for a longer time, the average power dissipation will increase depending on the input to output voltage difference until the thermal shutdown circuitry will turn off the NFET.

Please refer to the section on thermal information for power dissipation calculations.

THERMAL-OVERLOAD PROTECTION

Thermal-Overload Protection limits the total power dissipation in the LP5952. When the junction temperature exceeds T_J = 165°C typ., the shutdown logic is triggered and the NFET is turned off, allowing the device to cool down. After the junction temperature dropped by 20°C (temperature hysteresis) typical, the NFET is activated again. This results in a pulsed output voltage during continuous thermal-overload conditions.

The Thermal-Overload Protection is designed to protect the LP5952 in the event of a fault condition. For normal, continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C (see Absolute Maximum Ratings).

REVERSE CURRENT PATH

The internal NFET pass device in LP5952 has an inherent parasitic body diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 50mA. For currents above this limit an external Schottky diode must be connected from V_{OUT} to V_{IN} (cathode on V_{IN}, anode on V_{OUT}).

EVALUATION BOARDS

For availability of evaluation boards please refer to the Product Folder of LP5952 at www.ti.com.

For information regarding evaluation boards, please refer to Application Note: AN-1531 SNVA188.

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REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	14

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5952LC-1.2/NOPB	ACTIVE	USON	NKH	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L28	Samples
LP5952LC-1.3/NOPB	ACTIVE	USON	NKH	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L43	Samples
LP5952LC-1.5/NOPB	ACTIVE	USON	NKH	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L25	Samples
LP5952LC-1.8/NOPB	ACTIVE	USON	NKH	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L29	Samples
LP5952TL-1.0/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L	Samples
LP5952TL-1.2/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
LP5952TL-1.3/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5952TL-1.5/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	Samples
LP5952TL-1.6/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
LP5952TL-1.8/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
LP5952TLX-0.7/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	4	Samples
LP5952TLX-1.0/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L	Samples
LP5952TLX-1.2/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
LP5952TLX-1.5/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	Samples
LP5952TLX-1.8/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

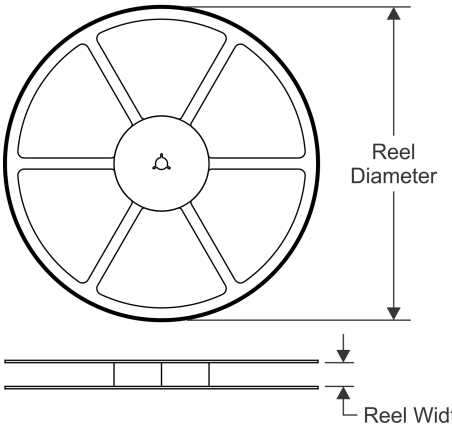
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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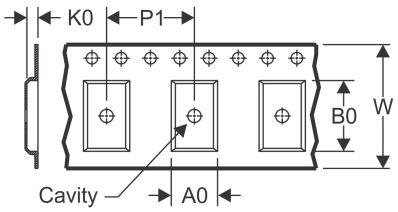
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

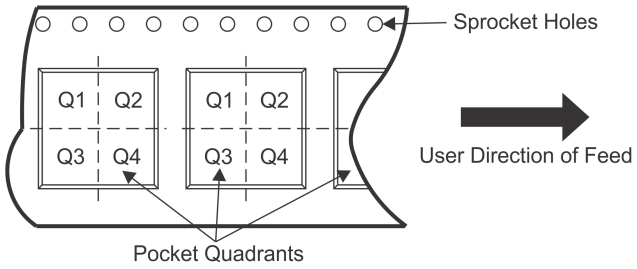


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

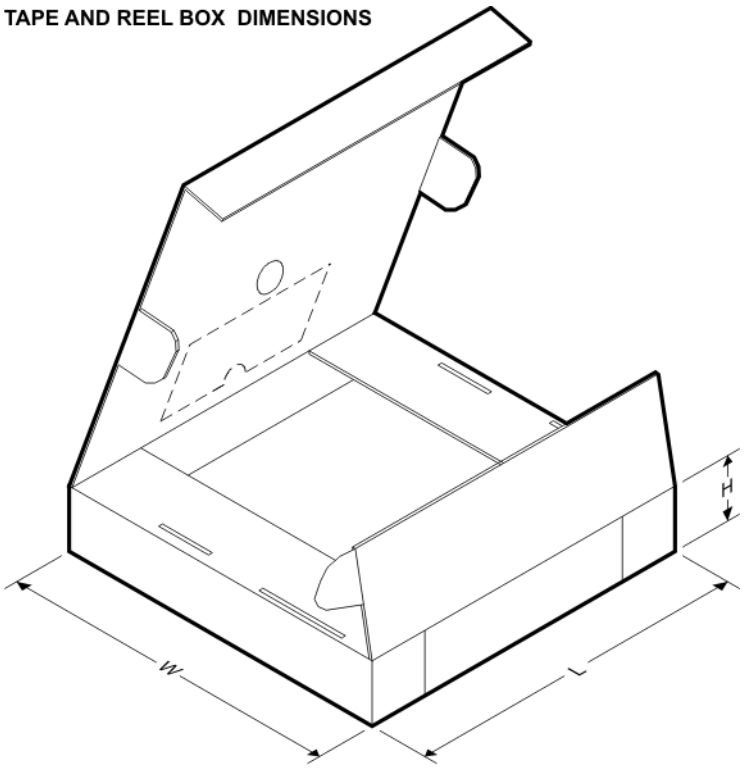
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5952LC-1.2/NOPB	USON	NKH	6	1000	178.0	12.4	2.2	2.2	1.0	8.0	12.0	Q1
LP5952LC-1.3/NOPB	USON	NKH	6	1000	178.0	12.4	2.2	2.2	1.0	8.0	12.0	Q1
LP5952LC-1.5/NOPB	USON	NKH	6	1000	178.0	12.4	2.2	2.2	1.0	8.0	12.0	Q1
LP5952LC-1.8/NOPB	USON	NKH	6	1000	178.0	12.4	2.2	2.2	1.0	8.0	12.0	Q1
LP5952TL-1.0/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TL-1.2/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TL-1.3/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TL-1.5/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TL-1.6/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TL-1.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TLX-0.7/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TLX-1.0/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TLX-1.2/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TLX-1.5/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TLX-1.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1

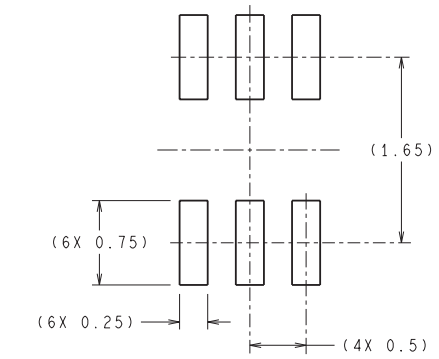
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

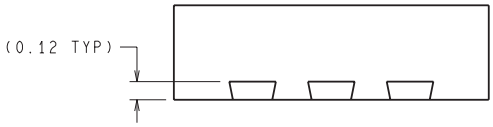
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5952LC-1.2/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LP5952LC-1.3/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LP5952LC-1.5/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LP5952LC-1.8/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LP5952TL-1.0/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TL-1.2/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TL-1.3/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TL-1.5/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TL-1.6/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TL-1.8/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TLX-0.7/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP5952TLX-1.0/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP5952TLX-1.2/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP5952TLX-1.5/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP5952TLX-1.8/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0

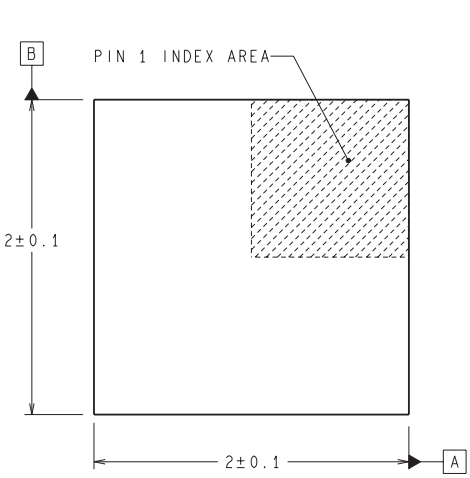
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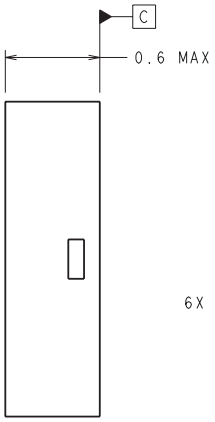


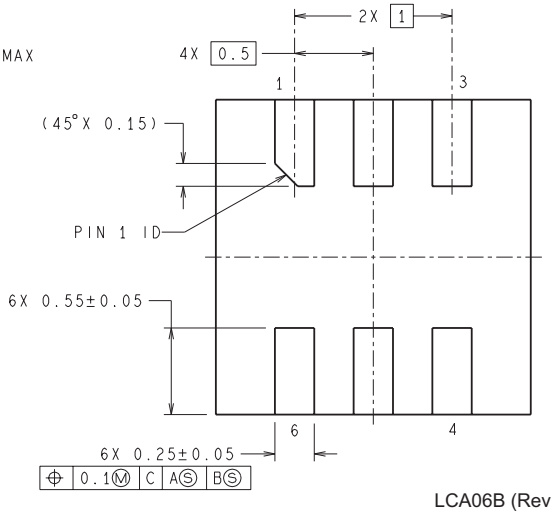
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN ( ) FOR REFERENCE ONLY



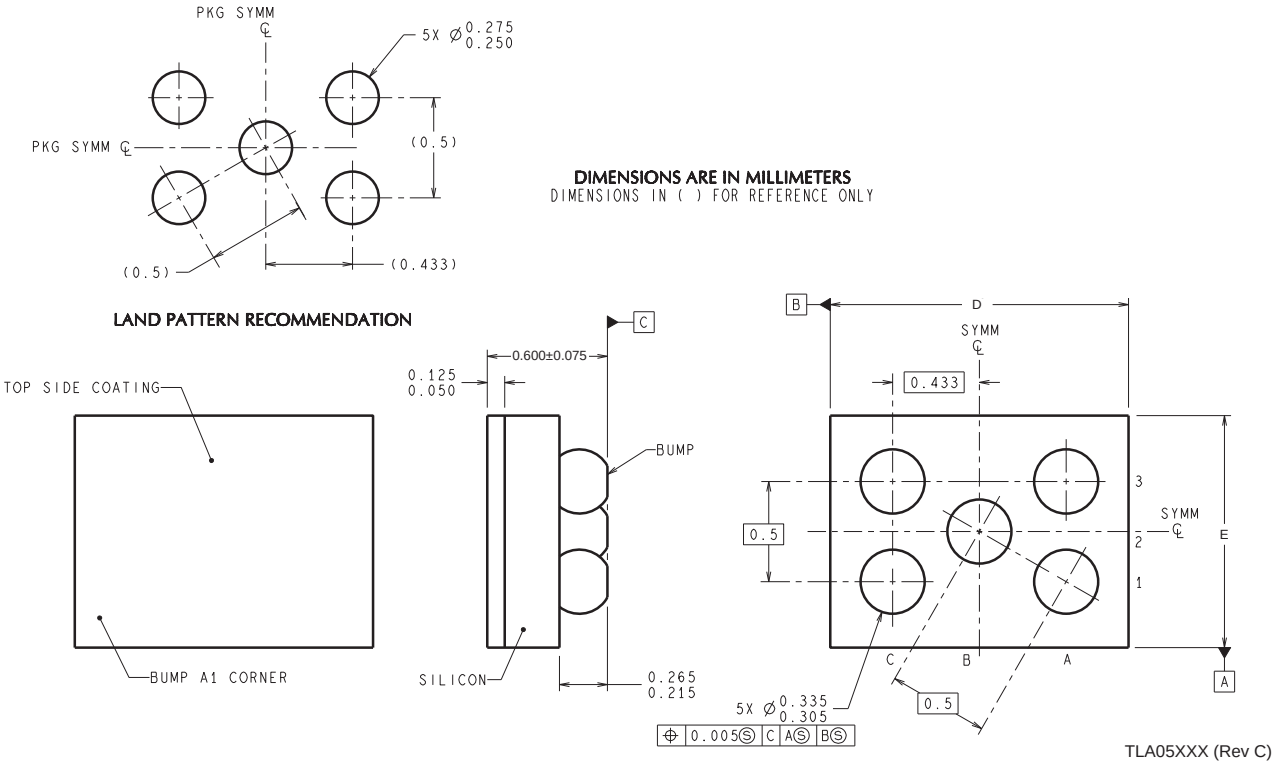






LCA06B (Rev A)

YZR0005



D: Max = 1.356 mm, Min =1.296 mm

E: Max = 0.99 mm, Min = 0.93 mm

4215043/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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