Advanced CMOS Logic – 54AC240

Octal 3-State Inverting Buffer / Line Driver / Line Receiver in bare die form

Rev 1.0
01/05/18

Description

The 54AC240 is produced on a 1.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power. The device can be used as two 4-bit buffers or one 8-bit buffer & features inverting inputs with two output enables, each controlling four of the 3-state outputs. The device is designed to improve performance & density in clock drivers, 3-state memory address drivers & bus orientated transmitters and receivers. Inputs accept standard CMOS outputs or LSTTL outputs using pull-up resistors. Inputs are also equipped with protection circuits against static discharge and transient excess voltage.

Features:

- Outputs Sink/Source 24mA
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 54LS240
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

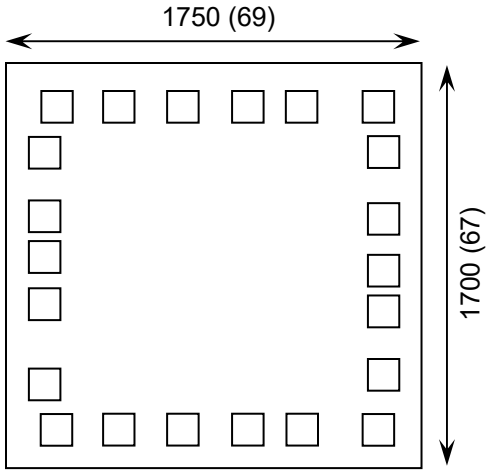
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

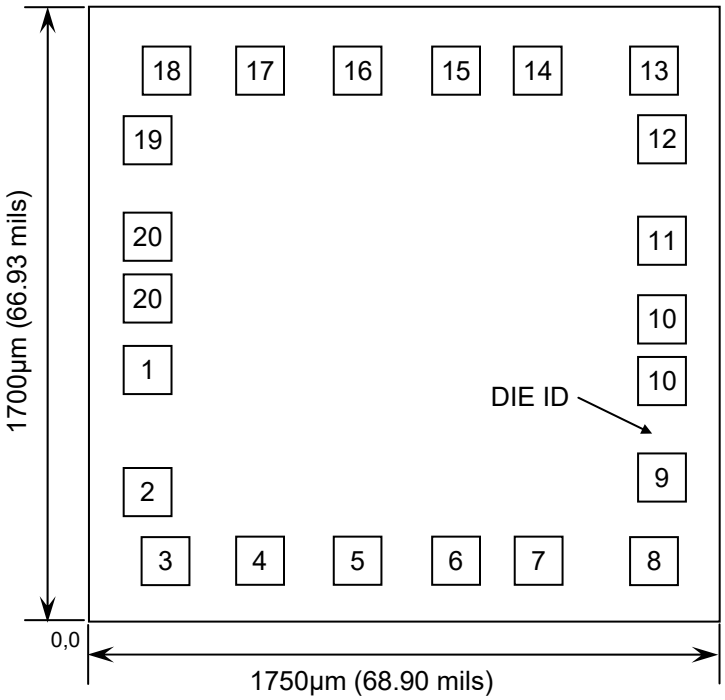
Mechanical Specification

Die Size (Unsawn)	1750 x 1700 69 x 67	µm mils
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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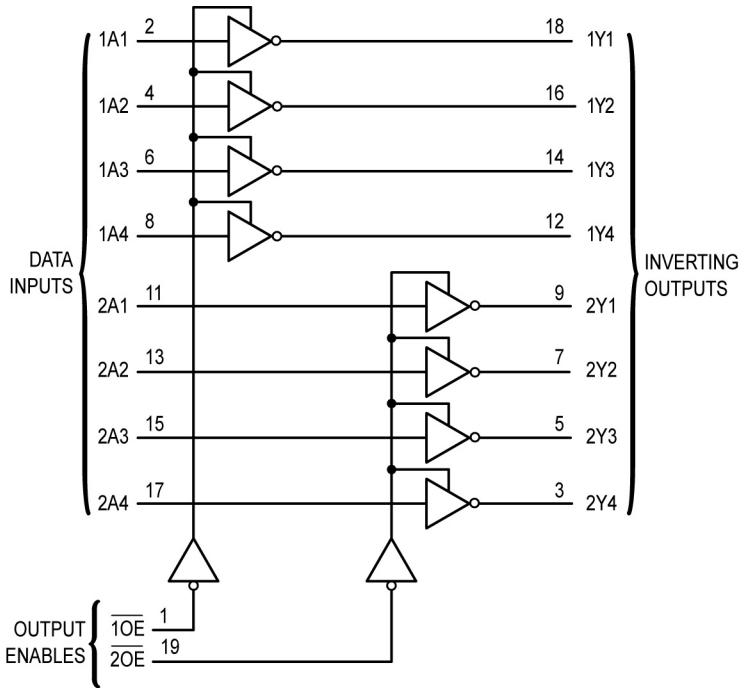
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Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{1OE}$	0.100	0.630
2	1A1	0.100	0.290
3	$\overline{2Y4}$	0.150	0.100
4	1A2	0.410	0.100
5	$\overline{2Y3}$	0.680	0.100
6	1A3	0.950	0.100
7	$\overline{2Y2}$	1.180	0.100
8	1A4	1.500	0.100
9	$\overline{2Y1}$	1.520	0.330
10	GND	1.520	0.600
10	GND	1.520	0.770
11	2A1	1.520	0.990
12	$\overline{1Y4}$	1.520	1.270
13	2A2	1.500	1.460
14	$\overline{1Y3}$	1.180	1.460
15	2A3	0.950	1.460
16	$\overline{1Y2}$	0.680	1.460
17	2A4	0.410	1.460
18	$\overline{1Y1}$	0.150	1.460
19	$\overline{2OE}$	0.100	1.270
20	V_{CC}	0.100	1.000
20	V_{CC}	0.100	0.830
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Truth Table

INPUTS		OUTPUTS
$\overline{1OE}$ $\overline{2OE}$	1A, 2A	1Y, 2Y
L L H	L H X	H L Z
H = High level (steady state) L = Low level (steady state) X = Don't care, Z = High impedance		

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Pad Descriptions

ADDRESS INPUTS
1A1, 1A2, 1A3, 1A4, 2A1, 2A2, 2A3, 2A4
(Pads 2, 4, 6, 8, 11, 13, 15, 17)
Data input pins. Data on these pins appear in non-inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROL INPUTS
$\overline{1OE}$, $\overline{2OE}$ (Pads 1, 19)
Output enables (active–low). When a low level is applied to these pins, the outputs are enabled and the devices function as non-inverting buffers. When a high level is applied, the outputs assume the high impedance state.

OUTPUTS
1Y1, 1Y2, 1Y3, 1Y4, 2Y1, 2Y2, 2Y3, 2Y4
(Pads 18, 16, 14, 12, 9, 7, 5, 3)
Device outputs. Depending upon the state of the output– enable pins, these outputs are either inverting outputs or high–impedance outputs.

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pin	I_{IN}	±20	mA
DC Output Current, per pin	I_{OUT}	±50	mA
DC V_{CC} or GND Current, per pin	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2	6	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-55	+125	°C
Output Current – High		I_{OH}	-	-24	mA
Output Current – Low		I_{OL}	-	24	mA
Input Rise and Fall Time (V_{IN} from 30% to 70%)	V_{CC} = 3.0V	t_r, t_f	0	150	ns/V
	V_{CC} = 4.5V		0	40	
	V_{CC} = 5.5V		0	24	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	3.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\| \le 20\mu A$	2.1	2.1	2.1	V
		4.5V		3.15	3.15	3.15	
		5.5V		3.85	3.85	3.85	
Maximum Low-Level Input Voltage	V_{IL}	3.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\| \le 20\mu A$	0.9	0.9	0.9	V
		4.5V		1.35	1.35	1.35	
		5.5V		1.65	1.65	1.65	
Minimum High-Level Output Voltage	V_{OH}	3.0V	I_{OUT} = -50μA	2.9	2.9	2.9	V
		4.5V		4.4	4.4	4.4	
		5.5V		5.4	5.4	5.4	
		3.0V	$V_{IN} = V_{IL}$ or V_{IH} I_{OH} = -12 mA	2.56	2.46	2.40	
		4.5V	$V_{IN} = V_{IL}$ or V_{IH} I_{OH} = -24mA[5]	3.86	3.76	3.70	
		5.5V	$V_{IN} = V_{IL}$ or V_{IH} I_{OH} = -24mA[5]	4.86	4.76	4.70	
		5.5V	$V_{IN} = V_{IL}$ or V_{IH} I_{OH} = -50mA[6]	-	-	3.85	
Maximum Low-Level Output Voltage	V_{OL}	3.0V	I_{OUT} = 50μA	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		5.5V		0.1	0.1	0.1	
		3.0V	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 12mA$	0.36	0.44	0.5	
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 24mA$[5]	0.36	0.44	0.5	
		5.5V	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 24mA$[5]	0.36	0.44	0.5	
		5.5V	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\|$ 50mA[6]	-	-	1.65	
Maximum Input Leakage Current	I_{IN}	5.5V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	5.5V	$V_{OUT}=V_{CC}$ or GND $V_{IN} = V_{IL}$ or V_{IH}	±0.5	±2.5	±5	μA
Minimum Dynamic Output Current[7]	I_{OLD}	5.5V	V_{OLD} = 1.65V Max	-	75	50	mA
	I_{OHD}	5.5V	V_{OHD} = 3.85V Min	-	-75	-50	
Maximum Quiescent Supply Current	I_{CC}	5.5V	$V_{IN} = V_{CC}$ or GND I_{OUT} = 0μA	8	80	160	μA

4. -55˚C ≤ T_J ≤ +125˚C **5.** All outputs loaded; thresholds on input associated with output under test. **6.** Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 125°C **7.** Maximum test duration 2ms, one output loaded at a time

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AC Electrical Characteristics[8] (V_{CC} 3.3V ±0.3V, V_{CC} 5V ±0.3V)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay 1A to 1Y or 2A to 2Y (Figure 1,3)	t_{PLH},	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	8.0	9.0	11.0	ns
		5.0V		6.5	7.0	8.5	
	t_{PHL}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	8.0	8.5	10.5	ns
		5.0V		6.0	6.5	8.0	
Output Enable Time OE to 1Y or 2Y (Figure 2,4)	t_{PZH},	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	10.5	11.0	11.5	ns
		5.0V		7.0	8.0	9.0	
	t_{PZL}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	10.0	11.0	13.0	ns
		5.0V		8.0	8.5	10.5	
Output Enable Time OE to 1Y or 2Y (Figure 2,4)	t_{PHZ}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	10	10.5	12.5	ns
		5.0V		9.0	9.5	10.5	
	t_{PLZ}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	10.5	11.5	13.5	ns
		5.0V		9.0	9.5	11.0	
Maximum Input Capacitance	C_{IN}	-	-	4.5	4.5	4.5	pF
Power Dissipation Capacitance[9]	C_{PD}	-	T_J = 25°C, V_{CC} = 5.0V	TYPICAL			
				45			pF

8. Not production tested in die form, characterized by chip design

9. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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Switching Waveforms

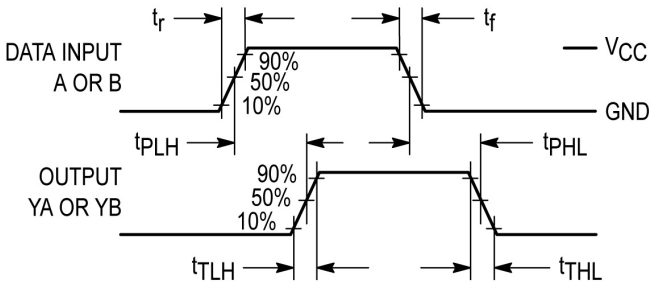


Figure 1 – Propagation Delay
Input A or B to Output YA or YB

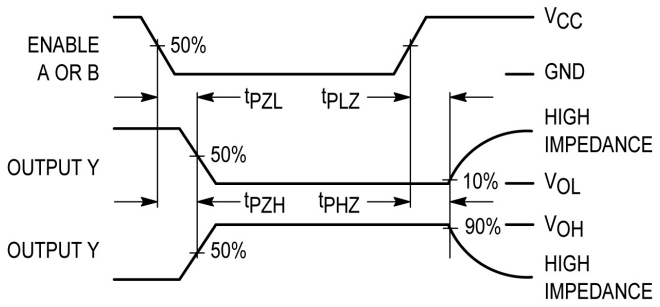
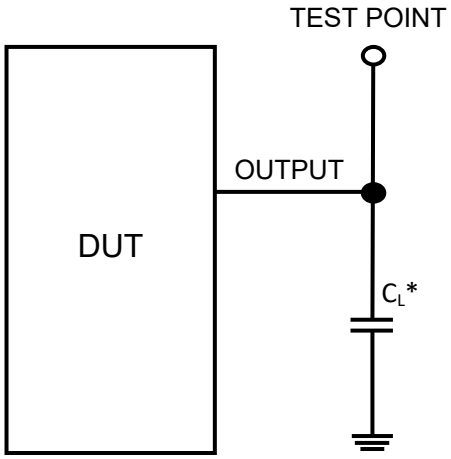


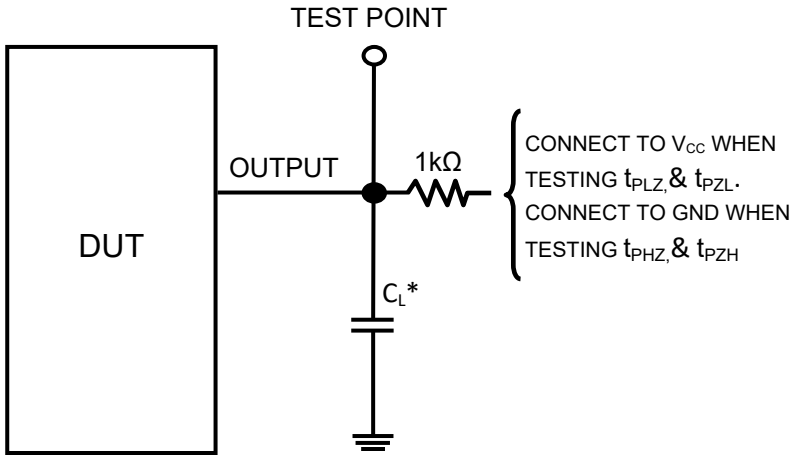
Figure 2 – Propagation Delay
Output Enable to Output YA or YB

Test Circuits



* Includes all probe and jig capacitance

Figure 3



* Includes all probe and jig capacitance

Figure 4

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