RX660 Group
Renesas MCUs

R01DS0393EJ0100
Rev.1.00
Mar 18, 2022

120-MHz 32-bit RX MCU, on-chip FPU, 709 CoreMark, Supportive of 5V power supply, up to 1-MB flash memory, up to 128-KB SRAM, 32-KB data flash memory, various communications interfaces, including CAN FD, 12-bit A/D converter, 12-bit D/A converter, Analog comparator, RTC, Remote control signal receiver

Features

■ 32-bit RXv3 CPU core
- Maximum operating frequency: 120 MHz
  Capable of 709 CoreMark in operation at 120 MHz
- A collective register bank save function is available.
- Supports the memory protection unit (MPU)
- JTAG and FINE (one-line) debugging interfaces

■ Low-power design and architecture
- Operation from a single 2.7- to 5.5-V supply
- Deep software standby mode with the RTC continuing to run
- Four low-power modes

■ On-chip code flash memory
- Supports versions with up to 1 Mbyte of ROM
- No waiting for access in 120-MHz operation
- User code is programmable by on-board or off-board programming.
- Programming/erasing as background operations (BGOs)

■ On-chip data flash memory
- 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM
- 128 Kbytes of SRAM (no wait states)

■ External address space
- Buses for full-speed data transfer (maximum operating frequency of 40 MHz)
- Four CS areas
- 8- or 16-bit bus space is selectable per area

■ Data transfer
- DMACAa: 8 channels
- DTCb: 1 channel

■ ELC
- Module operation can be initiated by event signals without using interrupts
- Linked operation between modules is possible when the CPU is in sleep mode

■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD)

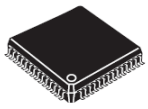
■ Clock functions
- The main clock oscillator is connectable to an 8- to 24-MHz external crystal resonator and usable as the PLL reference clock.
- A sub-clock oscillator connectable to a 32.768-kHz crystal resonator
- Internal 240-kHz LOCO and HOCO selectable from 16, 18, and 20 MHz
- 120-kHz clock for the IWDTa

■ Real-time clock
- Adjustment functions (30 seconds, leap year, and error)
- Real-time clock counting and binary counting modes are selectable
- Time capture in response to an event-signal input

■ Independent watchdog timer
- 120-kHz IWDT-dedicated on-chip oscillator clock operation

■ Useful functions for IEC60730 compliance
- Oscillation-stoppage detection, functions for self-diagnosis and detection of disconnection for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test-assisting function by DOC, and CRCA, etc.
- Register write protection function that protects important registers against overwriting

■ Remote control signal receiver



PLQP0144KA-B 20 × 20 mm, 0.5 mm pitch
PLQP0100KB-B 14 × 14 mm, 0.5 mm pitch
PLQP0080KB-B 12 × 12 mm, 0.5 mm pitch
PLQP0064KB-C 10 × 10 mm, 0.5 mm pitch
PLQP0048KB-B 7 × 7 mm, 0.5 mm pitch

■ Various communications interfaces
- CAN FD: Compliant with ISO 11898-1:2015, standard frame and extended frame (1 channel)
- SCIk, SCIm, and SCIh with multiple functionalities (up to 13 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I^2C, and extended serial mode.
- SCIm with 16-byte transmission and reception FIFOs (up to 2 channels)
- The I^2C bus interfaces (RIICa) for transfer at up to 400 kbps (fast mode), capable of SMBus operation (2 channels)
- RSPId (1 channel) for transfer at up to 30 Mbps

■ Up to 19 extended-function timers
- 16-bit MTU3a
- 8-bit TMRb (4 channels), 16-bit CMT (4 channels), 32-bit CMTW (2 channels)

■ 12-bit A/D converter
- Single 12-bit unit (24 channels)
- Self diagnosis, detection of analog input disconnection

■ Analog Comparator (CMPC): 4 channels

■ 12-bit D/A converter (R12DAb): 2 channels
- Usable as a reference voltage for the analog comparator

■ Temperature sensor for measuring temperature within the chip

■ Up to 134 pins for general I/O ports
- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating temp. range
- D-version: –40°C to +85°C
- G-version: –40°C to +105°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 give a comparison of the functions of products in different packages.
Table 1.1 is an outline of maximum specifications, and the peripheral modules and the number of channels of the modules differ depending on the number of pins on the package. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/8)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • 113 instructions Instructions installed as standard: 111 Basic instructions: 77 Single-precision floating-point operation instructions: 11 DSP instructions: 23 Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
	Register bank save function	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks
Memory	Code flash memory	• Capacity: 1 Mbyte/512 Kbytes • 120 MHz, no-wait access • On-board programming: Four types • Off-board programming (parallel programmer mode) • Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized.
	Data flash memory	• Capacity: 32 Kbytes • Programming/erasing: 100,000 times
	Unique ID	• 12-byte unique ID for the device
	RAM	• Capacity: 128 Kbytes • 120 MHz, no-wait access
Operating modes		• Operating modes by the mode-setting pins at the time of release from the reset state Single-chip mode Boot mode (for the SCI interface) Boot mode (for the FINE interface) User boot mode • Selection of operating mode by register setting Single-chip mode User boot mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode • Endian selectable

Table 1.1 Outline of Specifications (2/8)

Classification	Module/Function	Description
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 120 MHz The following peripheral modules run in synchronization with PCLKA, which runs at up to 120 MHz: MTU, RSPI, SCIs (SCI10 and SCI11), RSCI, and the ECC function control registers in the CAN FD module. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz ADCLK in the S12AD runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 40 MHz • Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit
Reset		Nine types of reset • RES# pin reset: Generated when the RES# pin is driven low. • Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 rises. • Voltage-monitoring 0 reset: Generated when VCC = AVCC0 falls. • Voltage-monitoring 1 reset: Generated when VCC = AVCC0 falls. • Voltage-monitoring 2 reset: Generated when VCC = AVCC0 falls. • Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. • Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. • Software reset: Generated by register setting.
Power-on reset		If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC pins and generates an internal reset or internal interrupt in response to the voltage reaching a threshold. • Voltage detection circuit 0 Capable of generating an internal reset The option-setting memory can be used to select enabling or disabling of the reset. Voltage detection level: Selectable from two different levels • Voltage detection circuits 1 and 2 Voltage detection level: Selectable from five different levels Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) Capable of generating an internal reset • Two types of timing are selectable for release from reset An internal interrupt can be requested. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable Voltage detection monitoring Event linking
Low power consumption	Low power consumption function	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
Interrupt	Interrupt controller (ICUF)	• Peripheral function interrupts: 256 sources • External interrupts: 16 (pins IRQ0 to IRQ15) • Software interrupts: 2 sources • Non-maskable interrupts: 7 sources • Sixteen levels specifiable for the order of priority • Method of interrupt source selection: The interrupt vectors consist of 256 vectors (128 sources are fixed. The remaining 133 vectors are selected from among the other 128 sources.)

Table 1.1 Outline of Specifications (3/8)

Classification	Module/Function	Description
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 2 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8-, or 16-bit bus space. The data arrangement in each area is selectable as little or big endian (only for data). • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACAa)	• 8 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCb)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: External interrupts and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	• I/O ports for the 144-pin LFQFP with no JTAG interface and no sub-clock oscillator I/O pins: 133 Input pin: 1 Pull-up resistors: 133 Open-drain outputs: 133 5-V tolerance: 4 • I/O ports for the 144-pin LFQFP with a sub-clock oscillator, but no JTAG interface I/O pins: 131 Input pin: 1 Pull-up resistors: 131 Open-drain outputs: 131 5-V tolerance: 4 • I/O ports for the 144-pin LFQFP with a JTAG interface, but no sub-clock oscillator I/O pins: 132 Input pin: 1 Pull-up resistors: 132 Open-drain outputs: 132 5-V tolerance: 4 • I/O ports for the 144-pin LFQFP with a JTAG interface and a sub-clock oscillator I/O pins: 130 Input pin: 1 Pull-up resistors: 130 Open-drain outputs: 130 5-V tolerance: 4 • I/O ports for the 100-pin LFQFP with no JTAG interface and no sub-clock oscillator I/O pins: 91 Input pin: 1 Pull-up resistors: 91 Open-drain outputs: 91 5-V tolerance: 4 • I/O ports for the 100-pin LFQFP with a sub-clock oscillator, but no JTAG interface I/O pins: 89 Input pin: 1 Pull-up resistors: 89 Open-drain outputs: 89 5-V tolerance: 4 • I/O ports for the 100-pin LFQFP with a JTAG interface, but no sub-clock oscillator I/O pins: 90 Input pin: 1 Pull-up resistors: 90 Open-drain outputs: 90 5-V tolerance: 4

Table 1.1 Outline of Specifications (4/8)

Classification	Module/Function	Description
I/O ports	Programmable I/O ports	• I/O ports for the 100-pin LFQFP with a JTAG interface and a sub-clock oscillator I/O pins: 88 Input pin: 1 Pull-up resistors: 88 Open-drain outputs: 88 5-V tolerance: 4 • I/O ports for the 80-pin LFQFP with no sub-clock oscillator I/O pins: 71 Input pin: 1 Pull-up resistors: 71 Open-drain outputs: 71 5-V tolerance: 4 • I/O ports for the 80-pin LFQFP with a sub-clock oscillator I/O pins: 69 Input pin: 1 Pull-up resistors: 69 Open-drain outputs: 69 5-V tolerance: 4 • I/O ports for the 64-pin LFQFP with no sub-clock oscillator I/O pins: 55 Input pin: 1 Pull-up resistors: 55 Open-drain outputs: 55 5-V tolerance: 2 • I/O ports for the 64-pin LFQFP with a sub-clock oscillator I/O pins: 53 Input pin: 1 Pull-up resistors: 53 Open-drain outputs: 53 5-V tolerance: 2 • I/O ports for the 48-pin LFQFP I/O pins: 39 Input pin: 1 Pull-up resistors: 39 Open-drain outputs: 39 5-V tolerance: 2
Event link controller (ELC)		• Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions. • 83 internal event signals can be freely combined for interlinked operation with connected functions. • Event signals from peripheral modules can be used to change the states of output pins (of ports B and E). • Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules.
Timers	8-bit timers (TMRb)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Capable of generating operating clock for the remote control signal receiver (REMC) • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events.

Table 1.1 Outline of Specifications (5/8)

Classification	Module/Function	Description
Timers	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC
	Multifunction timer pulse unit (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 14 counter-input clock signals for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLK/A32, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) 14 of the signals are available for channel 0, 11 are available for channels 1, 3, 4, 6 to 8, 12 are available for channel 2, and 10 are available for channel 5. • Input capture function • 39 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • 43 interrupt sources • Automatic transfer of register data • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffer configuration • Reset synchronous PWM mode Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion • A/D converter start triggers can be skipped • Digital filter function for signals on the input capture and external counter clock pins • Event linking by the ELC
	Port output enable 3 (POE3a)	• Control of the high-impedance state of the MTU waveform output pins • 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11# • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by oscillation-stoppage detection or software • Additional programming of output control target pins is enabled
	Realtime clock (RTCC)*1	• Clock sources: Sub clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Time capture function (up to 3 pins) • Event linking by the ELC

Table 1.1 Outline of Specifications (6/8)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIk, SCIm, SCIh)	• 13 channels (SCIk: 10 channels + SCIh: 1 channel + SCIm: 2 channels) • SCIk, SCIh, SCIm Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation Double-speed mode • SCIk, SCIh Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Event linking by the ELC (only on channel 5) • SCIh Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format • SCIm Data can be transmitted or received in sequence by the 16-byte FIFO buffers of the transmission and reception unit • SCIk, SCIm Data match detection Adjustment of the timing of sampling of the RXD signals
	Serial communications interfaces (RSCI)	• 2 channels (RSCI10, RSCI11) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multi-processor function • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Start-bit detection: Level or edge detection is selectable. • Simple I^2C • Simple SPI • 9-bit transfer mode • Bit rate modulation • Double-speed mode • Supports the serial communications protocol, which contains the start frame and information frame • Supports the LIN format • Data can be transmitted or received in sequence by the 32-byte FIFO buffers of the transmission and reception unit • Manchester encoding is supported. • RSCI has some home bus system (HBS) functionality. • Data match detection • Adjustment of the timing of sampling of the RXD signals
	I^2C bus interface (RIICa)	• 2 channels Communication formats I^2C bus format/SMBus format Supports the multi-master • Event linking by the ELC
	CAN FD module (CANFD)*2	• 1 channel • Compliance with the ISO11898-1:2015 specification (standard frame and extended frame)

Table 1.1 Outline of Specifications (7/8)

Classification	Module/Function	Description
Communication function	Serial peripheral interface (RSPId)	• 1 channel • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Transmit/receive data can be swapped in byte units • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC
	Remote control signal receiver (REMCa)	• 1 channel • Four pattern matching (header, data 0, data 1, and special data detection) • 8-byte receive buffer per unit • The operating clock can be selected from among the PCLK, sub-clock, and TMR.
12-bit A/D converter (S12ADH)		• 12 bits (24 channels × 1 unit) • 12-bit resolution • Minimum conversion time 0.9 µs per channel (when ADCLK operates at 60 MHz) • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group A priority control (only for 3 group scan mode) • Sampling variable Sampling time can be set up for each channel. • Conversion function in order of arbitrarily selected channels (Serial conversion of the same channel cannot be allowed) • Double trigger mode (A/D conversion data duplicated) • Three ways to start A/D conversion Software trigger, synchronous trigger (MTU, TMR, ELC), external trigger • Prioritization in group scanning can be controlled among group A, B, and C. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function • Detection of analog input disconnection • Event linking by the ELC
12-bit D/A converter (R12DAb)		• 2 channels • 12-bit resolution • Output voltage: 0 V to AVCC0 • Capable of providing as a reference voltage for comparator • Event linking by the ELC
Comparator C (CMPC)		• 4 channels • Function to compare the reference voltage and the analog input voltage • Digital filtering
Temperature sensor		• 1 channel • Relative precision: ± 1.0°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter.
Arithmetic unit for trigonometric functions (TFU)		• Sine, cosine, arctangent, $\sqrt{x^2 + y^2}$ Simultaneous calculation of sine and cosine Simultaneous calculation of arctangent and $\sqrt{x^2 + y^2}$

Table 1.1 Outline of Specifications (8/8)

Classification	Module/Function	Description
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An access exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	• Programs in the TM target area in the code flash memory are protected against reading • Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRCA)	• Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop detection	• Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, IWDT-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOCA)	• This handles the comparison, addition, subtraction, comparison in terms of which is larger or smaller, or window comparison of 32-bit values.
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = 2.7 to 5.5V AVCC0 = 3.0 to 5.5V (VCC ≤ AVCC0)
Operating temperature		D-version: –40 to +85°C G-version: –40 to +105°C
Package		144-pin LFQFP (PLQP0144KA-B) 100-pin LFQFP (PLQP0100KB-B) 80-pin LFQFP (PLQP0080KB-B) 64-pin LFQFP (PLQP0064KB-C) 48-pin LFQFP (PLQP0048KB-B)
Debugging interface		JTAG*3 and FINE interfaces

Note 1. When the realtime clock is not used, initialize the registers in the realtime clock according to description in section 27.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in the User's Manual: Hardware. The realtime clock cannot be used in products with no sub-clock oscillator. At this time, disable the realtime clock according to description in section 27.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in the User's Manual: Hardware.

Note 2. The product part number differs according to whether or not the CANFD actually supports the CAN FD protocol.

Note 3. The product part number differs according to whether or not the MCU includes a JTAG interface.

Table 1.2 Comparison of Functions for Different Packages

Functions			Products / Package	RX660 144-pin LFQFP	RX660 100-pin LFQFP	RX660 80-pin LFQFP	RX660 64-pin LFQFP	RX660 48-pin LFQFP
Code Flash Memory Capacity				1 Mbyte/512 Kbytes				
Data Flash Memory Capacity				32 Kbytes				
RAM				128 Kbytes				
External bus	External bus width			16 bits		Not available		
	Address Space			2 Mbytes × 4 areas		Not available		
DMA	DMA controller			Available				
	Data transfer controller			Available				
Oscillator	Main clock oscillator (MOSC)			Available				
	Sub-clock oscillator (SOSC)			Available/Not available				Not available
Timers	Multi-function timer pulse unit 3			Ch. 0 to 8		Ch. 0 to 7		Ch. 0 to 5, and 7
	Port output enable 3			Available				
	8-bit timers			Ch. 0 to 3				Ch. 0 to 2
	Compare match timer			Ch. 0 to 3				
	Compare match timer W			Ch. 0 and 1				
	Realtime clock			Available/Not available*1				Not available*1
	Watchdog timer			Available				
	Independent watchdog timer			Available				
Communication function	Serial communications interfaces (SCIk)			Ch. 0 to 9	Ch. 0 to 6, 8, and 9	Ch. 0, 1, 3 to 6, 8, and 9	Ch. 1, 3 to 6, 8, and 9	Ch. 1, 3 to 6, and 8
	Serial communications interfaces (SCIm)			Ch. 10 and 11				Ch. 10
	Serial communications interfaces (SCIh)			Ch. 12				
	Serial communications interfaces (RSCI)			Ch. 10 and 11				Ch. 10
	I²C bus interfaces (RIIC)			Ch. 0 to 2			Ch. 2	
	Serial peripheral interface (RSPI)			1 channel				
	CAN FD module (CANFD)			1 channel				
	Remote control signal receiver (REMC)			Ch. 0				
Analog	12-bit A/D converter			24 channels		17 channels	14 channels	10 channels
	Comparator C			4 channels				
	12-bit D/A converter*2	Number of channels		2 channels				
		Number of output pins		2 pins	2 pins/1 pin*3	2 pins	1 pin	Not available
	Temperature sensor			Available				
CRC calculator (CRCA)				Available				
Data operation circuit (DOCA)				Available				
Clock frequency accuracy measurement circuit (CAC)				Available				
Event link controller (ELC)				Available				
Off-board programming				Available		Not available		
Debugging interfaces	JTAG interface			Available/Not available		Not available		
	FINE interface			Available				

Note 1. The realtime clock cannot be used in products with no sub-clock oscillator. Disable the realtime clock according to description in section 27.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in the User's Manual: Hardware.
Note 2. The 2-channel analog output of the D/A converters can be used as the input of the comparators in all packages.
Note 3. Products with a JTAG interface that are also in the 100-pin LFQFP have a single D/A converter channel.

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/3)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	JTAG	Sub-clock oscillator	CANFD	Operating temperature (°C)
RX660 (D-version)	R5F56609ADFB	PLQP0144KA-B	1 M	128 K	32 K	Not available	Not available	Available*1	–40 to +85
	R5F56609BDFB	PLQP0144KA-B	1 M	128 K	32 K	Not available	Not available	Available	–40 to +85
	R5F56609CDFB	PLQP0144KA-B	1 M	128 K	32 K	Not available	Available	Available*1	–40 to +85
	R5F56609DDFB	PLQP0144KA-B	1 M	128 K	32 K	Not available	Available	Available	–40 to +85
	R5F56609EDFB	PLQP0144KA-B	1 M	128 K	32 K	Available	Not available	Available*1	–40 to +85
	R5F56609FDFB	PLQP0144KA-B	1 M	128 K	32 K	Available	Not available	Available	–40 to +85
	R5F56609GDFB	PLQP0144KA-B	1 M	128 K	32 K	Available	Available	Available*1	–40 to +85
	R5F56609HDFB	PLQP0144KA-B	1 M	128 K	32 K	Available	Available	Available	–40 to +85
	R5F56609ADFP	PLQP0100KB-B	1 M	128 K	32 K	Not available	Not available	Available*1	–40 to +85
	R5F56609BDFP	PLQP0100KB-B	1 M	128 K	32 K	Not available	Not available	Available	–40 to +85
	R5F56609CDFP	PLQP0100KB-B	1 M	128 K	32 K	Not available	Available	Available*1	–40 to +85
	R5F56609DDFP	PLQP0100KB-B	1 M	128 K	32 K	Not available	Available	Available	–40 to +85
	R5F56609EDFP	PLQP0100KB-B	1 M	128 K	32 K	Available	Not available	Available*1	–40 to +85
	R5F56609FDFP	PLQP0100KB-B	1 M	128 K	32 K	Available	Not available	Available	–40 to +85
	R5F56609GDFP	PLQP0100KB-B	1 M	128 K	32 K	Available	Available	Available*1	–40 to +85
	R5F56609HDFP	PLQP0100KB-B	1 M	128 K	32 K	Available	Available	Available	–40 to +85
	R5F56609ADFN	PLQP0080KB-B	1 M	128 K	32 K	Not available	Not available	Available*1	–40 to +85
	R5F56609BDFN	PLQP0080KB-B	1 M	128 K	32 K	Not available	Not available	Available	–40 to +85
	R5F56609CDFN	PLQP0080KB-B	1 M	128 K	32 K	Not available	Available	Available*1	–40 to +85
	R5F56609DDFN	PLQP0080KB-B	1 M	128 K	32 K	Not available	Available	Available	–40 to +85
	R5F56609ADFM	PLQP0064KB-C	1 M	128 K	32 K	Not available	Not available	Available*1	–40 to +85
	R5F56609BDFM	PLQP0064KB-C	1 M	128 K	32 K	Not available	Not available	Available	–40 to +85
	R5F56609CDFM	PLQP0064KB-C	1 M	128 K	32 K	Not available	Available	Available*1	–40 to +85
	R5F56609DDFM	PLQP0064KB-C	1 M	128 K	32 K	Not available	Available	Available	–40 to +85
	R5F56609ADFL	PLQP0048KB-B	1 M	128 K	32 K	Not available	Not available	Available*1	–40 to +85
	R5F56609BDFL	PLQP0048KB-B	1 M	128 K	32 K	Not available	Not available	Available	–40 to +85
	R5F56604ADFB	PLQP0144KA-B	512 K	128 K	32 K	Not available	Not available	Available*1	–40 to +85
	R5F56604BDFB	PLQP0144KA-B	512 K	128 K	32 K	Not available	Not available	Available	–40 to +85
	R5F56604CDFB	PLQP0144KA-B	512 K	128 K	32 K	Not available	Available	Available*1	–40 to +85
	R5F56604DDFB	PLQP0144KA-B	512 K	128 K	32 K	Not available	Available	Available	–40 to +85
	R5F56604EDFB	PLQP0144KA-B	512 K	128 K	32 K	Available	Not available	Available*1	–40 to +85
	R5F56604FDFB	PLQP0144KA-B	512 K	128 K	32 K	Available	Not available	Available	–40 to +85
	R5F56604GDFB	PLQP0144KA-B	512 K	128 K	32 K	Available	Available	Available*1	–40 to +85
	R5F56604HDFB	PLQP0144KA-B	512 K	128 K	32 K	Available	Available	Available	–40 to +85
	R5F56604ADFP	PLQP0100KB-B	512 K	128 K	32 K	Not available	Not available	Available*1	–40 to +85
	R5F56604BDFP	PLQP0100KB-B	512 K	128 K	32 K	Not available	Not available	Available	–40 to +85
	R5F56604CDFP	PLQP0100KB-B	512 K	128 K	32 K	Not available	Available	Available*1	–40 to +85
	R5F56604DDFP	PLQP0100KB-B	512 K	128 K	32 K	Not available	Available	Available	–40 to +85

Table 1.3 List of Products (2/3)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	JTAG	Sub-clock oscillator	CANFD	Operating temperature (°C)
RX660 (D-version)	R5F56604EDFP	PLQP0100KB-B	512 K	128 K	32 K	Available	Not available	Available*1	–40 to +85
	R5F56604FDFP	PLQP0100KB-B	512 K	128 K	32 K	Available	Not available	Available	–40 to +85
	R5F56604GDFP	PLQP0100KB-B	512 K	128 K	32 K	Available	Available	Available*1	–40 to +85
	R5F56604HDFP	PLQP0100KB-B	512 K	128 K	32 K	Available	Available	Available	–40 to +85
	R5F56604ADFN	PLQP0080KB-B	512 K	128 K	32 K	Not available	Not available	Available*1	–40 to +85
	R5F56604BDFN	PLQP0080KB-B	512 K	128 K	32 K	Not available	Not available	Available	–40 to +85
	R5F56604CDFN	PLQP0080KB-B	512 K	128 K	32 K	Not available	Available	Available*1	–40 to +85
	R5F56604DDFN	PLQP0080KB-B	512 K	128 K	32 K	Not available	Available	Available	–40 to +85
	R5F56604ADFM	PLQP0064KB-C	512 K	128 K	32 K	Not available	Not available	Available*1	–40 to +85
	R5F56604BDFM	PLQP0064KB-C	512 K	128 K	32 K	Not available	Not available	Available	–40 to +85
	R5F56604CDFM	PLQP0064KB-C	512 K	128 K	32 K	Not available	Available	Available*1	–40 to +85
	R5F56604DDFM	PLQP0064KB-C	512 K	128 K	32 K	Not available	Available	Available	–40 to +85
	R5F56604ADFL	PLQP0048KB-B	512 K	128 K	32 K	Not available	Not available	Available*1	–40 to +85
	R5F56604BDFL	PLQP0048KB-B	512 K	128 K	32 K	Not available	Not available	Available	–40 to +85
RX660 (G-version)	R5F56609AGFB	PLQP0144KA-B	1 M	128 K	32 K	Not available	Not available	Available*1	–40 to +105
	R5F56609BGFB	PLQP0144KA-B	1 M	128 K	32 K	Not available	Not available	Available	–40 to +105
	R5F56609CGFB	PLQP0144KA-B	1 M	128 K	32 K	Not available	Available	Available*1	–40 to +105
	R5F56609DGFB	PLQP0144KA-B	1 M	128 K	32 K	Not available	Available	Available	–40 to +105
	R5F56609EGFB	PLQP0144KA-B	1 M	128 K	32 K	Available	Not available	Available*1	–40 to +105
	R5F56609FGFB	PLQP0144KA-B	1 M	128 K	32 K	Available	Not available	Available	–40 to +105
	R5F56609GGFB	PLQP0144KA-B	1 M	128 K	32 K	Available	Available	Available*1	–40 to +105
	R5F56609HGFB	PLQP0144KA-B	1 M	128 K	32 K	Available	Available	Available	–40 to +105
	R5F56609AGFP	PLQP0100KB-B	1 M	128 K	32 K	Not available	Not available	Available*1	–40 to +105
	R5F56609BGFP	PLQP0100KB-B	1 M	128 K	32 K	Not available	Not available	Available	–40 to +105
	R5F56609CGFP	PLQP0100KB-B	1 M	128 K	32 K	Not available	Available	Available*1	–40 to +105
	R5F56609DGFP	PLQP0100KB-B	1 M	128 K	32 K	Not available	Available	Available	–40 to +105
	R5F56609EGFP	PLQP0100KB-B	1 M	128 K	32 K	Available	Not available	Available*1	–40 to +105
	R5F56609FGFP	PLQP0100KB-B	1 M	128 K	32 K	Available	Not available	Available	–40 to +105
	R5F56609GGFP	PLQP0100KB-B	1 M	128 K	32 K	Available	Available	Available*1	–40 to +105
	R5F56609HGFP	PLQP0100KB-B	1 M	128 K	32 K	Available	Available	Available	–40 to +105
	R5F56609AGFN	PLQP0080KB-B	1 M	128 K	32 K	Not available	Not available	Available*1	–40 to +105
	R5F56609BGFN	PLQP0080KB-B	1 M	128 K	32 K	Not available	Not available	Available	–40 to +105
	R5F56609CGFN	PLQP0080KB-B	1 M	128 K	32 K	Not available	Available	Available*1	–40 to +105
	R5F56609DGFN	PLQP0080KB-B	1 M	128 K	32 K	Not available	Available	Available	–40 to +105
	R5F56609AGFM	PLQP0064KB-C	1 M	128 K	32 K	Not available	Not available	Available*1	–40 to +105
	R5F56609BGFM	PLQP0064KB-C	1 M	128 K	32 K	Not available	Not available	Available	–40 to +105
	R5F56609CGFM	PLQP0064KB-C	1 M	128 K	32 K	Not available	Available	Available*1	–40 to +105
	R5F56609DGFM	PLQP0064KB-C	1 M	128 K	32 K	Not available	Available	Available	–40 to +105
	R5F56609AGFL	PLQP0048KB-B	1 M	128 K	32 K	Not available	Not available	Available*1	–40 to +105
	R5F56609BGFL	PLQP0048KB-B	1 M	128 K	32 K	Not available	Not available	Available	–40 to +105

Table 1.3 List of Products (3/3)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	JTAG	Sub-clock oscillator	CANFD	Operating temperature (°C)
RX660 (G-version)	R5F56604AGFB	PLQP0144KA-B	512 K	128 K	32 K	Not available	Not available	Available*1	–40 to +105
	R5F56604BGFB	PLQP0144KA-B	512 K	128 K	32 K	Not available	Not available	Available	–40 to +105
	R5F56604CGFB	PLQP0144KA-B	512 K	128 K	32 K	Not available	Available	Available*1	–40 to +105
	R5F56604DGFB	PLQP0144KA-B	512 K	128 K	32 K	Not available	Available	Available	–40 to +105
	R5F56604EGFB	PLQP0144KA-B	512 K	128 K	32 K	Available	Not available	Available*1	–40 to +105
	R5F56604FGFB	PLQP0144KA-B	512 K	128 K	32 K	Available	Not available	Available	–40 to +105
	R5F56604GGFB	PLQP0144KA-B	512 K	128 K	32 K	Available	Available	Available*1	–40 to +105
	R5F56604HGFB	PLQP0144KA-B	512 K	128 K	32 K	Available	Available	Available	–40 to +105
	R5F56604AGFP	PLQP0100KB-B	512 K	128 K	32 K	Not available	Not available	Available*1	–40 to +105
	R5F56604BGFP	PLQP0100KB-B	512 K	128 K	32 K	Not available	Not available	Available	–40 to +105
	R5F56604CGFP	PLQP0100KB-B	512 K	128 K	32 K	Not available	Available	Available*1	–40 to +105
	R5F56604DGFP	PLQP0100KB-B	512 K	128 K	32 K	Not available	Available	Available	–40 to +105
	R5F56604EGFP	PLQP0100KB-B	512 K	128 K	32 K	Available	Not available	Available*1	–40 to +105
	R5F56604FGFP	PLQP0100KB-B	512 K	128 K	32 K	Available	Not available	Available	–40 to +105
	R5F56604GGFP	PLQP0100KB-B	512 K	128 K	32 K	Available	Available	Available*1	–40 to +105
	R5F56604HGFP	PLQP0100KB-B	512 K	128 K	32 K	Available	Available	Available	–40 to +105
	R5F56604AGFN	PLQP0080KB-B	512 K	128 K	32 K	Not available	Not available	Available*1	–40 to +105
	R5F56604BGFN	PLQP0080KB-B	512 K	128 K	32 K	Not available	Not available	Available	–40 to +105
	R5F56604CGFN	PLQP0080KB-B	512 K	128 K	32 K	Not available	Available	Available*1	–40 to +105
	R5F56604DGFN	PLQP0080KB-B	512 K	128 K	32 K	Not available	Available	Available	–40 to +105
	R5F56604AGFM	PLQP0064KB-C	512 K	128 K	32 K	Not available	Not available	Available*1	–40 to +105
	R5F56604BGFM	PLQP0064KB-C	512 K	128 K	32 K	Not available	Not available	Available	–40 to +105
	R5F56604CGFM	PLQP0064KB-C	512 K	128 K	32 K	Not available	Available	Available*1	–40 to +105
	R5F56604DGFM	PLQP0064KB-C	512 K	128 K	32 K	Not available	Available	Available	–40 to +105
	R5F56604AGFL	PLQP0048KB-B	512 K	128 K	32 K	Not available	Not available	Available*1	–40 to +105
	R5F56604BGFL	PLQP0048KB-B	512 K	128 K	32 K	Not available	Not available	Available	–40 to +105

Note 1. Products with this part number support only CAN 2.0 protocol.

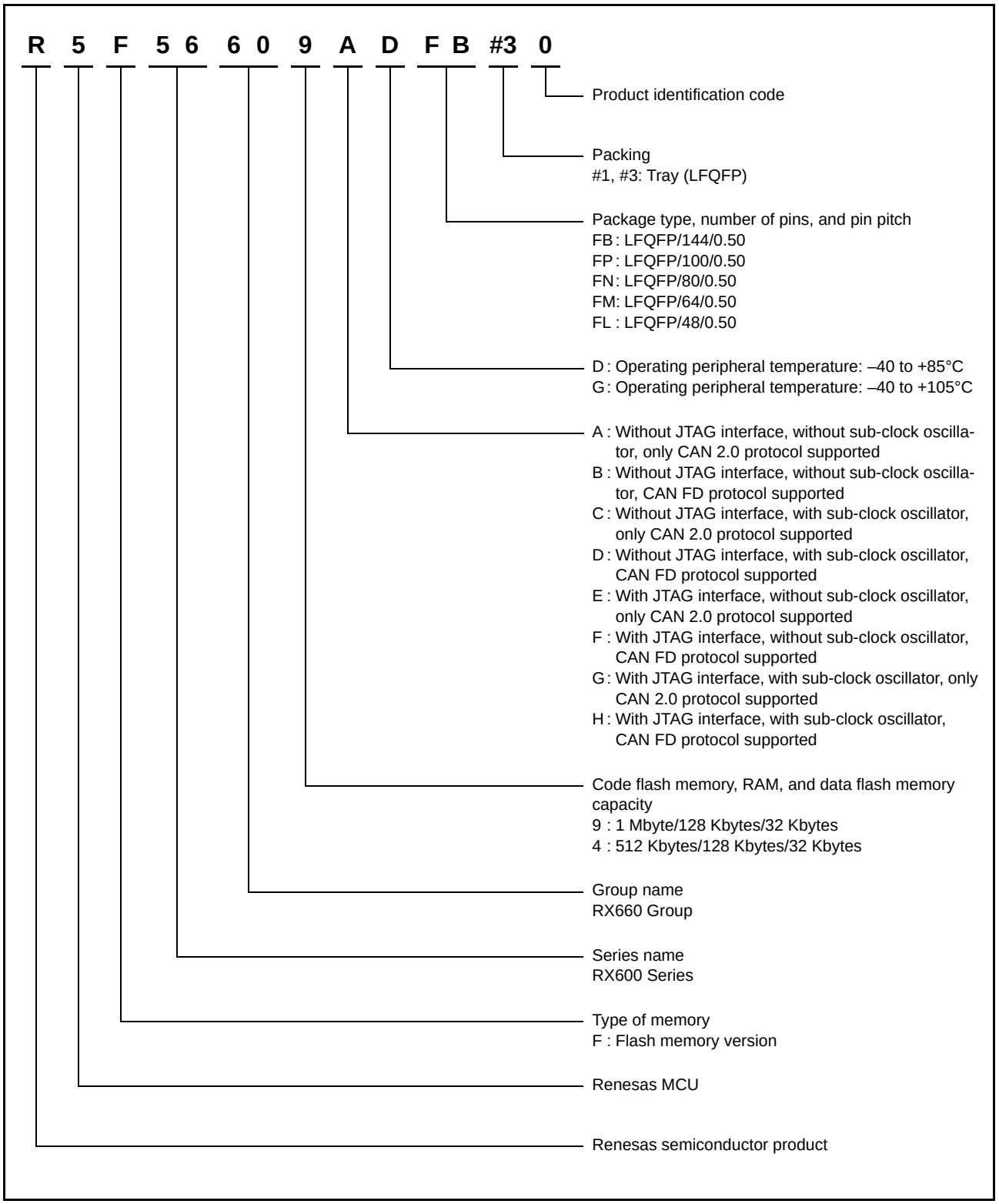


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.

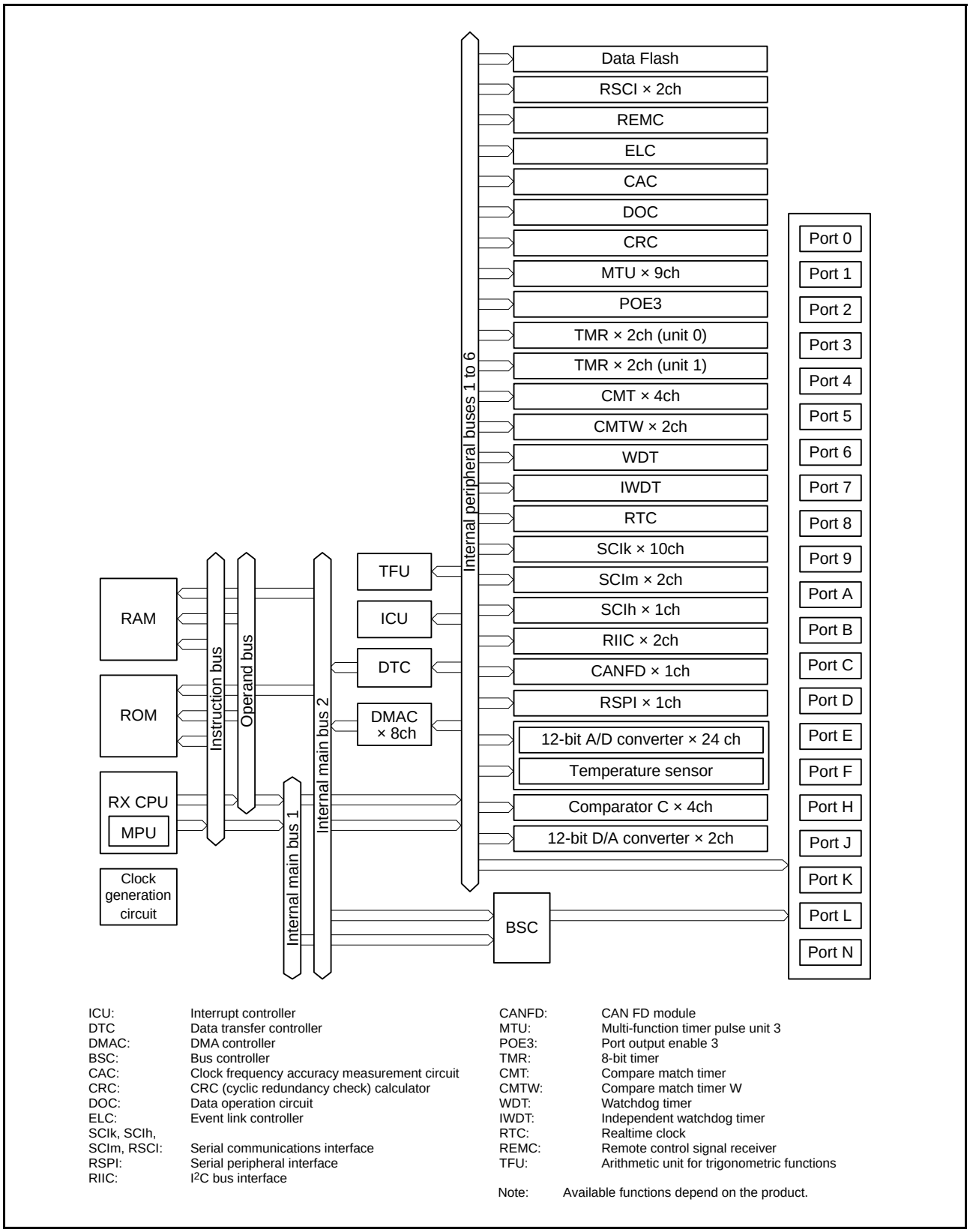


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/5)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.47-µF smoothing capacitor used to stabilize the internal power supply. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	XCOUT	Output	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Operating mode control	MD	Input	Pin for setting the operating mode. For details on how to use this pin, see section 3.1, Operating Mode Types and Selection in the User's Manual: Hardware.
	UB	Input	User boot mode enable pin
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	On-chip emulator enable pin while the JTAG pins are in use If the on-chip emulator is to be used, drive this pin to the high level. If the on-chip emulator is not to be used, drive this pin to the low level.
On-chip emulator	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC TRSYNC1	Output	These pins indicate that output from the TRDATA0 to TRDATA7 pins is valid.
	TRDATA0 TRDATA1 TRDATA2 TRDATA3 TRDATA4 TRDATA5 TRDATA6 TRDATA7	Output	These pins output the trace information.
Address bus	A0 to A20	Output	Output pins for the address
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus

Table 1.4 Pin Functions (2/5)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode
	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS3#	Output	Select signals for CS areas
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15, IRQ0-DS to IRQ15-DS	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU in the high impedance state
8-bit timer	TMO0 to TMO3	Output	Compare match output pins
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter
	TMRI0 to TMRI3	Input	Input pins for the counter reset
Compare match timer W	TIC0 to TIC3	Input	Input pins for CMTW
	TOC0 to TOC3	Output	Output pins for CMTW
Serial communications interface (SCIk)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK9	I/O	Input/output pins for the clock
	RXD0 to RXD9	Input	Input pins for received data
	TXD0 to TXD9	Output	Output pins for transmitted data
	CTS0# to CTS9#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS9#	Output	Output pins for controlling the start of transmission and reception

Table 1.4 Pin Functions (3/5)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIk)	• Simple I2C mode		
	SSCL0 to SSCL9	I/O	Input/output pins for the I2C clock
	SSDA0 to SSDA9	I/O	Input/output pins for the I2C data
	• Simple SPI mode		
	SCK0 to SCK9	I/O	Input/output pins for the clock
	SMISO0 to SMISO9	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI9	I/O	Input/output pins for master transmission of data
	SS0# to SS9#	Input	Chip-select input pins
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I2C mode		
	SSCL12	I/O	Input/output pin for the I2C clock
	SSDA12	I/O	Input/output pin for the I2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface (SCIm)	• Asynchronous mode/clock synchronous mode		
	SCK10, SCK11	I/O	Input/output pins for the clock
	RXD10, RXD11	Input	Input pins for received data
	TXD10, TXD11	Output	Output pins for transmitted data
	CTS10#, CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS10#, RTS11#	Output	Output pins for controlling the start of transmission and reception
	• Simple I2C mode		
	SSCL10, SSCL11	I/O	Input/output pins for the I2C clock
	SSDA10, SSDA11	I/O	Input/output pins for the I2C data
	• Simple SPI mode		
	SCK10, SCK11	I/O	Input/output pins for the clock
	SMISO10, SMISO11	I/O	Input/output pins for slave transmission of data
	SMOSI10, SMOSI11	I/O	Input/output pins for master transmission of data
	SS10#, SS11#	Input	Chip-select input pins

Table 1.4 Pin Functions (4/5)

Classifications	Pin Name	I/O	Description
Serial communications interface (RSCI)	• Asynchronous mode/clock synchronous mode		
	SCK010, SCK011	I/O	Input/output pins for the clock
	RXD010, RXD011	Input	Input pins for received data
	TXD010, TXD011	Output	Output pins for transmitted data
	CTS010#, CTS011#	Input	Input pins for controlling the start of transmission and reception
	RTS010#, RTS011#	Output	Output pins for controlling the start of transmission and reception
	DE010, DE011	Output	DriveEnable output pins
	• Simple I^2C mode		
	SSCL010, SSCL011	I/O	Input/output pins for the I^2C clock
	SSDA010, SSDA011	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK010, SCK011	I/O	Input/output pins for the clock
	SMISO010, SMISO011	I/O	Input/output pins for slave transmission of data
	SMOSI010, SMOSI011	I/O	Input/output pins for master transmission of data
	SS010#, SS011#	Input	Chip-select input pins
	• HBS support mode		
	RXD010, RXD011	Input	Input pin for received data
	TXD010, TXD011, TXDA011, TXDB011	Output	Output pins for transmitted data
I^2C bus interface	SCL0, SCL2	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0, SDA2,	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain
CAN FD module	CRX0	Input	Input pins
	CTX0	Output	Output pins
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave
	SSLA0	I/O	Input/output pin to select the slave for the RSPI
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI
12-bit A/D converter	AN000 to AN023	Input	Input pins for the analog signals to be processed by the A/D converter
	ADST0	Output	Output pin for A/D conversion status.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion
12-bit D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator C	COMP0 to COMP3	Output	Comparator detection result output pins
	CVREFC0 to CVREFC3	Input	Analog reference voltage supply pins for comparator C
	CMPC00, CMPC10, CMPC20, CMPC30	Input	Analog input pins for CMPCn0 (n = 0 to 3)
Realtime clock	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
Remote control signal receiver (REMC)	PMC0	Input	Input pin for external pulse signal

Table 1.4 Pin Functions (5/5)

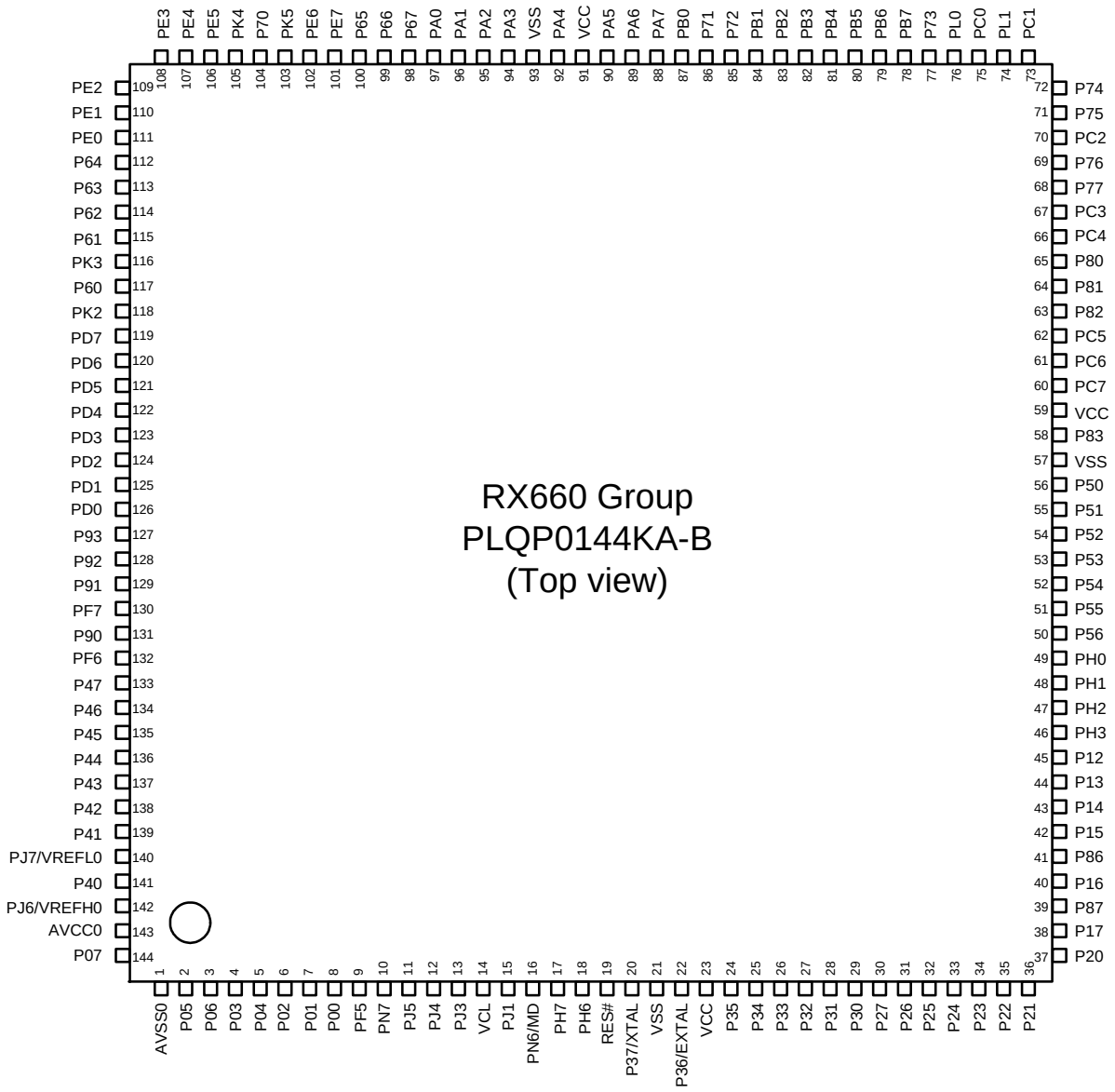
Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0*1	Input	Analog voltage supply pin for the 12-bit A/D converter, 12-bit D/A converter, comparator C, and temperature sensor. Connect the pin to AVSS0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	AVSS0*1	Input	Analog ground pin for the 12-bit A/D converter, 12-bit D/A converter, comparator C, and temperature sensor. Connect the pin to AVCC0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect the pin to VREFL0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin. If the 12-bit A/D converter is not to be used, set this pin to its general-purpose function.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect the pin to VREFH0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin. If the 12-bit A/D converter is not to be used, set this pin to its general-purpose function.
I/O ports	P00 to P07	I/O	8-bit input/output pins
	P12 to P17	I/O	6-bit input/output pins
	P20 to P27	I/O	8-bit input/output pins
	P30 to P37	I/O	8-bit input/output pins (P35: input pin)
	P40 to P47	I/O	8-bit input/output pins
	P50 to P56	I/O	7-bit input/output pins
	P60 to P67	I/O	8-bit input/output pins
	P70 to P77	I/O	8-bit input/output pins
	P80 to P83, P86, P87	I/O	6-bit input/output pins
	P90 to P93	I/O	4-bit input/output pins
	PA0 to PA7	I/O	8-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC7	I/O	8-bit input/output pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0 to PE7	I/O	8-bit input/output pins
	PF5, PF6, PF7	I/O	3-bit input/output pins
	PH0 to PH3, PH6, PH7	I/O	6-bit input/output pins
	PJ1, PJ3 to PJ7	I/O	6-bit input/output pins
	PK2 to PK5	I/O	4-bit input/output pins
	PL0, PL1	I/O	2-bit input/output pins
	PN6, PN7	I/O	2-bit input/output pins

Note: Note the following regarding pin names. For details, see section 1.6, List of Pin and Pin Functions.
- When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group.
- When the pin functions have “-DS” appended to their names, they can also be used as triggers for release from deep software standby.

Note 1. When neither the 12-bit A/D converter nor temperature sensor is to be used, connect the AVCC0 pin to VCC, and the AVSS0 pin to VSS.

1.5 Pin Assignments

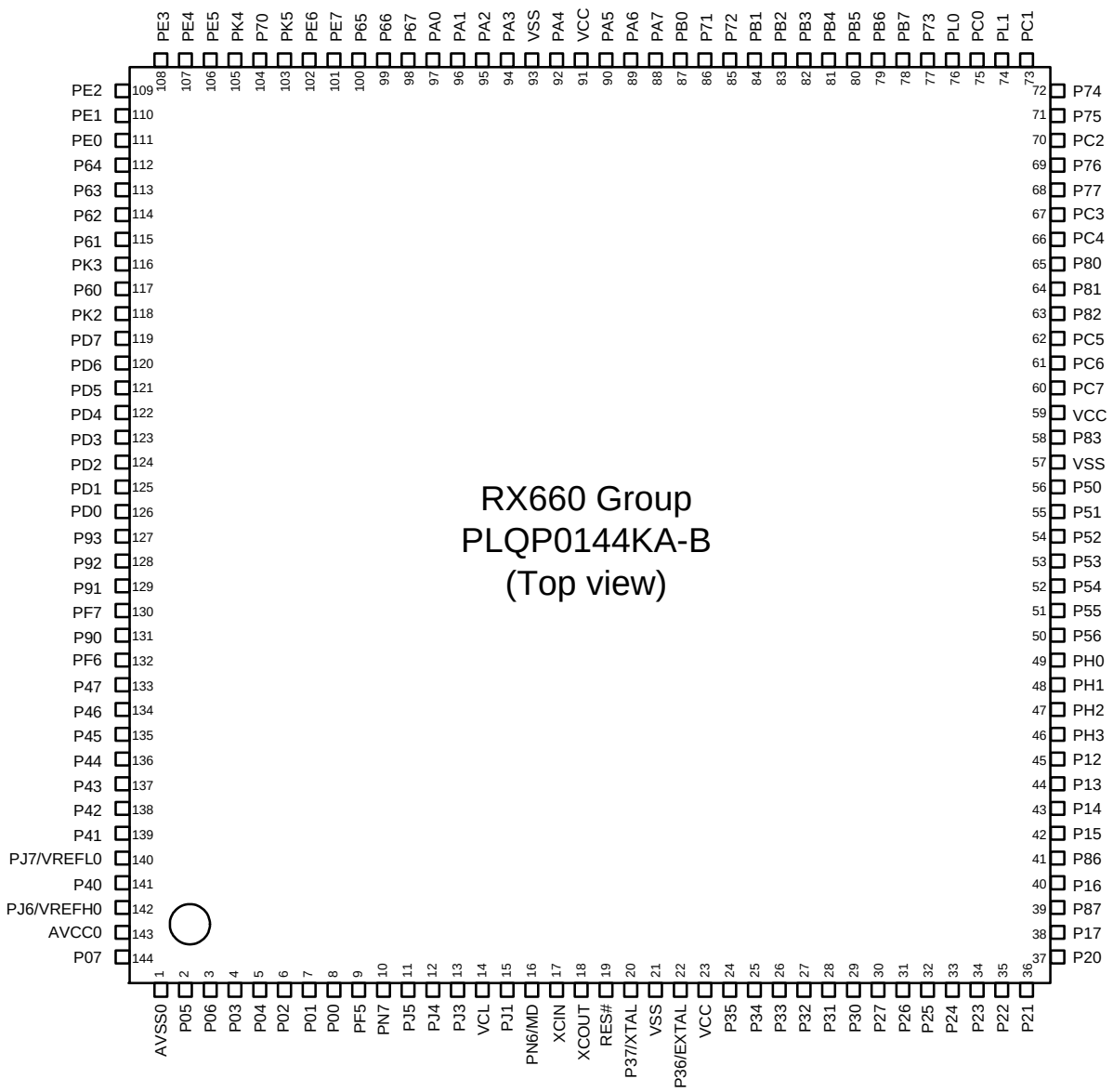
1.5.1 144-Pin LFQFP (without JTAG Interface, without Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (144-Pin LFQFP).

Figure 1.3 Pin Assignment (144-Pin LFQFP (without JTAG Interface, without Sub-clock Oscillator))

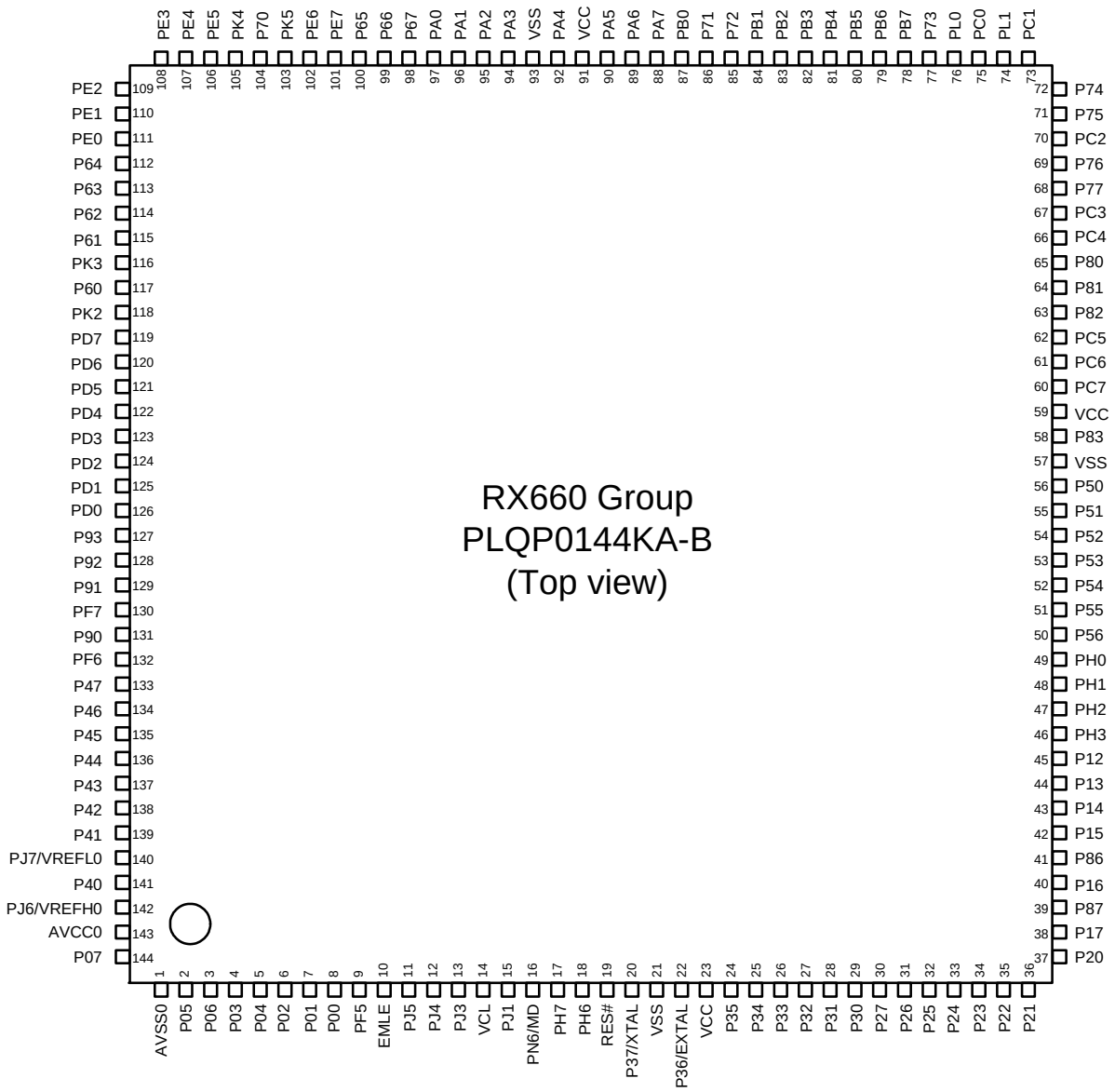
1.5.2 144-Pin LFQFP (without JTAG Interface, with Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (144-Pin LFQFP).

Figure 1.4 Pin Assignment (144-Pin LFQFP (without JTAG Interface, with Sub-clock Oscillator))

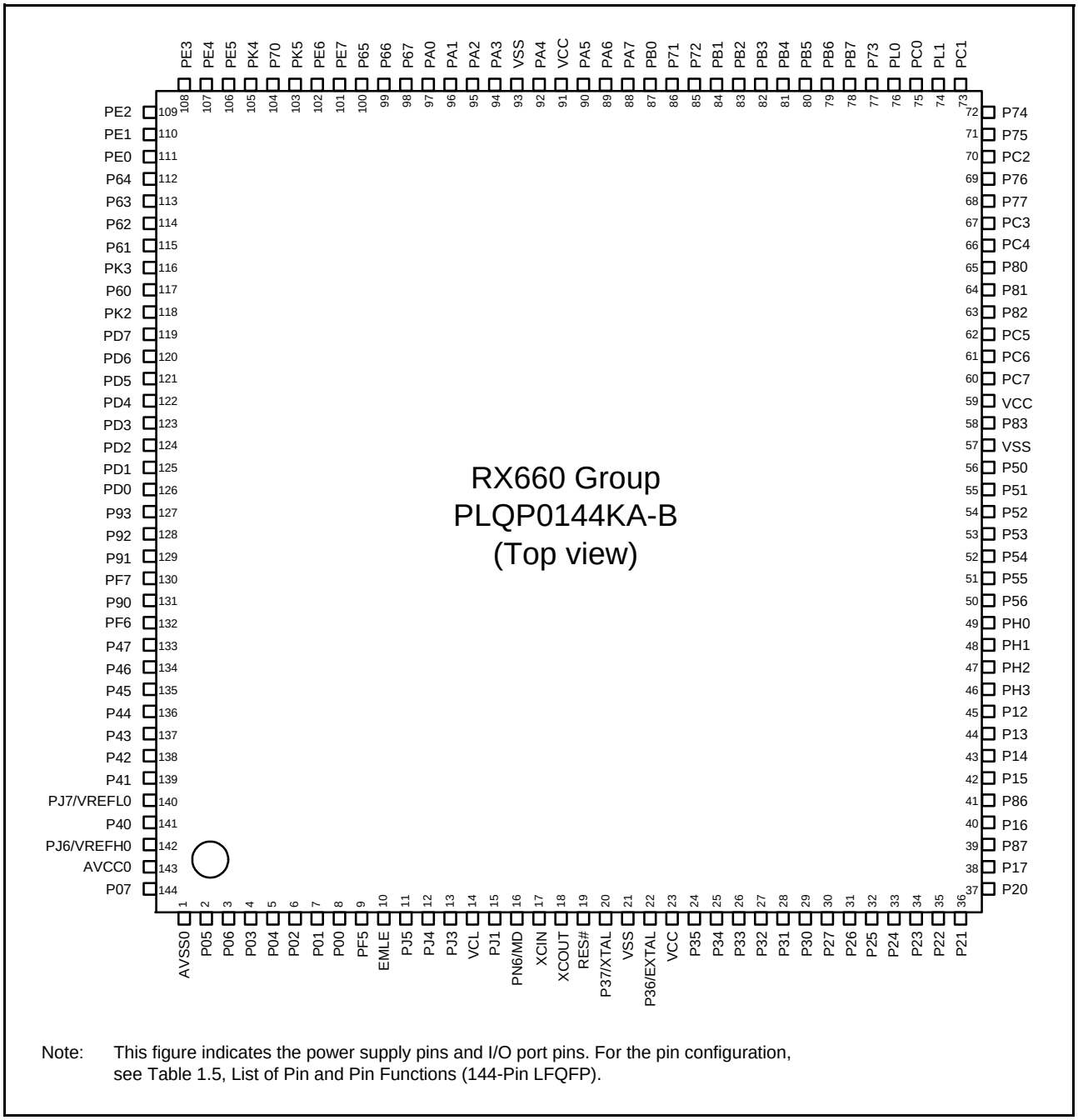
1.5.3 144-Pin LFQFP (with JTAG Interface, without Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (144-Pin LFQFP).

Figure 1.5 Pin Assignment (144-Pin LFQFP (with JTAG Interface, without Sub-clock Oscillator))

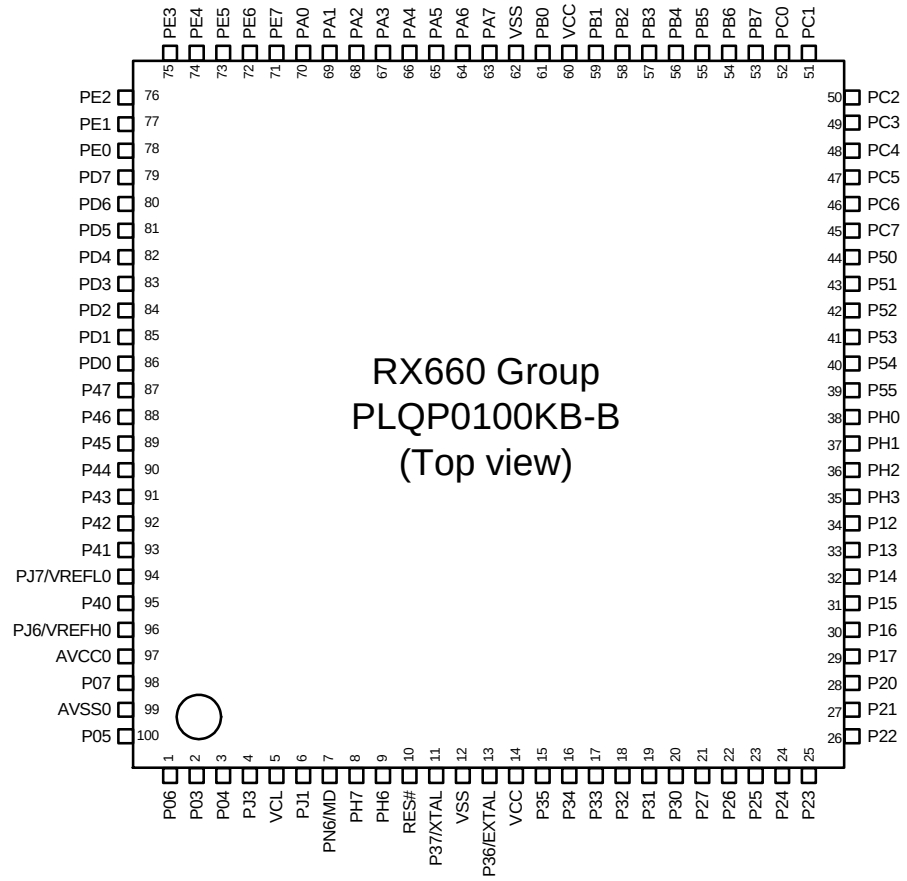
1.5.4 144-Pin LFQFP (with JTAG Interface, with Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (144-Pin LFQFP).

Figure 1.6 Pin Assignment (144-Pin LFQFP (with JTAG Interface, with Sub-clock Oscillator))

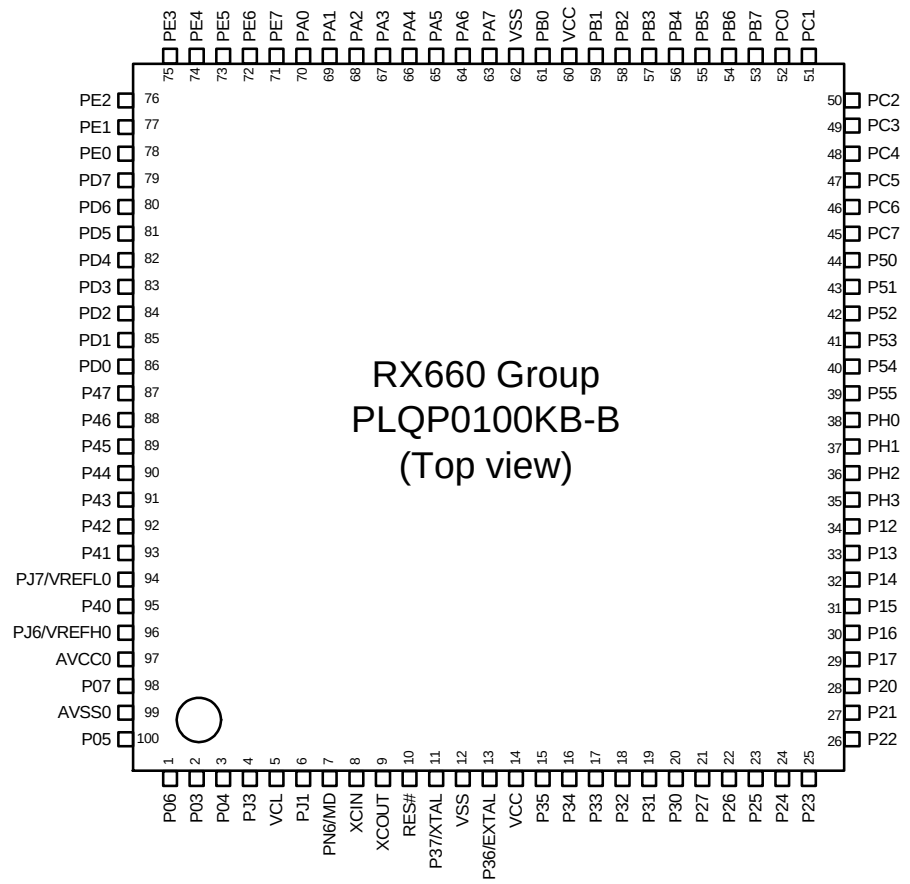
1.5.5 100-Pin LFQFP (without JTAG Interface, without Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (100-Pin LFQFP).

Figure 1.7 Pin Assignment (100-Pin LFQFP (without JTAG Interface, without Sub-clock Oscillator))

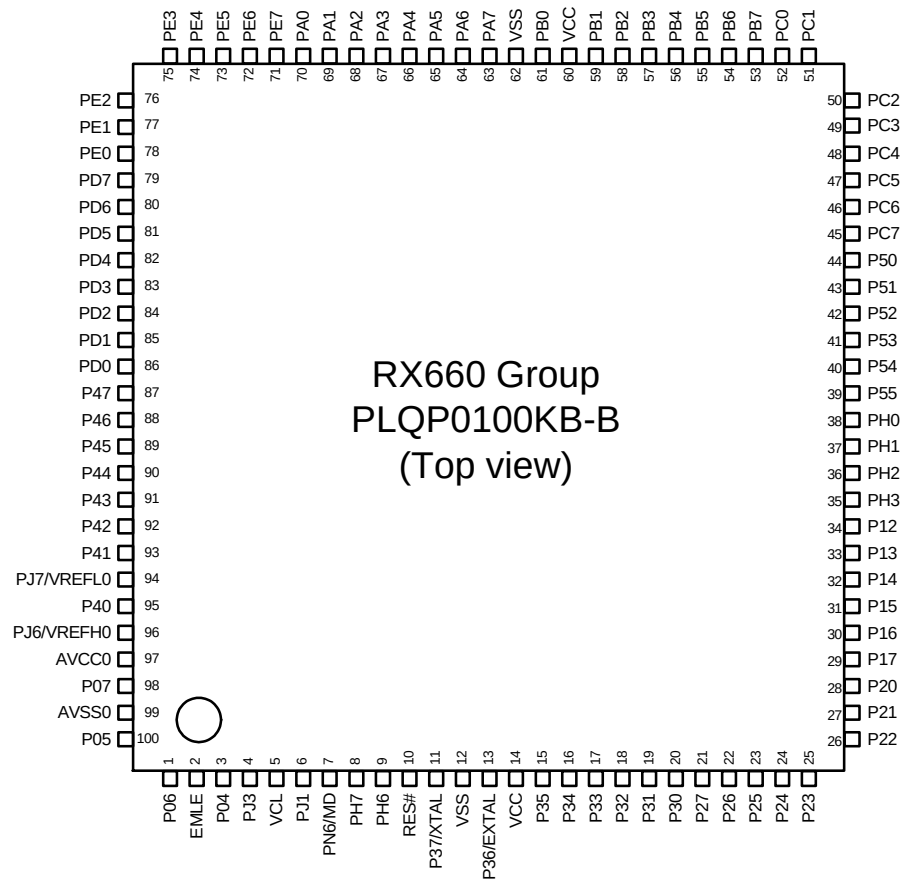
1.5.6 100-Pin LFQFP (without JTAG Interface, with Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (100-Pin LFQFP).

Figure 1.8 Pin Assignment (100-Pin LFQFP (without JTAG Interface, with Sub-clock Oscillator))

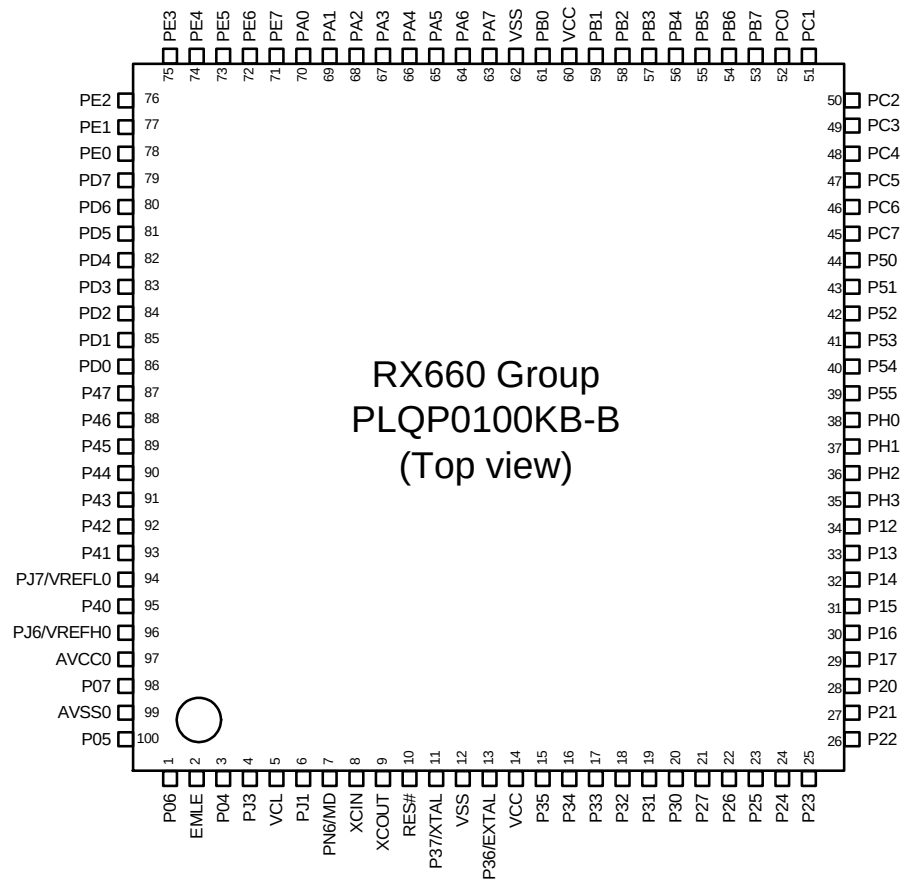
1.5.7 100-Pin LFQFP (with JTAG Interface, without Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (100-Pin LFQFP).

Figure 1.9 Pin Assignment (100-Pin LFQFP (with JTAG Interface, without Sub-clock Oscillator))

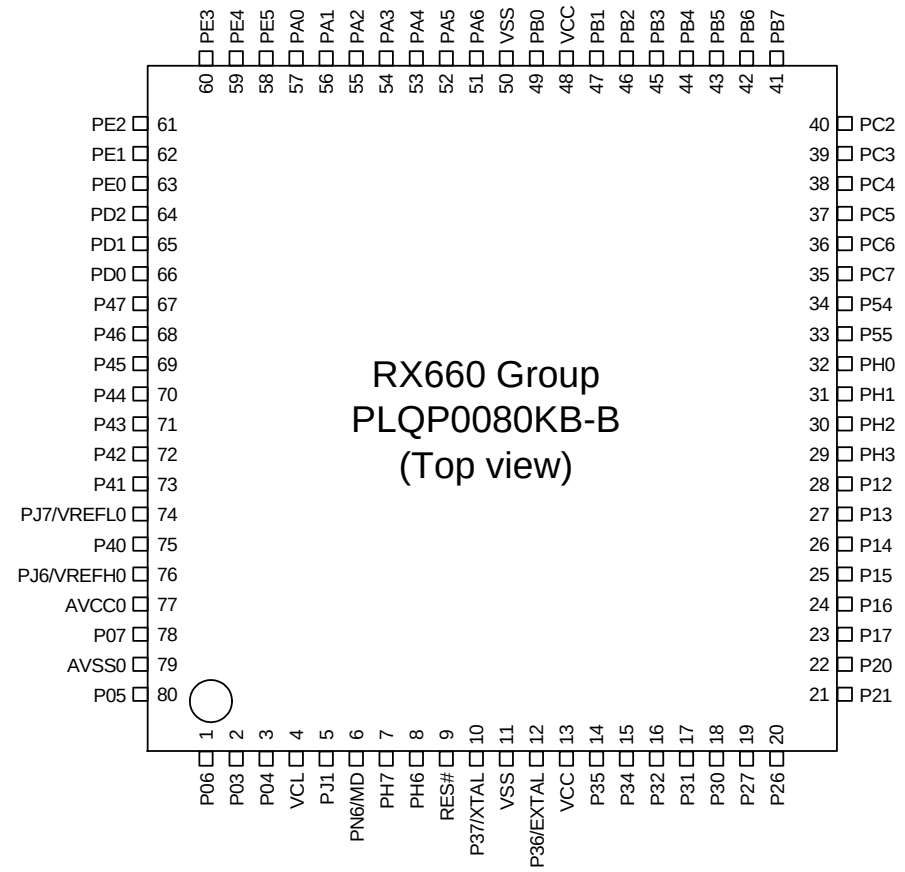
1.5.8 100-Pin LFQFP (with JTAG Interface, with Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (100-Pin LFQFP).

Figure 1.10 Pin Assignment (100-Pin LFQFP (with JTAG Interface, with Sub-clock Oscillator))

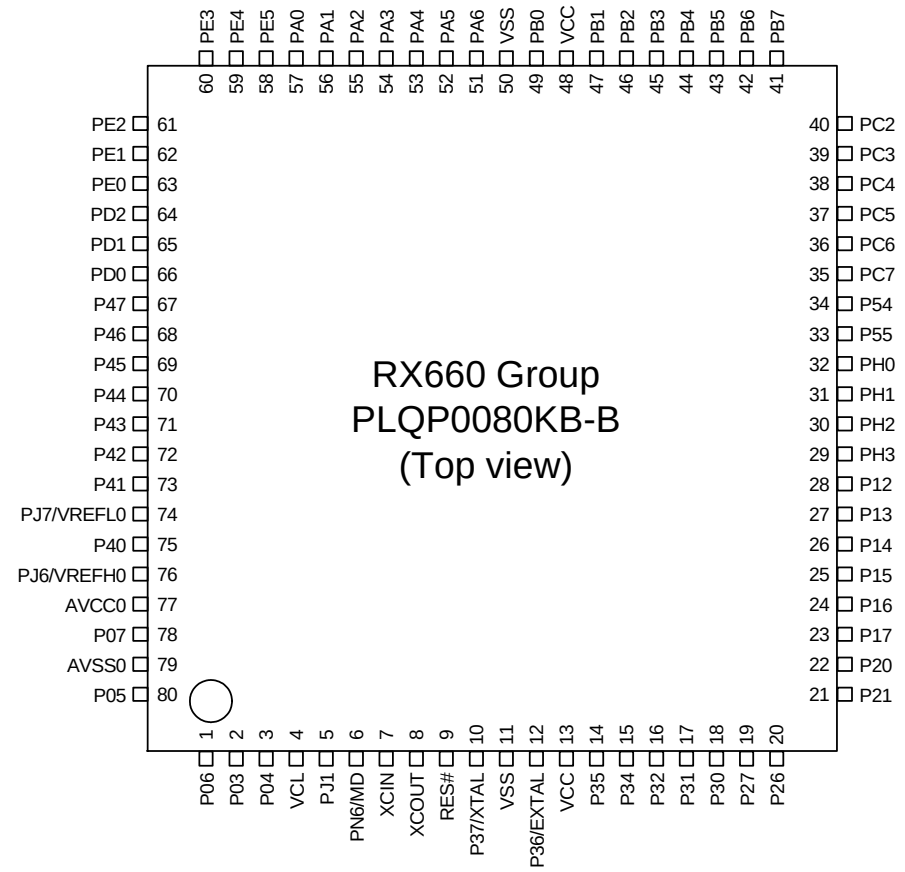
1.5.9 80-Pin LFQFP (without Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pin and Pin Functions (80-Pin LFQFP).

Figure 1.11 Pin Assignment (80-Pin LFQFP (without Sub-clock Oscillator))

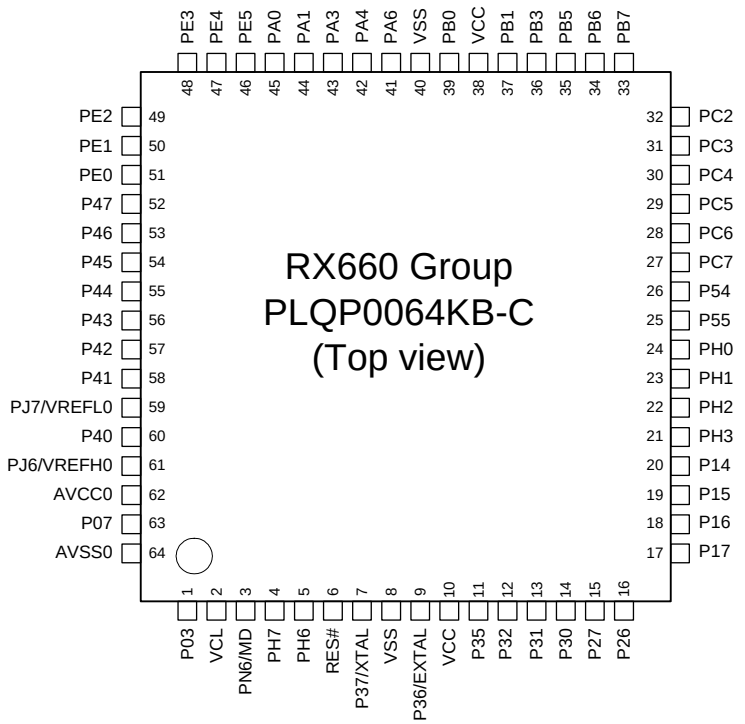
1.5.10 80-Pin LFQFP (with Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pin and Pin Functions (80-Pin LFQFP).

Figure 1.12 Pin Assignment (80-Pin LFQFP (with Sub-clock Oscillator))

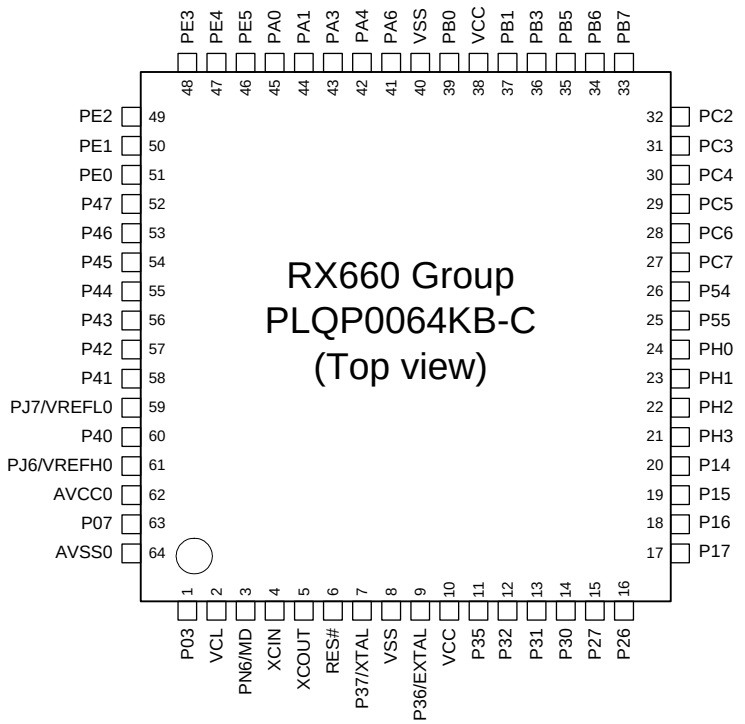
1.5.11 64-Pin LFQFP (without Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pin and Pin Functions (64-Pin LFQFP).

Figure 1.13 Pin Assignment (64-Pin LFQFP (without Sub-clock Oscillator))

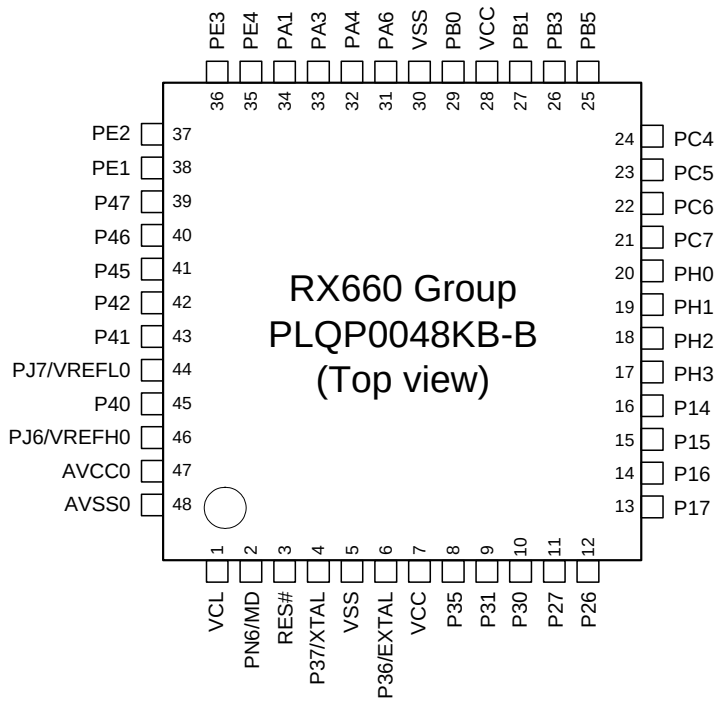
1.5.12 64-Pin LFQFP (with Sub-clock Oscillator)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pin and Pin Functions (64-Pin LFQFP).

Figure 1.14 Pin Assignment (64-Pin LFQFP (with Sub-clock Oscillator))

1.5.13 48-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pin and Pin Functions (48-Pin LFQFP).

Figure 1.15 Pin Assignment (48-Pin LFQFP)

1.6 List of Pin and Pin Functions

1.6.1 144-Pin LFQFP

Table 1.5 List of Pin and Pin Functions (144-Pin LFQFP) (1/6)

Pin No.	Power Supply Clock System Control	I/O Port	Bus	Timer	Communication	Interrupt	A/D, D/A, CMPC
144-Pin LFQFP				(MTU, TMR, RTC, POE, CAC, CMTW)	(SCI, RSCI, RSPI, RIIC, CANFD, REMC)	(IRQ, NMI)	
1	AVSS0						
2		P05				IRQ13	DA1
3		P06					
4		P03				IRQ11	DA0
5		P04					
6		P02		TMCI1	SCK6	IRQ10	
7		P01		TMCI0	RXD6/SMISO6/ SSCL6	IRQ9	
8		P00		TMRI0	TXD6/SMOSI6/ SSDA6	IRQ8	
9		PF5				IRQ4	
10	EMLE*1	PN7*2					
11		PJ5		POE8#	CTS2#/RTS2#/SS2#	IRQ13	
12		PJ4					
13		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#	IRQ11	
14	VCL						
15		PJ1		MTIOC3A			
16	MD/FINED	PN6					
17	XCIN*3	PH7*4					
18	XCOUT*3	PH6*4					
19	RES#						
20	XTAL	P37				IRQ4	
21	VSS						
22	EXTAL	P36				IRQ5	
23	VCC						
24		P35				NMI	
25	TRST#*1	P34		MTIOC0A/TMCI3/ POE10#	SCK6/SCK0	IRQ4	
26		P33		MTIOC0D/TMRI3/ POE4#/POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0-A	IRQ3-DS	
27		P32		MTIOC0C/TMO3/ RTCIC2*5/RTCOUT*5/ POE0#/POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0-A	IRQ2-DS	
28	TMS*1	P31		MTIOC4D/TMCI2/ RTCIC1*5	CTS1#/RTS1#/SS1#	IRQ1-DS	
29	TDI*1	P30		MTIOC4B/TMRI3/ RTCIC0*5/POE8#	RXD1/SMISO1/ SSCL1	IRQ0-DS	COMP3
30	TCK*1	P27	CS3#	MTIOC2B/TMCI3	SCK1	IRQ7	CVREFC3

Table 1.5 List of Pin and Pin Functions (144-Pin LFQFP) (2/6)

Pin No. 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
31	TDO*1	P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#	IRQ6	CMPC30
32		P25	CS1#	MTIOC4C/MTCLKB	RXD3/SMISO3/ SSCL3	IRQ5	ADTRG0#
33		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1	SCK3	IRQ12	
34		P23		MTIOC3D/MTCLKD	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#	IRQ3	
35		P22		MTIOC3B/MTCLKC/ TMO0	SCK0	IRQ15	
36		P21		MTIOC1B/TMCI0/ MTIOC4A	RXD0/SMISO0/ SSCL0	IRQ9	
37		P20		MTIOC1A/TMRI0	TXD0/SMOSI0/ SSDA0	IRQ8	
38		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#/ MTIOC4B	SCK1/TXD3/SMOSI3/ SSDA3/MISOA-C/ SDA2	IRQ7	COMP2
39		P87		MTIOC4C	SMOSI10/SSDA10/ TXD10/TXD010-B/ SMOSI010-B/ SSDA010-B	IRQ15	
40		P16		MTIOC3C/MTIOC3D/ TMO2/RTCOUT*5	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ MOSIA-C/SCL2	IRQ6	ADTRG0#
41		P86		MTIOC4D	SMISO10/SSCL10/ RXD10/RXD010-B/ SMISO010-B/ SSCL010-B	IRQ14	
42		P15		MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/ SSCL1/SCK3/ CRX0-C	IRQ5	CMPC20
43		P14		MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#/ CTX0-C	IRQ4	CVREFC2
44		P13		MTIOC0B/TMO3	TXD2/SMOSI2/ SSDA2/SDA0	IRQ3	
45		P12		MTIC5U/TMCI1	RXD2/SMISO2/ SSCL2/SCL0	IRQ2	
46		PH3		MTIOC4D/TMCI0			
47		PH2		MTIOC4C/TMRI0/ TOC1		IRQ1	
48		PH1		MTIOC3D/TMO0/TIC1		IRQ0	ADST0
49		PH0		MTIOC3B/CACREF			ADTRG0#
50		P56		MTIOC3C	SCK7	IRQ6	
51	TRDATA3*1	P55	D0[A0/D0]/ WAIT#	MTIOC4D/MTIOC4A/ TMO3	TXD7/SMOSI7/ SSDA7/CRX0-D	IRQ10	
52	TRDATA2*1	P54	ALE/ D1[A1/D1]	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX0-D	IRQ4	
53		P53	BCLK		PMC0	IRQ3	
54		P52	RD#		RXD2/SMISO2/ SSCL2	IRQ2	

Table 1.5 List of Pin and Pin Functions (144-Pin LFQFP) (3/6)

Pin No. 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
55		P51	WR1#/BC1#/ WAIT#		SCK2/PMC0	IRQ1	
56		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2	IRQ0	
57	VSS						
58	TRCLK*1	P83		MTIOC4C	SCK10/SS10#/ CTS10#/SCK010-B/ CTS010#-A/SS010#-A	IRQ3	
59	VCC						
60	UB	PC7	CS0#	MTIOC3A/MTCLKB/ TMO2/CACREF/TOC0	TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ TXD010-C/ SMOSI010-C/ SSDA010-C/MISOA-A	IRQ14	
61		PC6	D2[A2/D2]/ CS1#	MTIOC3C/MTCLKA/ TMCI2/TIC0	RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ RXD010-C/ SMISO010-C/ SSCL010-C/MOSIA-A	IRQ13	
62		PC5	D3[A3/D3]/ CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2/MTIOC0C	SCK8/SCK10/ SCK010-C/ RSPCKA-A/PMC0	IRQ5	
63	TRSYNC*1	P82		MTIOC4A	SMOSI10/SSDA10/ TXD10/TXD010-A/ SMOSI010-A/ SSDA010-A	IRQ2	
64	TRDATA1*1	P81		MTIOC3D	SMISO10/SSCL10/ RXD10/RXD010-A/ SMISO010-A/ SSCL010-A	IRQ9	
65	TRDATA0*1	P80		MTIOC3B	SCK10/RTS10#/ SCK010-A/ RTS010#-A/DE010-A	IRQ8	
66		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#/ MTIOC0A	SCK5/CTS8#/RTS8#/ SS8#/SS10#/CTS10#/ RTS10#/CTS010#-B/ RTS010#-B/ SS010#-B/DE010-B/ SSLA0-A/PMC0	IRQ12	
67		PC3	A19	MTIOC4D	TXD5/SMOSI5/ SSDA5/PMC0	IRQ11	
68	TRDATA7*1	P77			SMOSI11/SSDA11/ TXD11/TXD011-A/ SMOSI011-A/ SSDA011-A	IRQ7	
69	TRDATA6*1	P76			SMISO11/SSCL11/ RXD11/RXD011-A/ SMISO011-A/ SSCL011-A	IRQ14	
70		PC2	A18	MTIOC4B	RXD5/SMISO5/ SSCL5/TXDB011-A/ SSLA3-A	IRQ10	
71	TRSYNC1*1	P75			SCK11/RTS11#/ SCK011-A/ RTS011#-A/DE011-A	IRQ13	

Table 1.5 List of Pin and Pin Functions (144-Pin LFQFP) (4/6)

Pin No. 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
72	TRDATA5*1	P74	A20		SS11#/CTS11#/ CTS011#-A/SS011#-A	IRQ12	
73		PC1	A17	MTIOC3A	SCK5/TXD011-C/ SMOSI011-C/ SSDA011-C/ TXDA011-C/SSLA2-A	IRQ12	
74		PL1					
75		PC0	A16	MTIOC3C	CTS5#/RTS5#/SS5#/ RXD011-C/ SMISO011-C/ SSCL011-C/SSLA1-A	IRQ14	
76		PL0					
77	TRDATA4*1	P73	CS3#			IRQ8	
78		PB7	A15	MTIOC3B	TXD9/SMOSI9/ SSDA9/SMOSI11/ SSDA11/TXD11/ TXD011-B/ SMOSI011-B/ SSDA011-B	IRQ15	
79		PB6	A14	MTIOC3D	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ RXD011-B/ SMISO011-B/ SSCL011-B	IRQ6	
80		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE4#/TOC2	SCK9/SCK11/ SCK011-B	IRQ13	
81		PB4	A12		CTS9#/RTS9#/SS9#/ SS11#/CTS11#/ RTS11#/CTS011#-B/ RTS011#-B/ SS011#-B/DE011-B	IRQ4	
82		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE11#/TIC2	SCK4/SCK6/PMC0	IRQ3	
83		PB2	A10		CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#	IRQ2	
84		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0	TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6	IRQ4-DS	COMP1
85		P72	A19/CS2#			IRQ10	
86		P71	A18/CS1#			IRQ1	
87		PB0	A8	MTIC5W/MTIOC3D	RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6/ RSPCKA-C	IRQ12	
88		PA7	A7		MISOA-B	IRQ7	
89		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE10#/ MTIOC3D/MTIOC6B	CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/ SS12#/MOSIA-B	IRQ14	
90		PA5	A5	MTIOC6B	RSPCKA-B	IRQ5	
91	VCC						

Table 1.5 List of Pin and Pin Functions (144-Pin LFQFP) (5/6)

Pin No. 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
92		PA4	A4	MTIC5U/MTCLKA/ TMRI0/MTIOC4C/ MTIOC7C	TXD5/SMOSI5/ SSDA5/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ SSLA0-B	IRQ5-DS	CVREFC1/ ADST0
93	VSS						
94		PA3	A3	MTIOC0D/MTCLKD/ MTIC5V/MTIOC4D	RXD5/SMISO5/ SSCL5	IRQ6-DS	CMPC10
95		PA2	A2	MTIOC7A	RXD5/SMISO5/ SSCL5/RXD12/ SMISO12/SSCL12/ RXDX12/SSLA3-B	IRQ10	
96		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/MTIOC3B	SCK5/SCK12/ SSLA2-B	IRQ11	ADTRG0#
97		PA0	BC0#/A0	MTIOC4A/CACREF/ MTIOC6D	SSLA1-B	IRQ0	
98		P67		MTIOC7C		IRQ15	
99		P66		MTIOC7D		IRQ14	
100		P65				IRQ13	
101		PE7	D15[A15/D15]/ D7[A7/D7]	MTIOC6A/TOC1		IRQ7	AN015
102		PE6	D14[A14/D14]/ D6[A6/D6]	MTIOC6C/TIC1	CTS4#/RTS4#/SS4#	IRQ6	AN014
103		PK5			TXD4/SMOSI4/ SSDA4		
104		P70			SCK4	IRQ0	
105		PK4			RXD4/SMISO4/ SSCL4		
106		PE5	D13[A13/D13]/ D5[A5/D5]	MTIOC4C/MTIOC2B		IRQ5	AN013/ COMP0
107		PE4	D12[A12/D12]/ D4[A4/D4]	MTIOC4D/MTIOC1A/ MTIOC4A/MTIOC7D		IRQ12	AN012
108		PE3	D11[A11/D11]/ D3[A3/D3]	MTIOC4B/POE8#/ MTIOC1B/TOC3	CTS12#/RTS12#/ SS12#	IRQ11	AN011
109		PE2	D10[A10/D10]/ D2[A2/D2]	MTIOC4A/MTIOC7A/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12	IRQ7-DS	AN010/ CVREFC0
110		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/MTIOC3B	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	IRQ9	AN009/ CMPC00
111		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12	IRQ8	AN008
112		P64	D3[A3/D3]			IRQ4	
113		P63	D2[A2/D2]/ CS3#			IRQ3	
114		P62	D1[A1/D1]/ CS2#			IRQ2	
115		P61	D0[A0/D0]/ CS1#		CTS9#/RTS9#/SS9#	IRQ1	
116		PK3			RXD9/SMISO9/ SSCL9		
117		P60	CS0#		SCK9	IRQ0	
118		PK2			TXD9/SMOSI9/ SSDA9		

Table 1.5 List of Pin and Pin Functions (144-Pin LFQFP) (6/6)

Pin No. 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
119	TRDATA3*1	PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7	AN023
120	TRDATA2*1	PD6	D6[A6/D6]	MTIC5V/POE4#/ MTIOC8A		IRQ6	AN022
121	TRCLK*1	PD5	D5[A5/D5]	MTIC5W/POE10#/ MTIOC8C		IRQ5	AN021
122	TRSYNC*1	PD4	D4[A4/D4]	POE11#/MTIOC8B		IRQ4	AN020
123	TRDATA1*1	PD3	D3[A3/D3]	POE8#/MTIOC8D/ TOC2		IRQ3	AN019
124	TRDATA0*1	PD2	D2[A2/D2]	MTIOC4D/TIC2	CRX0-B	IRQ2	AN018
125	TRDATA7*1	PD1	D1[A1/D1]	MTIOC4B/POE0#	CTX0-B	IRQ1	AN017
126	TRDATA6*1	PD0	D0[A0/D0]	POE4#		IRQ0	AN016
127	TRSYNC1*1	P93	A19	POE0#	CTS7#/RTS7#/SS7#	IRQ11	
128	TRDATA5*1	P92	A18	POE4#	RXD7/SMISO7/ SSCL7	IRQ10	
129	TRDATA4*1	P91	A17		SCK7	IRQ9	
130		PF7					
131		P90	A16		TXD7/SMOSI7/ SSDA7	IRQ0	
132		PF6					
133		P47				IRQ15-DS	AN007
134		P46				IRQ14-DS	AN006
135		P45				IRQ13-DS	AN005
136		P44				IRQ12-DS	AN004
137		P43				IRQ11-DS	AN003
138		P42				IRQ10-DS	AN002
139		P41				IRQ9-DS	AN001
140	VREFL0	PJ7					
141		P40				IRQ8-DS	AN000
142	VREFH0	PJ6					
143	AVCC0						
144		P07				IRQ15	ADTRG0#

Note 1. This pin function is not provided for products with no JTAG interface.
Note 2. This pin function is not provided for products with a JTAG interface.
Note 3. This pin function is not provided for products with no sub-clock oscillator.
Note 4. This pin function is not provided for products with a sub-clock oscillator.
Note 5. This pin function is not available in products with no sub-clock oscillator.

1.6.2 100-Pin LFQFP

Table 1.6 List of Pin and Pin Functions (100-Pin LFQFP) (1/5)

Pin No. 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
1		P06					
2	EMLE*1	P03*2				IRQ11*2	DA0*2
3		P04					
4		PJ3		MTIOC3C	CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#	IRQ11	
5	VCL						
6		PJ1		MTIOC3A			
7	MD/FINED	PN6					
8	XCIN*3	PH7*4					
9	XCOUT*3	PH6*4					
10	RES#						
11	XTAL	P37				IRQ4	
12	VSS						
13	EXTAL	P36				IRQ5	
14	VCC						
15		P35				NMI	
16	TRST#*1	P34		MTIOC0A/TMCI3/ POE10#	SCK6/SCK0	IRQ4	
17		P33		MTIOC0D/TMRI3/ POE4#/POE11#	RXD6/SMISO6/ SSCL6/RXD0/ SMISO0/SSCL0/ CRX0-A	IRQ3-DS	
18		P32		MTIOC0C/TMO3/ RTCIC2*5/RTCOUT*5/ POE0#/POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0-A	IRQ2-DS	
19	TMS*1	P31		MTIOC4D/TMCI2/ RTCIC1*5	CTS1#/RTS1#/SS1#	IRQ1-DS	
20	TDI*1	P30		MTIOC4B/TMRI3/ RTCIC0*5/POE8#	RXD1/SMISO1/ SSCL1	IRQ0-DS	COMP3
21	TCK*1	P27	CS3#	MTIOC2B/TMCI3	SCK1	IRQ7	CVREFC3
22	TDO*1	P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#	IRQ6	CMPC30
23		P25	CS1#	MTIOC4C/MTCLKB	RXD3/SMISO3/ SSCL3	IRQ5	ADTRG0#
24		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1	SCK3	IRQ12	
25		P23		MTIOC3D/MTCLKD	TXD3/SMOSI3/ SSDA3/CTS0#/ RTS0#/SS0#	IRQ3	
26		P22		MTIOC3B/MTCLKC/ TMO0	SCK0	IRQ15	
27		P21		MTIOC1B/TMCI0/ MTIOC4A	RXD0/SMISO0/ SSCL0	IRQ9	
28		P20		MTIOC1A/TMRI0	TXD0/SMOSI0/ SSDA0	IRQ8	

Table 1.6 List of Pin and Pin Functions (100-Pin LFQFP) (2/5)

Pin No. 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
29		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#/ MTIOC4B	SCK1/TXD3/SMOSI3/ SSDA3/MISOA-C/ SDA2	IRQ7	COMP2
30		P16		MTIOC3C/MTIOC3D/ TMO2/RTCOUT*5	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ MOSIA-C/SCL2	IRQ6	ADTRG0#
31		P15		MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/ SSCL1/SCK3/ CRX0-C	IRQ5	CMPC20
32		P14		MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#/ CTX0-C	IRQ4	CVREFC2
33		P13		MTIOC0B/TMO3	TXD2/SMOSI2/ SSDA2/SDA0	IRQ3	
34		P12		MTIC5U/TMCI1	RXD2/SMISO2/ SSCL2/SCL0	IRQ2	
35		PH3		MTIOC4D/TMCI0			
36		PH2		MTIOC4C/TMRI0/ TOC1		IRQ1	
37		PH1		MTIOC3D/TMO0/TIC1		IRQ0	ADST0
38		PH0		MTIOC3B/CACREF			ADTRG0#
39		P55	D0[A0/D0]/ WAIT#	MTIOC4D/MTIOC4A/ TMO3	CRX0-D	IRQ10	
40		P54	ALE/ D1[A1/D1]	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX0-D	IRQ4	
41		P53	BCLK		PMC0	IRQ3	
42		P52	RD#		RXD2/SMISO2/ SSCL2	IRQ2	
43		P51	WR1#/BC1#/ WAIT#		SCK2/PMC0	IRQ1	
44		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2	IRQ0	
45	UB	PC7	CS0#	MTIOC3A/MTCLKB/ TMO2/CACREF/TOC0	TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ TXD010-C/ SMOSI010-C/ SSDA010-C/MISOA-A	IRQ14	
46		PC6	D2[A2/D2]/ CS1#	MTIOC3C/MTCLKA/ TMCI2/TIC0	RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ RXD010-C/ SMISO010-C/ SSCL010-C/MOSIA-A	IRQ13	
47		PC5	D3[A3/D3]/ CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2/MTIOC0C	SCK8/SCK10/ SCK010-C/ RSPCKA-A/PMC0	IRQ5	
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#/ MTIOC0A	SCK5/CTS8#/RTS8#/ SS8#/SS10#/CTS10#/ RTS10#/CTS010#-B/ RTS010#-B/ SS010#-B/DE010-B/ SSLA0-A/PMC0	IRQ12	
49		PC3	A19	MTIOC4D	TXD5/SMOSI5/ SSDA5/PMC0	IRQ11	

Table 1.6 List of Pin and Pin Functions (100-Pin LFQFP) (3/5)

Pin No.	Power Supply Clock System Control	I/O Port	Bus	Timer	Communication	Interrupt	A/D, D/A, CMPC
100-Pin LFQFP				(MTU, TMR, RTC, POE, CAC, CMTW)	(SCI, RSCI, RSPI, RIIC, CANFD, REMC)	(IRQ, NMI)	
50		PC2	A18	MTIOC4B	RXD5/SMISO5/ SSCL5/TXDB011-A/ SSLA3-A	IRQ10	
51		PC1	A17	MTIOC3A	SCK5/TXD011-C/ SMOSI011-C/ SSDA011-C/ TXDA011-C/SSLA2-A	IRQ12	
52		PC0	A16	MTIOC3C	CTS5#/RTS5#/SS5#/ RXD011-C/ SMISO011-C/ SSCL011-C/SSLA1-A	IRQ14	
53		PB7	A15	MTIOC3B	TXD9/SMOSI9/ SSDA9/SMOSI11/ SSDA11/TXD11/ TXD011-B/ SMOSI011-B/ SSDA011-B	IRQ15	
54		PB6	A14	MTIOC3D	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ RXD011-B/ SMISO011-B/ SSCL011-B	IRQ6	
55		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE4#/TOC2	SCK9/SCK11/ SCK011-B	IRQ13	
56		PB4	A12		CTS9#/RTS9#/SS9#/ SS11#/CTS11#/ RTS11#/CTS011#-B/ RTS011#-B/ SS011#-B/DE011-B	IRQ4	
57		PB3	A11	MTIOC0A/MTIOC4A/ TMO0/POE11#/TIC2	SCK4/SCK6/PMC0	IRQ3	
58		PB2	A10		CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#	IRQ2	
59		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0	TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6	IRQ4-DS	COMP1
60	VCC						
61		PB0	A8	MTIC5W/MTIOC3D	RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6/ RSPCKA-C	IRQ12	
62	VSS						
63		PA7	A7		MISOA-B	IRQ7	
64		PA6	A6	MTIC5V/MTCLKB/ TMCI3/POE10#/ MTIOC3D/MTIOC6B	CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/ SS12#/MOSIA-B	IRQ14	
65		PA5	A5	MTIOC6B	RSPCKA-B	IRQ5	
66		PA4	A4	MTIC5U/MTCLKA/ TMRI0/MTIOC4C/ MTIOC7C	TXD5/SMOSI5/ SSDA5/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ SSLA0-B	IRQ5-DS	CVREFC1/ ADST0
67		PA3	A3	MTIOC0D/MTCLKD/ MTIC5V/MTIOC4D	RXD5/SMISO5/ SSCL5	IRQ6-DS	CMPC10

Table 1.6 List of Pin and Pin Functions (100-Pin LFQFP) (4/5)

Pin No. 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
68		PA2	A2	MTIOC7A	RXD5/SMISO5/ SSCL5/RXD12/ SMISO12/SSCL12/ RXDX12/SSLA3-B	IRQ10	
69		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/MTIOC3B	SCK5/SCK12/ SSLA2-B	IRQ11	ADTRG0#
70		PA0	BC0#/A0	MTIOC4A/CACREF/ MTIOC6D	SSLA1-B	IRQ0	
71		PE7	D15[A15/D15]/ D7[A7/D7]	MTIOC6A/TOC1		IRQ7	AN015
72		PE6	D14[A14/D14]/ D6[A6/D6]	MTIOC6C/TIC1	CTS4#/RTS4#/SS4#	IRQ6	AN014
73		PE5	D13[A13/D13]/ D5[A5/D5]	MTIOC4C/MTIOC2B		IRQ5	AN013/ COMP0
74		PE4	D12[A12/D12]/ D4[A4/D4]	MTIOC4D/MTIOC1A/ MTIOC4A/MTIOC7D		IRQ12	AN012
75		PE3	D11[A11/D11]/ D3[A3/D3]	MTIOC4B/POE8#/ MTIOC1B/TOC3	CTS12#/RTS12#/ SS12#	IRQ11	AN011
76		PE2	D10[A10/D10]/ D2[A2/D2]	MTIOC4A/MTIOC7A/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12	IRQ7-DS	AN010/ CVREFC0
77		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/MTIOC3B	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	IRQ9	AN009/ CMPC00
78		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12	IRQ8	AN008
79		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7	AN023
80		PD6	D6[A6/D6]	MTIC5V/POE4#/ MTIOC8A		IRQ6	AN022
81		PD5	D5[A5/D5]	MTIC5W/POE10#/ MTIOC8C		IRQ5	AN021
82		PD4	D4[A4/D4]	POE11#/MTIOC8B		IRQ4	AN020
83		PD3	D3[A3/D3]	POE8#/MTIOC8D/ TOC2		IRQ3	AN019
84		PD2	D2[A2/D2]	MTIOC4D/TIC2	CRX0-B	IRQ2	AN018
85		PD1	D1[A1/D1]	MTIOC4B/POE0#	CTX0-B	IRQ1	AN017
86		PD0	D0[A0/D0]	POE4#		IRQ0	AN016
87		P47				IRQ15-DS	AN007
88		P46				IRQ14-DS	AN006
89		P45				IRQ13-DS	AN005
90		P44				IRQ12-DS	AN004
91		P43				IRQ11-DS	AN003
92		P42				IRQ10-DS	AN002
93		P41				IRQ9-DS	AN001
94	VREFL0	PJ7					
95		P40				IRQ8-DS	AN000
96	VREFH0	PJ6					
97	AVCC0						
98		P07				IRQ15	ADTRG0#
99	AVSS0						

Table 1.6 List of Pin and Pin Functions (100-Pin LFQFP) (5/5)

Pin No. 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
100		P05				IRQ13	DA1

Note 1. This pin function is not provided for products with no JTAG interface.
Note 2. This pin function is not provided for products with a JTAG interface.
Note 3. This pin function is not provided for products with no sub-clock oscillator.
Note 4. This pin function is not provided for products with a sub-clock oscillator.
Note 5. This pin function is not available in products with no sub-clock oscillator.

1.6.3 80-Pin LFQFP

Table 1.7 List of Pin and Pin Functions (80-Pin LFQFP) (1/4)

Pin No. 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
1		P06				
2		P03			IRQ11	DA0
3		P04				
4	VCL					
5		PJ1	MTIOC3A			
6	MD/FINED	PN6				
7	XCIN*1	PH7*2				
8	XCOUT*1	PH6*2				
9	RES#					
10	XTAL	P37			IRQ4	
11	VSS					
12	EXTAL	P36			IRQ5	
13	VCC					
14		P35			NMI	
15		P34	MTIOC0A/TMCI3/ POE10#	SCK6/SCK0	IRQ4	
16		P32	MTIOC0C/TMO3/ RTCIC2*3/RTCOUT*3/ POE0#/POE10#	TXD6/SMOSI6/ SSDA6/TXD0/ SMOSI0/SSDA0/ CTX0-A	IRQ2-DS	
17		P31	MTIOC4D/TMCI2/ RTCIC1*3	CTS1#/RTS1#/SS1#	IRQ1-DS	
18		P30	MTIOC4B/TMRI3/ RTCIC0*3/POE8#	RXD1/SMISO1/ SSCL1	IRQ0-DS	COMP3
19		P27	MTIOC2B/TMCI3	SCK1	IRQ7	CVREFC3
20		P26	MTIOC2A/TMO1	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#	IRQ6	CMPC30
21		P21	MTIOC1B/TMCI0/ MTIOC4A	RXD0/SMISO0/ SSCL0	IRQ9	
22		P20	MTIOC1A/TMRI0	TXD0/SMOSI0/ SSDA0	IRQ8	
23		P17	MTIOC3A/MTIOC3B/ TMO1/POE8#/ MTIOC4B	SCK1/TXD3/SMOSI3/ SSDA3/MISOA-C/ SDA2	IRQ7	COMP2
24		P16	MTIOC3C/MTIOC3D/ TMO2/RTCOUT*3	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ MOSIA-C/SCL2	IRQ6	ADTRG0#
25		P15	MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/ SSCL1/SCK3/ CRX0-C	IRQ5	CMPC20
26		P14	MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#/ CTX0-C	IRQ4	CVREFC2
27		P13	MTIOC0B/TMO3	SDA0	IRQ3	
28		P12	MTIC5U/TMCI1	SCL0	IRQ2	
29		PH3	MTIOC4D/TMCI0			

Table 1.7 List of Pin and Pin Functions (80-Pin LFQFP) (2/4)

Pin No. 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
30		PH2	MTIOC4C/TMRI0/ TOC1		IRQ1	
31		PH1	MTIOC3D/TMO0/TIC1		IRQ0	ADST0
32		PH0	MTIOC3B/CACREF			ADTRG0#
33		P55	MTIOC4D/MTIOC4A/ TMO3	CRX0-D	IRQ10	
34		P54	MTIOC4B/TMCI1	CTX0-D	IRQ4	
35	UB	PC7	MTIOC3A/MTCLKB/ TMO2/CACREF/TOC0	TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ TXD010-C/ SMOSI010-C/ SSDA010-C/MISOA-A	IRQ14	
36		PC6	MTIOC3C/MTCLKA/ TMCI2/TIC0	RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ RXD010-C/ SMISO010-C/ SSCL010-C/MOSIA-A	IRQ13	
37		PC5	MTIOC3B/MTCLKD/ TMRI2/MTIOC0C	SCK8/SCK10/ SCK010-C/ RSPCKA-A/PMC0	IRQ5	
38		PC4	MTIOC3D/MTCLKC/ TMCI1/POE0#/ MTIOC0A	SCK5/CTS8#/RTS8#/ SS8#/SS10#/CTS10#/ RTS10#/CTS010#-B/ RTS010#-B/ SS010#-B/DE010-B/ SSLA0-A/PMC0	IRQ12	
39		PC3	MTIOC4D	TXD5/SMOSI5/ SSDA5/PMC0	IRQ11	
40		PC2	MTIOC4B	RXD5/SMISO5/ SSCL5/TXDB011-A/ SSLA3-A	IRQ10	
41		PB7	MTIOC3B	TXD9/SMOSI9/ SSDA9/SMOSI11/ SSDA11/TXD11/ TXD011-B/ SMOSI011-B/ SSDA011-B	IRQ15	
42		PB6	MTIOC3D	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ RXD011-B/ SMISO011-B/ SSCL011-B	IRQ6	
43		PB5	MTIOC2A/MTIOC1B/ TMRI1/POE4#/TOC2	SCK9/SCK11/ SCK011-B	IRQ13	
44		PB4		CTS9#/RTS9#/SS9#/ SS11#/CTS11#/ RTS11#/CTS011#-B/ RTS011#-B/ SS011#-B/DE011-B	IRQ4	
45		PB3	MTIOC0A/MTIOC4A/ TMO0/POE11#/TIC2	SCK4/SCK6/PMC0	IRQ3	
46		PB2		CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#	IRQ2	

Table 1.7 List of Pin and Pin Functions (80-Pin LFQFP) (3/4)

Pin No. 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
47		PB1	MTIOC0C/MTIOC4C/ TMCI0	TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6	IRQ4-DS	COMP1
48	VCC					
49		PB0	MTIC5W/MTIOC3D	RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6/ RSPCKA-C	IRQ12	
50	VSS					
51		PA6	MTIC5V/MTCLKB/ TMCI3/POE10#/ MTIOC3D/MTIOC6B	CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/ SS12#/MOSIA-B	IRQ14	
52		PA5	MTIOC6B	RSPCKA-B	IRQ5	
53		PA4	MTIC5U/MTCLKA/ TMRI0/MTIOC4C/ MTIOC7C	TXD5/SMOSI5/ SSDA5/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ SSLA0-B	IRQ5-DS	CVREFC1/ ADST0
54		PA3	MTIOC0D/MTCLKD/ MTIC5V/MTIOC4D	RXD5/SMISO5/ SSCL5	IRQ6-DS	CMPC10
55		PA2	MTIOC7A	RXD5/SMISO5/ SSCL5/RXD12/ SMISO12/SSCL12/ RXDX12/SSLA3-B	IRQ10	
56		PA1	MTIOC0B/MTCLKC/ MTIOC7B/MTIOC3B	SCK5/SCK12/ SSLA2-B	IRQ11	ADTRG0#
57		PA0	MTIOC4A/CACREF/ MTIOC6D	SSLA1-B	IRQ0	
58		PE5	MTIOC4C/MTIOC2B		IRQ5	AN013/COMP0
59		PE4	MTIOC4D/MTIOC1A/ MTIOC4A/MTIOC7D		IRQ12	AN012
60		PE3	MTIOC4B/POE8#/ MTIOC1B/TOC3	CTS12#/RTS12#/ SS12#	IRQ11	AN011
61		PE2	MTIOC4A/MTIOC7A/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12	IRQ7-DS	AN010/ CVREFC0
62		PE1	MTIOC4C/MTIOC3B	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	IRQ9	AN009/ CMPC00
63		PE0	MTIOC3D	SCK12	IRQ8	AN008
64		PD2	MTIOC4D/TIC2	CRX0-B	IRQ2	AN018
65		PD1	MTIOC4B/POE0#	CTX0-B	IRQ1	AN017
66		PD0	POE4#		IRQ0	AN016
67		P47			IRQ15-DS	AN007
68		P46			IRQ14-DS	AN006
69		P45			IRQ13-DS	AN005
70		P44			IRQ12-DS	AN004
71		P43			IRQ11-DS	AN003
72		P42			IRQ10-DS	AN002
73		P41			IRQ9-DS	AN001
74	VREFL0	PJ7				
75		P40			IRQ8-DS	AN000

Table 1.7 List of Pin and Pin Functions (80-Pin LFQFP) (4/4)

Pin No. 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
76	VREFH0	PJ6				
77	AVCC0					
78		P07			IRQ15	ADTRG0#
79	AVSS0					
80		P05			IRQ13	DA1

Note 1. This pin function is not provided for products with no sub-clock oscillator.
Note 2. This pin function is not provided for products with a sub-clock oscillator.
Note 3. This pin function is not available in products with no sub-clock oscillator.

1.6.4 64-Pin LFQFP

Table 1.8 List of Pin and Pin Functions (64-Pin LFQFP) (1/3)

Pin No. 64-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
1		P03			IRQ11	DA0
2	VCL					
3	MD/FINED	PN6				
4	XCIN*1	PH7*2				
5	XCOUT*1	PH6*2				
6	RES#					
7	XTAL	P37			IRQ4	
8	VSS					
9	EXTAL	P36			IRQ5	
10	VCC					
11		P35			NMI	
12		P32	MTIOC0C/TMO3/ RTCIC2*3/RTCOUT*3/ POE0#/POE10#	TXD6/SMOSI6/ SSDA6/CTX0-A	IRQ2-DS	
13		P31	MTIOC4D/TMCI2/ RTCIC1*3	CTS1#/RTS1#/SS1#	IRQ1-DS	
14		P30	MTIOC4B/TMRI3/ RTCIC0*3/POE8#	RXD1/SMISO1/ SSCL1	IRQ0-DS	COMP3
15		P27	MTIOC2B/TMCI3	SCK1	IRQ7	CVREFC3
16		P26	MTIOC2A/TMO1	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#	IRQ6	CMPC30
17		P17	MTIOC3A/MTIOC3B/ TMO1/POE8#/ MTIOC4B	SCK1/TXD3/SMOSI3/ SSDA3/MISOA-C/ SDA2	IRQ7	COMP2
18		P16	MTIOC3C/MTIOC3D/ TMO2/RTCOUT*3	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ MOSIA-C/SCL2	IRQ6	ADTRG0#
19		P15	MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/ SSCL1/SCK3/ CRX0-C	IRQ5	CMPC20
20		P14	MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#/ CTX0-C	IRQ4	CVREFC2
21		PH3	MTIOC4D/TMCI0			
22		PH2	MTIOC4C/TMRI0/ TOC1		IRQ1	
23		PH1	MTIOC3D/TMO0/TIC1		IRQ0	ADST0
24		PH0	MTIOC3B/CACREF			ADTRG0#
25		P55	MTIOC4D/MTIOC4A/ TMO3	CRX0-D	IRQ10	
26		P54	MTIOC4B/TMCI1	CTX0-D	IRQ4	
27	UB	PC7	MTIOC3A/MTCLKB/ TMO2/CACREF/TOC0	TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ TXD010-C/ SMOSI010-C/ SSDA010-C/MISOA-A	IRQ14	

Table 1.8 List of Pin and Pin Functions (64-Pin LFQFP) (2/3)

Pin No. 64-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
28		PC6	MTIOC3C/MTCLKA/ TMCI2/TIC0	RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ RXD010-C/ SMISO010-C/ SSCL010-C/MOSIA-A	IRQ13	
29		PC5	MTIOC3B/MTCLKD/ TMRI2/MTIOC0C	SCK8/SCK10/ SCK010-C/ RSPCKA-A/PMC0	IRQ5	
30		PC4	MTIOC3D/MTCLKC/ TMCI1/POE0#/ MTIOC0A	SCK5/CTS8#/RTS8#/ SS8#/SS10#/CTS10#/ RTS10#/CTS010#-B/ RTS010#-B/ SS010#-B/DE010-B/ SSLA0-A/PMC0	IRQ12	
31		PC3	MTIOC4D	TXD5/SMOSI5/ SSDA5/PMC0	IRQ11	
32		PC2	MTIOC4B	RXD5/SMISO5/ SSCL5/TXDB011-A/ SSLA3-A	IRQ10	
33		PB7	MTIOC3B	TXD9/SMOSI9/ SSDA9/SMOSI11/ SSDA11/TXD11/ TXD011-B/ SMOSI011-B/ SSDA011-B	IRQ15	
34		PB6	MTIOC3D	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ RXD011-B/ SMISO011-B/ SSCL011-B	IRQ6	
35		PB5	MTIOC2A/MTIOC1B/ TMRI1/POE4#/TOC2	SCK9/SCK11/ SCK011-B	IRQ13	
36		PB3	MTIOC0A/MTIOC4A/ TMO0/POE11#/TIC2	SCK4/SCK6/PMC0	IRQ3	
37		PB1	MTIOC0C/MTIOC4C/ TMCI0	TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6	IRQ4-DS	COMP1
38	VCC					
39		PB0	MTIC5W/MTIOC3D	RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6/ RSPCKA-C	IRQ12	
40	VSS					
41		PA6	MTIC5V/MTCLKB/ TMCI3/POE10#/ MTIOC3D/MTIOC6B	CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/ SS12#/MOSIA-B	IRQ14	
42		PA4	MTIC5U/MTCLKA/ TMRI0/MTIOC4C/ MTIOC7C	TXD5/SMOSI5/ SSDA5/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ SSLA0-B	IRQ5-DS	CVREFC1/ ADST0
43		PA3	MTIOC0D/MTCLKD/ MTIC5V/MTIOC4D	RXD5/SMISO5/ SSCL5	IRQ6-DS	CMPC10
44		PA1	MTIOC0B/MTCLKC/ MTIOC7B/MTIOC3B	SCK5/SCK12/ SSLA2-B	IRQ11	ADTRG0#

Table 1.8 List of Pin and Pin Functions (64-Pin LFQFP) (3/3)

Pin No. 64-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TMR, RTC, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, D/A, CMPC
45		PA0	MTIOC4A/CACREF/ MTIOC6D	SSLA1-B	IRQ0	
46		PE5	MTIOC4C/MTIOC2B		IRQ5	AN013/COMP0
47		PE4	MTIOC4D/MTIOC1A/ MTIOC4A/MTIOC7D		IRQ12	AN012
48		PE3	MTIOC4B/POE8#/ MTIOC1B/TOC3	CTS12#/RTS12#/ SS12#	IRQ11	AN011
49		PE2	MTIOC4A/MTIOC7A/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12	IRQ7-DS	AN010/ CVREFC0
50		PE1	MTIOC4C/MTIOC3B	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	IRQ9	AN009/ CMPC00
51		PE0	MTIOC3D	SCK12	IRQ8	AN008
52		P47			IRQ15-DS	AN007
53		P46			IRQ14-DS	AN006
54		P45			IRQ13-DS	AN005
55		P44			IRQ12-DS	AN004
56		P43			IRQ11-DS	AN003
57		P42			IRQ10-DS	AN002
58		P41			IRQ9-DS	AN001
59	VREFL0	PJ7				
60		P40			IRQ8-DS	AN000
61	VREFH0	PJ6				
62	AVCC0					
63		P07			IRQ15	ADTRG0#
64	AVSS0					

Note 1. This pin function is not provided for products with no sub-clock oscillator.
Note 2. This pin function is not provided for products with a sub-clock oscillator.
Note 3. This pin function is not available in products with no sub-clock oscillator.

1.6.5 48-Pin LFQFP

Table 1.9 List of Pin and Pin Functions (48-Pin LFQFP) (1/2)

Pin No. 48-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TMR, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, CMPC
1	VCL					
2	MD/FINED	PN6				
3	RES#					
4	XTAL	P37			IRQ4	
5	VSS					
6	EXTAL	P36			IRQ5	
7	VCC					
8		P35			NMI	
9		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS	
10		P30	MTIOC4B/POE8#	RXD1/SMISO1/ SSCL1	IRQ0-DS	COMP3
11		P27	MTIOC2B	SCK1	IRQ7	CVREFC3
12		P26	MTIOC2A/TMO1	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#/SS3#	IRQ6	CMPC30
13		P17	MTIOC3A/MTIOC3B/ TMO1/POE8#/ MTIOC4B	SCK1/TXD3/SMOSI3/ SSDA3/MISOA-C/ SDA2	IRQ7	COMP2
14		P16	MTIOC3C/MTIOC3D/ TMO2	TXD1/SMOSI1/ SSDA1/RXD3/ SMISO3/SSCL3/ MOSIA-C/SCL2	IRQ6	ADTRG0#
15		P15	MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/ SSCL1/SCK3/ CRX0-C	IRQ5	CMPC20
16		P14	MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#/ CTX0-C	IRQ4	CVREFC2
17		PH3	MTIOC4D/TMCI0			
18		PH2	MTIOC4C/TMRI0/ TOC1		IRQ1	
19		PH1	MTIOC3D/TMO0/TIC1		IRQ0	ADST0
20		PH0	MTIOC3B/CACREF			ADTRG0#
21	UB	PC7	MTIOC3A/MTCLKB/ TMO2/CACREF/TOC0	TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ TXD010-C/ SMOSI010-C/ SSDA010-C/MISOA-A	IRQ14	
22		PC6	MTIOC3C/MTCLKA/ TMCI2/TIC0	RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ RXD010-C/ SMISO010-C/ SSCL010-C/MOSIA-A	IRQ13	
23		PC5	MTIOC3B/MTCLKD/ TMRI2/MTIOC0C	SCK8/SCK10/ SCK010-C/ RSPCKA-A/PMC0	IRQ5	

Table 1.9 List of Pin and Pin Functions (48-Pin LFQFP) (2/2)

Pin No. 48-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, TMR, POE, CAC, CMTW)	Communication (SCI, RSCI, RSPI, RIIC, CANFD, REMC)	Interrupt (IRQ, NMI)	A/D, CMPC
24		PC4	MTIOC3D/MTCLKC/ TMCI1/POE0#/ MTIOC0A	SCK5/CTS8#/RTS8#/ SS8#/SS10#/CTS10#/ RTS10#/CTS010#-B/ RTS010#-B/ SS010#-B/DE010-B/ SSLA0-A/PMC0	IRQ12	
25		PB5	MTIOC2A/MTIOC1B/ TMRI1/POE4#/TOC2		IRQ13	
26		PB3	MTIOC0A/MTIOC4A/ TMO0/POE11#/TIC2	SCK4/SCK6/PMC0	IRQ3	
27		PB1	MTIOC0C/MTIOC4C/ TMCI0	TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6	IRQ4-DS	COMP1
28	VCC					
29		PB0	MTIC5W/MTIOC3D	RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6/ RSPCKA-C	IRQ12	
30	VSS					
31		PA6	MTIC5V/MTCLKB/ POE10#/MTIOC3D	CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/ SS12#/MOSIA-B	IRQ14	
32		PA4	MTIC5U/MTCLKA/ TMRI0/MTIOC4C/ MTIOC7C	TXD5/SMOSI5/ SSDA5/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ SSLA0-B	IRQ5-DS	CVREFC1/ ADST0
33		PA3	MTIOC0D/MTCLKD/ MTIC5V/MTIOC4D	RXD5/SMISO5/ SSCL5	IRQ6-DS	CMPC10
34		PA1	MTIOC0B/MTCLKC/ MTIOC7B/MTIOC3B	SCK5/SCK12/ SSLA2-B	IRQ11	ADTRG0#
35		PE4	MTIOC4D/MTIOC1A/ MTIOC4A/MTIOC7D		IRQ12	AN012
36		PE3	MTIOC4B/POE8#/ MTIOC1B/TOC3	CTS12#/RTS12#/ SS12#	IRQ11	AN011
37		PE2	MTIOC4A/MTIOC7A/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12	IRQ7-DS	AN010/ CVREFC0
38		PE1	MTIOC4C/MTIOC3B	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	IRQ9	AN009/ CMPC00
39		P47			IRQ15-DS	AN007
40		P46			IRQ14-DS	AN006
41		P45			IRQ13-DS	AN005
42		P42			IRQ10-DS	AN002
43		P41			IRQ9-DS	AN001
44	VREFL0	PJ7				
45		P40			IRQ8-DS	AN000
46	VREFH0	PJ6				
47	AVCC0					
48	AVSS0					

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Conditions: VSS = AVSS0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Analog power supply voltage		AVCC0*1	–0.3 to +6.5	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3 (up to 6.5)	V
Input voltage	P12, P13, P16, P17	V_{in}	–0.3 to +6.5	V
	P03, P05 to P7, P40 to P47, PJ6, PJ7		–0.3 to AVCC0 + 0.3 (up to 6.5)	
	Other than above		–0.3 to VCC + 0.3 (up to 6.5)	
Junction temperature		T_j	–40 to +125	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Insert capacitors of high frequency characteristics between the AVCC0 and AVSS0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

2.2 Recommended Operating Conditions

Table 2.2 Recommended Operating Conditions (1)

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply voltage*1		VCC	2.7	—	5.5	V
		VSS	—	0	—	
Analog power supply voltage*1, *2		AVCC0	3.0	—	5.5	V
		AVSS0	—	0	—	
		VREFH0	AVCC0 – 1.0	—	AVCC0	
		VREFL0	—	0	—	
Input voltage	P12, P13, P16, P17	V_{in}	–0.3	—	5.8	V
	P03, P05 to P7, P40 to P47, PJ6, PJ7		–0.3	—	AVCC0 + 0.3	
	Other than above		–0.3	—	VCC + 0.3	
Operating temperature	D version	T_{opr}	–40	—	85	°C
	G version		–40	—	105	
Junction temperature	D version	T_j	–40	—	105	°C
	G version		–40	—	125	

Note 1. Comply with the following potential condition: VCC ≤ AVCC0

Note 2. For details, see section 38.6.10, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.

Table 2.3 Recommended Operating Conditions (2)

Item	Symbol	Value
Decoupling capacitance to stabilize the internal voltage	C_{VCL}	0.47 µF ± 30%*1

Note 1. Use a multilayer ceramic capacitor whose nominal capacitance is 0.47 µF and a capacitance tolerance is ±30% or better.

2.3 DC Characteristics

Table 2.4 DC Characteristics (1)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin MTU input pin POE input pin TMR input pin CMTW input pin RTC input pin SCI input pin CANFD input pin REMC input pin ADTRG# input pin RES#, NMI	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	0.7 × VCC	—	—		
		V_{IL}	—	—	0.3 × VCC		
		ΔV_T	0.05 × VCC	—	—		
	Ports for 5 V tolerant (P12, P13, P16, P17)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	Other input pins excluding ports for 5 V tolerant	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
High level input voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	0.9 × VCC	—	—	V	
	EXTAL, RSPI input pin, WAIT#		0.8 × VCC	—	—		
	D0 to D15		0.7 × VCC	—	—		
	RIIC (SMBus)		2.1	—	—		
Low level input voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	—	—	0.1 × VCC	V	
	EXTAL, RSPI input pin, WAIT#		—	—	0.2 × VCC		
	D0 to D15		—	—	0.3 × VCC		
	RIIC (SMBus)		—	—	0.8		

Table 2.5 DC Characteristics (2)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	P03, P05 to P7, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.5	—	—	V	I_{OH} = –1 mA
	Other than above		VCC – 0.5	—	—		
Output low voltage	RIIC pins	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	Other than above		—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES#, EMLE	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	RIIC pins	$\lvert I_{TSI} \rvert$	—	—	5.0	µA	V_{in} = 0 V V_{in} = VCC
	Other than above		—	—	1.0		
Input pull-up resistors	P03, P05 to P7, P40 to P47, PJ6, PJ7	R_{PU}	10	—	100	kΩ	AVCC0 = 3.0 to 5.5 V V_{in} = 0 V
	Other than above		10	—	100		VCC = 2.7 to 5.5 V V_{in} = 0 V
Input pull-down resistors	EMLE	R_{PD}	5	—	50	kΩ	V_{in} = VCC = AVCC0
Input capacitance	RIIC pins	C_{in}	—	—	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	PJ6, PJ7		—	—	12		
	Other than above		—	—	8		
Output voltage of the VCL pin		V_{CL}	—	1.25	—	V	

Table 2.6 DC Characteristics (3)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item				Symbol	D version		G version		Unit	Test Conditions
					Typ.	Max.	Typ.	Max.		
Supply current*1	Normal operating mode	Full operation		I_{CC}*2	—	68	—	76	mA	ICLK = 120 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKD = 60 MHz, FCLK = 60 MHz, BCLK = 60 MHz, BCLK pin = 30 MHz
		Normal operation	Peripheral module clocks are supplied		21	—	21	—		
			Peripheral module clocks are stopped		12	—	12	—		
		CoreMark	Peripheral module clocks are stopped		19	—	19	—		
		Sleep mode	Peripheral module clocks are supplied		16	36	16	44		
		All module clock stop mode			7.8	24	7.8	32		
		Increased by BGO operation*3	Reading from the code flash memory while the data flash memory is being programmed		12	—	12	—		
	Software standby mode				0.9	9	0.9	14	mA	
	Deep software standby mode				15	23	15	32	µA	
		Increase current by operating RTC			2.6	—	2.6	—		When a standard C_L crystal is in use

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. I_{CC} depends on the f (ICLK) as follows.
- D version
  I_{CC} max = 0.500 × f + 8 (full operation in normal operating mode)
  I_{CC} typ = 0.144 × f + 4 (normal operation in normal operating mode)
  I_{CC} max = 0.234 × f + 8 (sleep mode)
- G version
  I_{CC} max = 0.534 × f + 12 (full operation in normal operating mode)
  I_{CC} typ = 0.144 × f + 4 (normal operation in normal operating mode)
  I_{CC} max = 0.267 × f + 12 (sleep mode)

Note 3. This is an increase caused by programming/erasing of the data flash memory during execution of the user program from the code flash memory.

Table 2.7 DC Characteristics (4)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

	Item				Symbol	Typ.	Max.	Unit
	A/D	D/A (2 channels)	CMPC (4 channels)	TEMPS				
Analog power supply current	During conversion	Waiting for conversion	Waiting	Waiting	A_{ICC}	0.9	1.4	mA
	Waiting for conversion	During conversion	Waiting	Waiting		0.6	0.8	
	Waiting for conversion	Waiting for conversion	During operation	Waiting		0.4	0.5	
	During conversion	Waiting for conversion	Waiting	During operation		1.0	1.5	
	When waiting					0.4	7.7	µA
	In the module-stop state					0.4	6.5	

Table 2.8 DC Characteristics (5)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM retension voltage		V_{RAM}	2.7	—	—	V	
VCC ramp rate at power-on	At normal startup	SrVCC	0.02	—	8	ms/V	Figure 2.1
	Voltage monitoring 0 reset enabled at startup*1, *2		0.02	—	20		
VCC ramp rate at power fluctuation		dt/dVCC	1.0	—	—		When VCC change exceeds VCC ±10%

Note 1. When OFS1.LVDAS = 0.
Note 2. Settings of the OFS1 register are not read in boot mode or user boot mode, so turn on the power supply voltage with a ramp rate at normal startup.

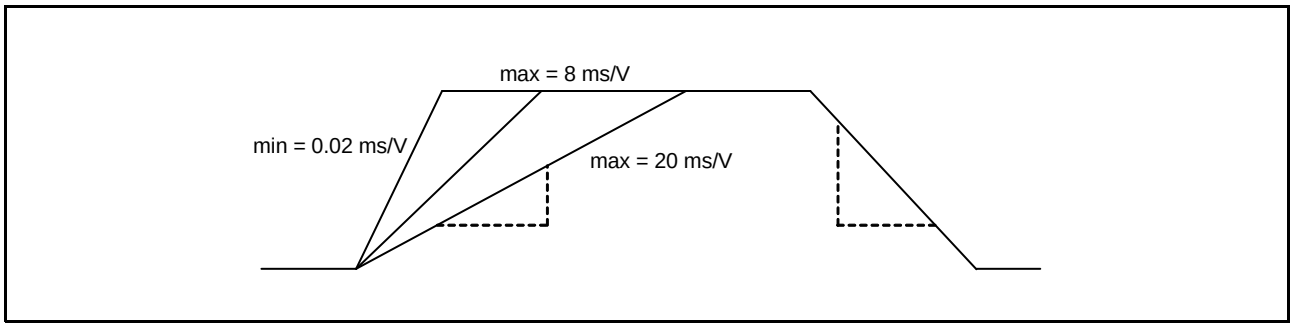


Figure 2.1 VCC Ramp Rate at Power-On

Table 2.9 Permissible Output Currents

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive		—	—	3.8	
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive		—	—	7.6	
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–2.0	mA
	All output pins*2	High drive		—	—	–3.8	
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–4.0	mA
	All output pins*2	High drive		—	—	–7.6	
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	–80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.
Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.
Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Table 2.10 Standard Output Characteristics (1)

Conditions: VCC = AVCC0 = 5.0 V,
VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	Normal drive output	V_{OH}	—	4.97	—	V	I_{OH} = –0.5 mA
			—	4.94	—		I_{OH} = –1.0 mA
			—	4.87	—		I_{OH} = –2.0 mA
			—	4.74	—		I_{OH} = –4.0 mA
	High-drive output		—	4.98	—		I_{OH} = –0.5 mA
			—	4.97	—		I_{OH} = –1.0 mA
			—	4.94	—		I_{OH} = –2.0 mA
			—	4.87	—		I_{OH} = –4.0 mA
Output low voltage	Normal drive output	V_{OL}	—	0.02	—	V	I_{OL} = 0.5 mA
			—	0.04	—		I_{OL} = 1.0 mA
			—	0.09	—		I_{OL} = 2.0 mA
			—	0.18	—		I_{OL} = 4.0 mA
	High-drive output		—	0.01	—		I_{OL} = 0.5 mA
			—	0.03	—		I_{OL} = 1.0 mA
			—	0.05	—		I_{OL} = 2.0 mA
			—	0.10	—		I_{OL} = 4.0 mA

Table 2.11 Standard Output Characteristics (2)

Conditions: VCC = AVCC0 = 3.3V,
VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	Normal drive output	V_{OH}	—	3.26	—	V	I_{OH} = –0.5 mA
			—	3.22	—		I_{OH} = –1.0 mA
			—	3.13	—		I_{OH} = –2.0 mA
			—	2.94	—		I_{OH} = –4.0 mA
	High-drive output		—	3.28	—		I_{OH} = –0.5 mA
			—	3.26	—		I_{OH} = –1.0 mA
			—	3.22	—		I_{OH} = –2.0 mA
			—	3.13	—		I_{OH} = –4.0 mA
Output low voltage	Normal drive output	V_{OL}	—	0.03	—	V	I_{OL} = 0.5 mA
			—	0.06	—		I_{OL} = 1.0 mA
			—	0.12	—		I_{OL} = 2.0 mA
			—	0.25	—		I_{OL} = 4.0 mA
	High-drive output		—	0.02	—		I_{OL} = 0.5 mA
			—	0.03	—		I_{OL} = 1.0 mA
			—	0.07	—		I_{OL} = 2.0 mA
			—	0.13	—		I_{OL} = 4.0 mA

Table 2.12 Thermal Resistance Value (Reference)

Item	Package	Symbol	Max.	Unit	Test Conditions
Thermal resistance	144-pin LFQFP (PLQP0144KA-B)	θ_{ja}	52.1	°C/W	JESD51-2 and JESD51-7 compliant T_a = 105°C
	100-pin LFQFP (PLQP0100KB-B)		51.3		
	80-pin LFQFP (PLQP0080KB-B)		52.0		
	64-pin LFQFP (PLQP0064KB-C)		50.8		
	48-pin LFQFP (PLQP0048KB-B)		58.4		
	144-pin LFQFP (PLQP0144KA-B)	Ψ_{jt}	1.3	°C/W	JESD51-2 and JESD51-7 compliant
	100-pin LFQFP (PLQP0100KB-B)		1.3		
	80-pin LFQFP (PLQP0080KB-B)		1.3		
	64-pin LFQFP (PLQP0064KB-C)		1.3		
	48-pin LFQFP (PLQP0048KB-B)		1.8		

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

2.4 AC Characteristics

Table 2.13 Operating Frequency

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Operating frequency	System clock (ICLK)	f	—	—	120	MHz	
	Peripheral module clock (PCLKA)		—	—	120		
	Peripheral module clock (PCLKB)		—	—	60		
	Peripheral module clock (PCLKD)		—*1	—	60		
	Flash-IF clock (FCLK)		—*2	—	60		
	External bus clock (BCLK)		—	—	60		
	BCLK pin output		—	—	40		VCC ≥ 4.5 V, High-drive output is selected in the driving ability control register.
			—	—	32		VCC < 4.5 V, High-drive output is selected in the driving ability control register.

Note 1. When the 12-bit A/D converter is to be used, the frequency of PCLKD must be set to at least 8 MHz.
Note 2. The FCLK must run at a frequency of at least 4 MHz when the contents of flash memory are to be changed.

2.4.1 Reset Timing

Table 2.14 Reset Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2.0	—	—	ms	Figure 2.2
	Deep software standby mode	t_{RESWD}	0.6	—	—	ms	Figure 2.3
	Software standby mode	t_{RESWS}	0.3	—	—	ms	
	Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Waiting time after release from the RES# pin reset		t_{RESWT}	62	—	63	t_{Lcyc}	Figure 2.2
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	108	—	116	t_{Lcyc}	

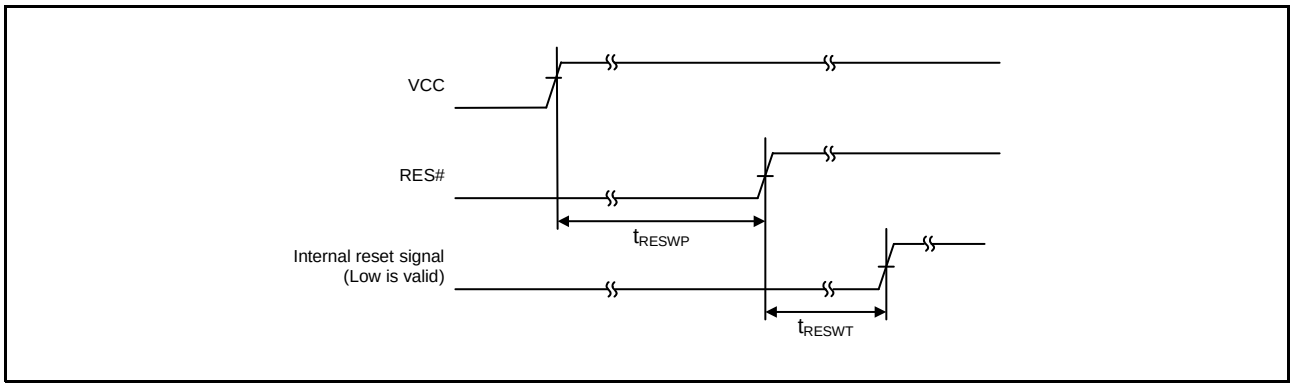


Figure 2.2 Reset Input Timing at Power-On

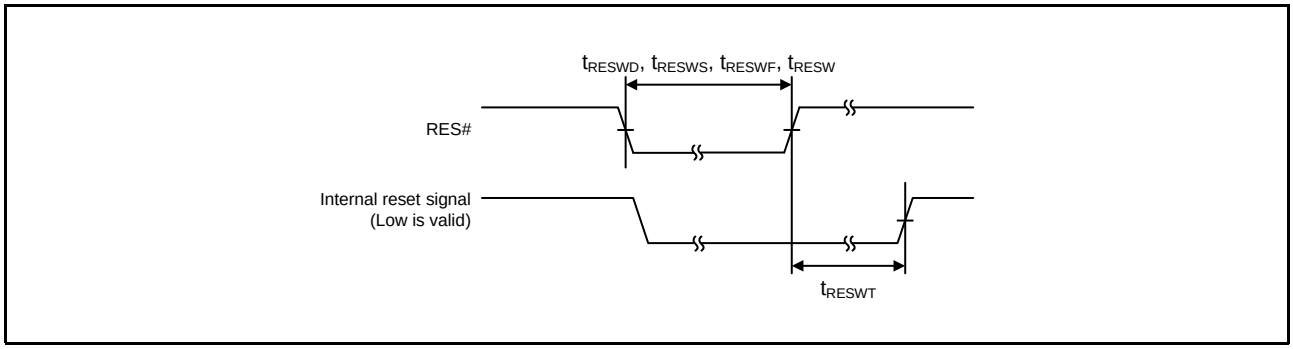


Figure 2.3 Reset Input Timing

2.4.2 Clock Timing

Table 2.15 BCLK Pin Output Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
BCLK pin output cycle time	t_{Bcyc}	25	—	—	ns	VCC ≥ 4.5 V	Figure 2.4
		31.25	—	—		VCC < 4.5 V	
BCLK pin output high pulse width	t_{CH}	7.5	—	—	ns	VCC ≥ 4.5 V	
		10.625	—	—		VCC < 4.5 V	
BCLK pin output low pulse width	t_{CL}	7.5	—	—	ns	VCC ≥ 4.5 V	
		10.625	—	—		VCC < 4.5 V	
BCLK pin output rising time	t_{Cr}	—	—	5	ns		
BCLK pin output falling time	t_{Cf}	—	—	5	ns		

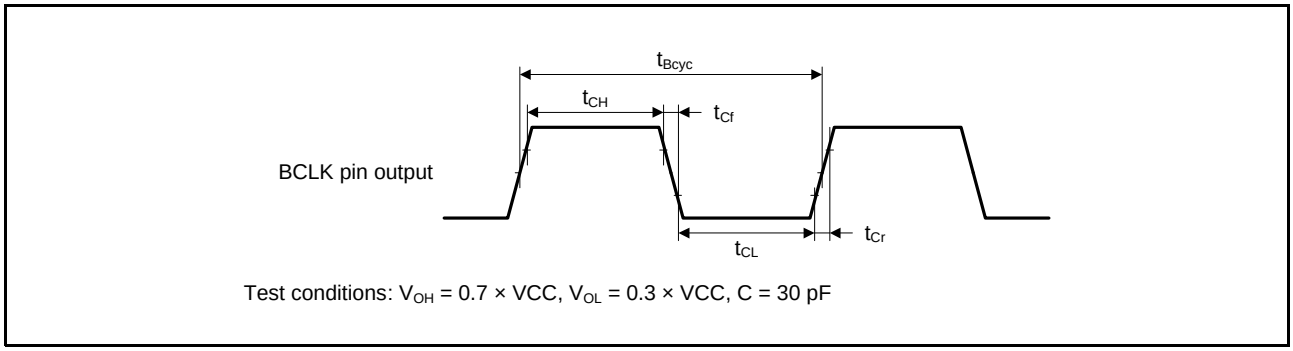


Figure 2.4 BCLK Pin Output Timing

Table 2.16 EXTAL Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 2.5
EXTAL external clock input frequency	f_{EXMAIN}	—	—	24	MHz	
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

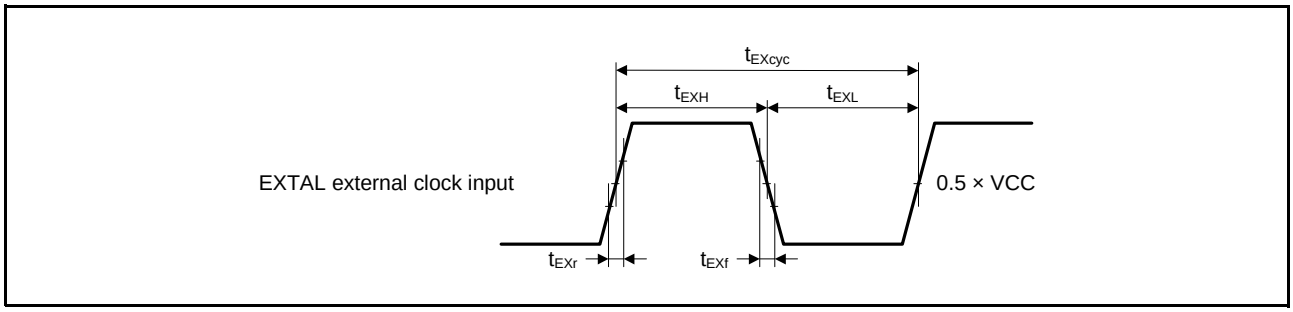


Figure 2.5 EXTAL External Clock Input Timing

Table 2.17 Main Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 2.6
Main clock oscillation stabilization waiting time (crystal)	$t_{MAINOSCWT}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization waiting time in accord with the formula below.

$t_{MAINOSCWT}$ = [(MSTS[7:0] bits × 32) + 10] / f_{LOCO}

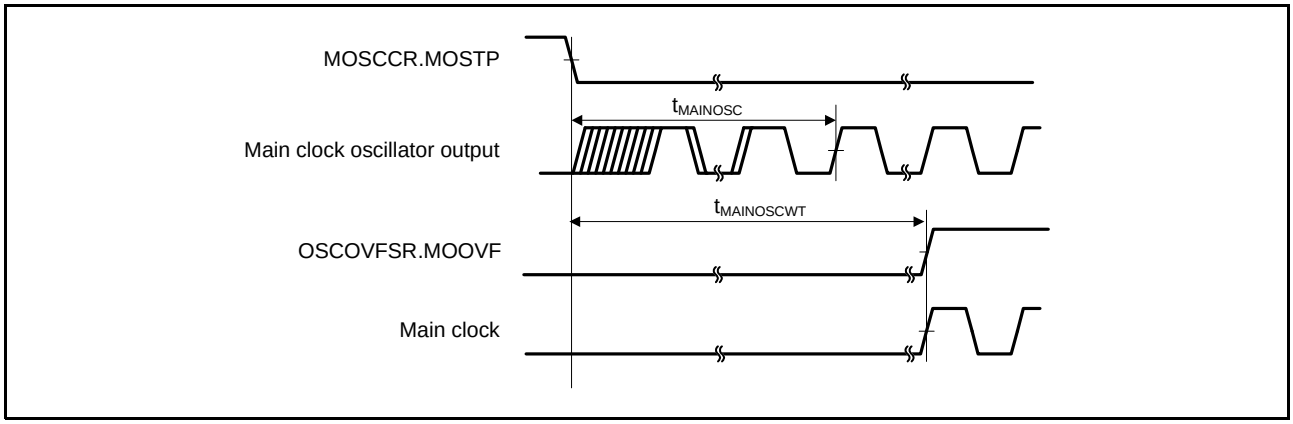


Figure 2.6 Main Clock Oscillation Start Timing

Table 2.18 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	3.78	4.16	4.63	µs	
LOCO clock oscillation frequency	f_{LOCO}	216 (–10%)	240	264 (+10%)	kHz	
LOCO clock oscillation stabilization waiting time	t_{LOCOWT}	—	—	44	µs	Figure 2.7
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	7.57	8.33	9.26	µs	
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108 (–10%)	120	132 (+10%)	kHz	
IWDT-dedicated low-speed clock oscillation stabilization waiting time	$t_{ILOCOWT}$	—	142	190	µs	Figure 2.8

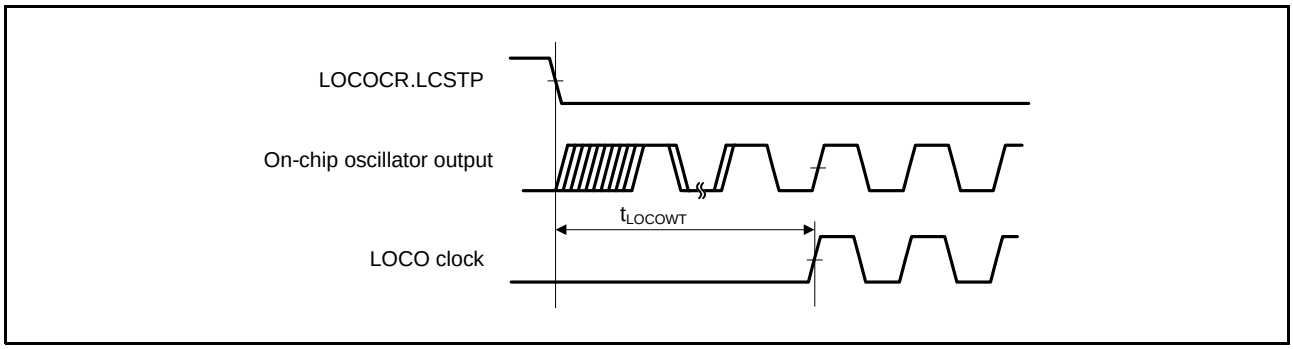


Figure 2.7 LOCO Clock Oscillation Start Timing

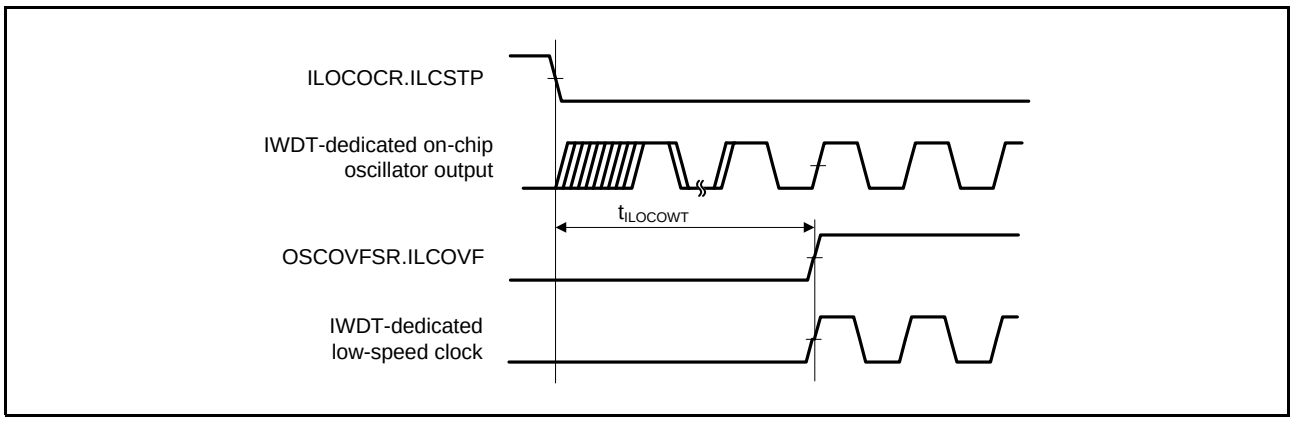


Figure 2.8 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

Table 2.19 HOCO Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	FLL not in use	f_{HOCO}	15.84 (–1.0%)	16	16.16 (+1.0%)	MHz	–20°C ≤ T_a
			17.82 (–1.0%)	18	18.18 (+1.0%)		
			19.80 (–1.0%)	20	20.20 (+1.0%)		
			15.68 (–2.0%)	16	16.16 (+1.0%)		T_a < –20°C
			17.64 (–2.0%)	18	18.18 (+1.0%)		
			19.60 (–2.0%)	20	20.20 (+1.0%)		
	FLL in use	f_{HOCO}	15.960 (–0.25%)	16	16.040 (+0.25%)	MHz	Sub-clock frequency precision: ±50 ppm
			17.955 (–0.25%)	18	18.045 (+0.25%)		
			19.950 (–0.25%)	20	20.050 (+0.25%)		
HOCO clock oscillation stabilization waiting time		t_{HOCOWT}	—	105	149	µs	Figure 2.9
HOCO clock power supply stabilization time		t_{HOCOP}	—	—	150	µs	Figure 2.10
FLL stabilization waiting time		t_{FLLWT}	—	—	1.8	ms	

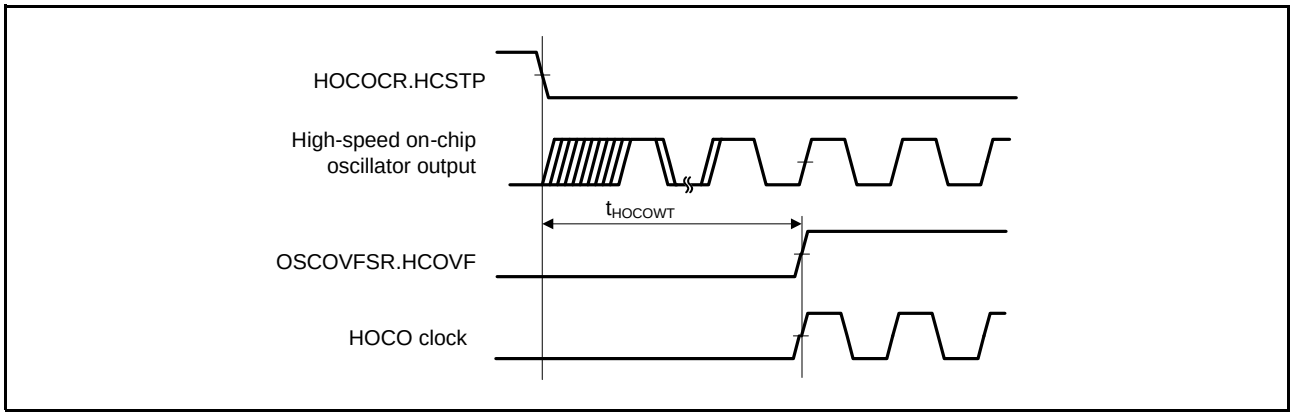


Figure 2.9 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

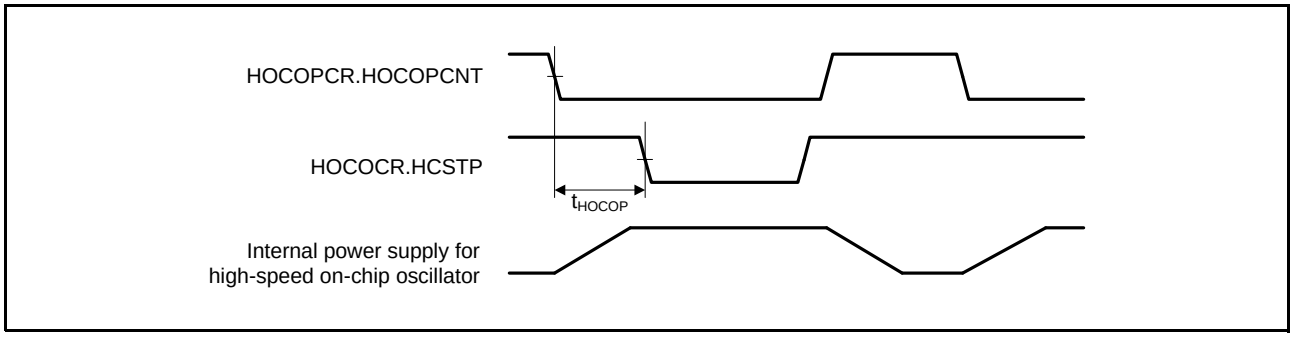


Figure 2.10 High-Speed On-Chip Oscillator Power Supply Control Timing

Table 2.20 PLL Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL clock oscillation frequency	f_{PLL}	120	—	240	MHz	
PLL clock oscillation stabilization waiting time	t_{PLLWT}	—	259	320	µs	Figure 2.11

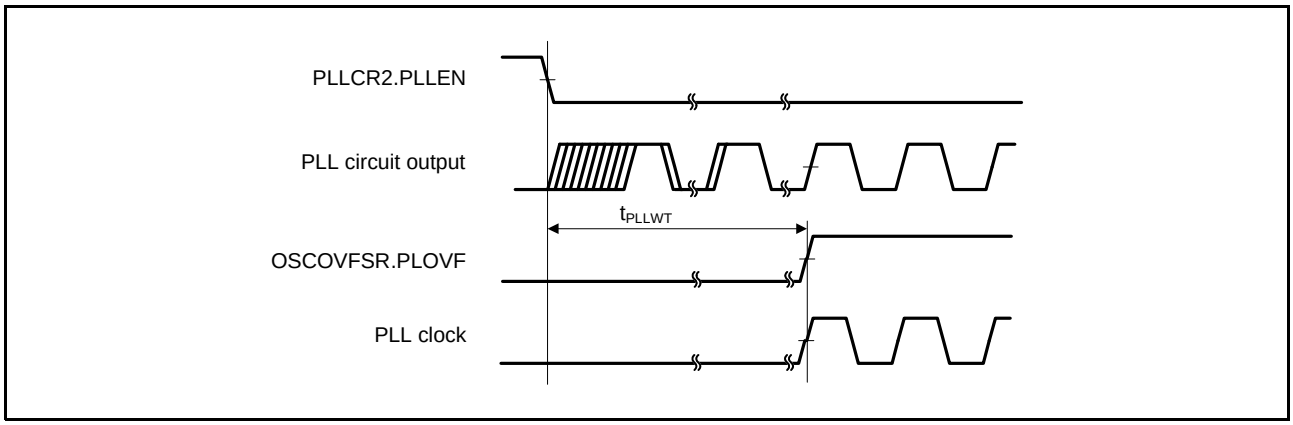


Figure 2.11 PLL Clock Oscillation Start Timing

Table 2.21 Sub-Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillation frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time	t_{SUBOSC}	—	—	*1	s	Figure 2.12
Sub-clock oscillation stabilization waiting time	$t_{SUBOSCWT}$	—	—	*2	s	

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the SOSCWTCR.SSTS[7:0] bits determines the sub-clock oscillation stabilization waiting time in accord with the formula below.
$t_{SUBOSCWT}$ = [(SSTS[7:0] bits × 16384) + 10] / f_{LOCO}

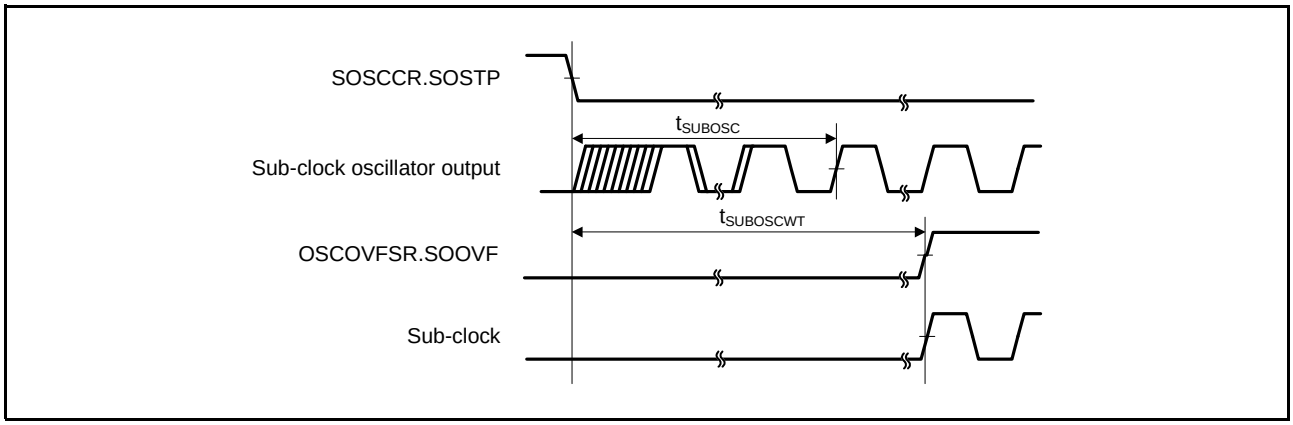


Figure 2.12 Sub-Clock Oscillation Start Timing

2.4.3 Timing of Recovery from Low Power Consumption Modes

Table 2.22 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.		Unit	Test Conditions
						$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time from software standby mode *1	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	—	—	{(MSTS[7:0] bit × 32) + 76} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{MAIN}	µs	Figure 2.13
		Main clock oscillator and PLL circuit operating	t_{SBYPC}			{(MSTS[7:0] bit × 32) + 138} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}			352	100 + 7 / f_{ICLK} + 2n / f_{EXMAIN}		
		Main clock oscillator and PLL circuit operating	t_{SBYPE}			639	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Sub-clock oscillator operating		t_{SBYSC}			{(SSTS[7:0] bit × 16384) + 13} / 0.216 + 10 / f_{FCLK}	100 + 4 / f_{ICLK} + 2n / f_{SUE}		
	High-speed on-chip oscillator operating	High-speed on-chip oscillator operating	t_{SBYHO}			454	100 + 7 / f_{ICLK} + 2n / f_{HOCO}		
		High-speed on-chip oscillator operating and PLL circuit operating	t_{SBYPH}			741	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Low-speed on-chip oscillator operating*4		t_{SBYLO}			338	100 + 7 / f_{ICLK} + 2n / f_{LOCO}		

Note 1. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when f_{ICLK}:f_{FCLK} = 1:1, 2:1, or 4:1.

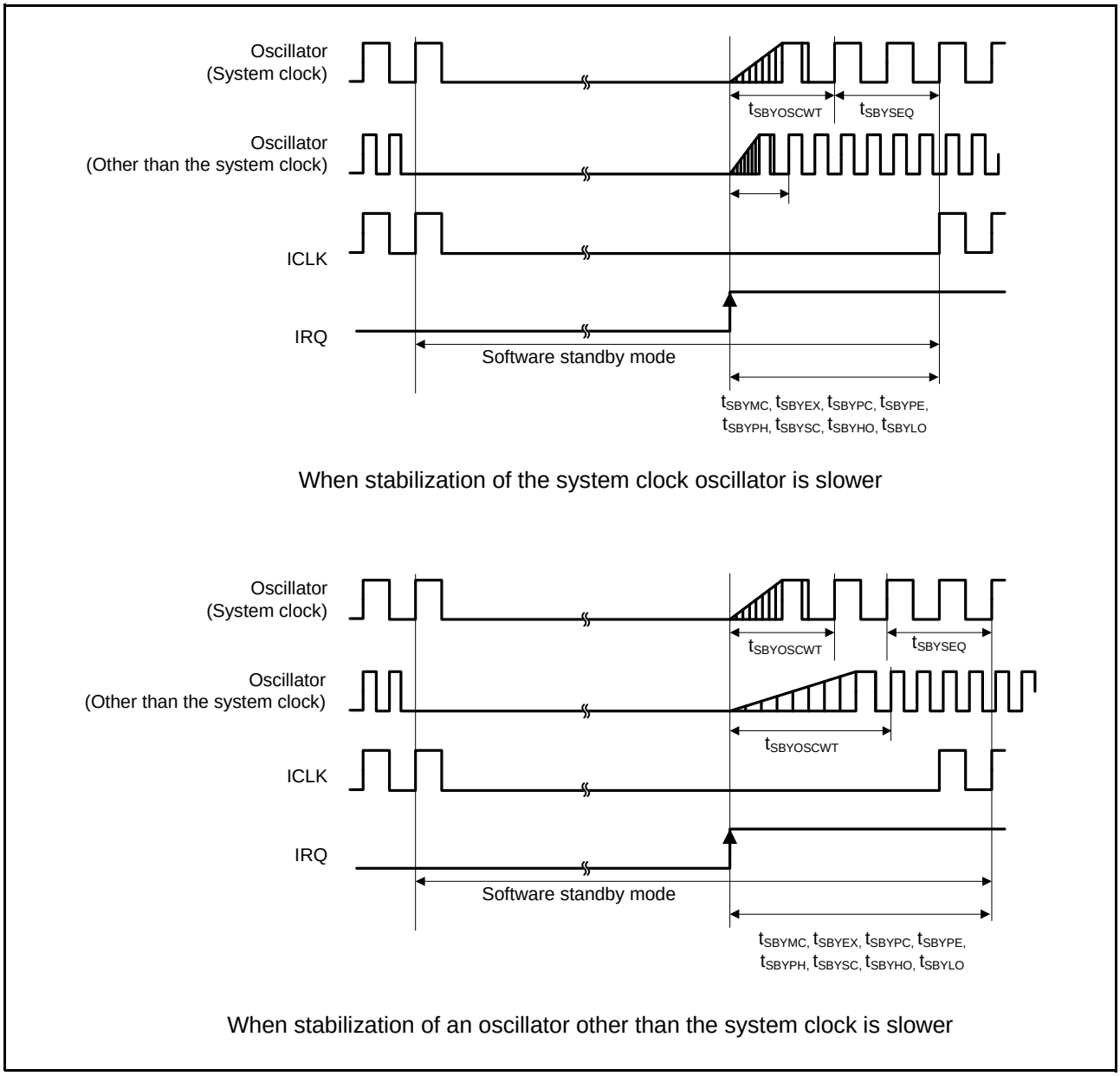


Figure 2.13 Software Standby Mode Recovery Timing

Table 2.23 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep software standby mode	t_{DSBY}	—	—	0.9	ms	Figure 2.14
Waiting time after recovery from deep software standby mode	t_{DSBYWT}	31	—	32	t_{Lcyc}	

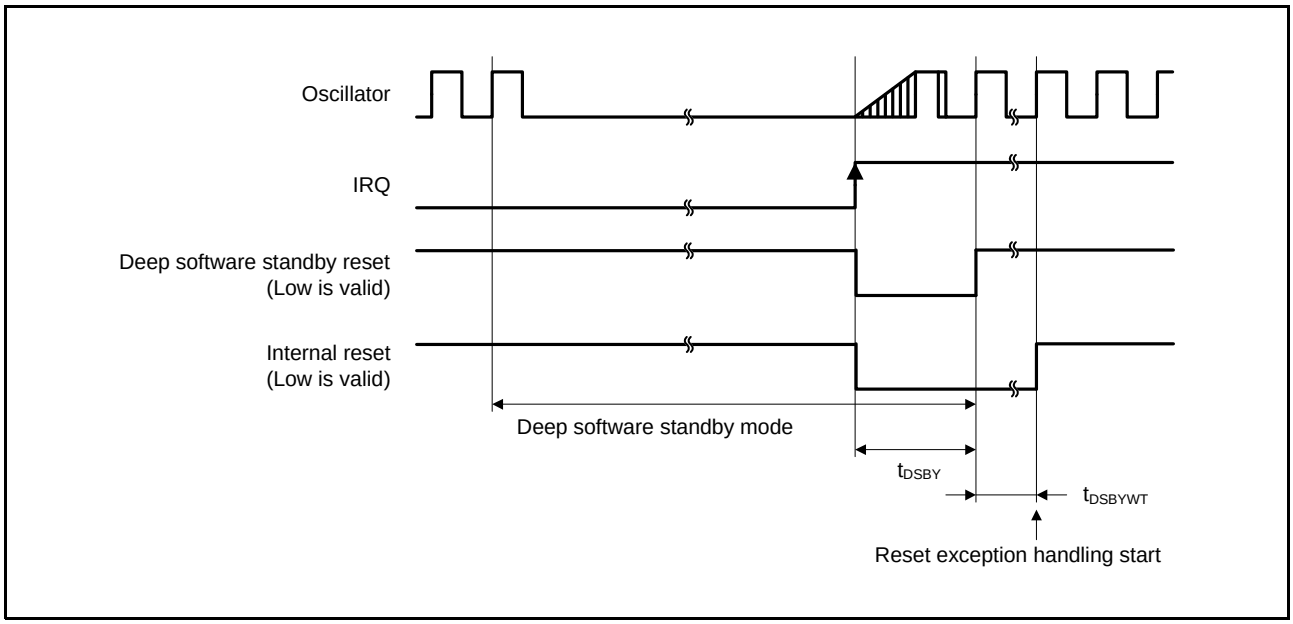


Figure 2.14 Deep Software Standby Mode Recovery Timing

2.4.4 Control Signal Timing

Table 2.24 Control Signal Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	$2 \times t_{PBcyc} \leq 200$ ns, Figure 2.15
		$2 \times t_{PBcyc}$	—	—		$2 \times t_{PBcyc} > 200$ ns, Figure 2.15
IRQ pulse width	t_{IRQW}	200	—	—	ns	$2 \times t_{PBcyc} \leq 200$ ns, Figure 2.16
		$2 \times t_{PBcyc}$	—	—		$2 \times t_{PBcyc} > 200$ ns, Figure 2.16

Note 1. t_{PBcyc}: PCLKB cycle

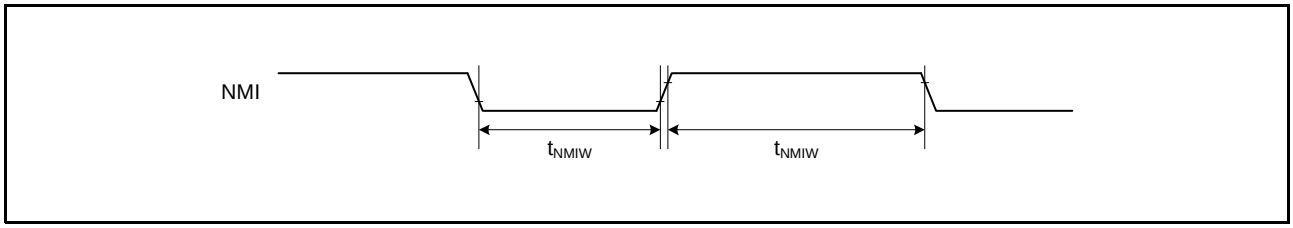


Figure 2.15 NMI Interrupt Input Timing

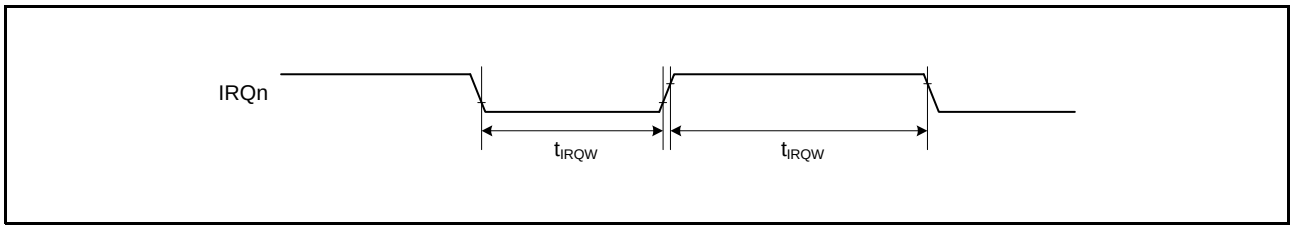


Figure 2.16 IRQ Interrupt Input Timing

2.4.5 Bus Timing

Table 2.25 Bus Timing (1)

Conditions: 4.5 V ≤ VCC ≤ 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	12.5	ns	Figure 2.17 to Figure 2.22
Byte control delay time	t_{BCD}	—	12.5	ns	
CS# delay time	t_{CSD}	—	12.5	ns	
ALE delay time	t_{ALED}	—	12.5	ns	
RD# delay time	t_{RSD}	—	12.5	ns	
Read data setup time	t_{RDS}	12.5	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	12.5	ns	
Write data delay time	t_{WDD}	—	12.5	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	12.5	—	ns	Figure 2.23
WAIT# hold time	t_{WTH}	0	—	ns	

Table 2.26 Bus Timing (2)

Conditions: 2.7 V ≤ VCC < 4.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	25	ns	Figure 2.17 to Figure 2.22
Byte control delay time	t_{BCD}	—	25	ns	
CS# delay time	t_{CSD}	—	25	ns	
ALE delay time	t_{ALED}	—	25	ns	
RD# delay time	t_{RSD}	—	25	ns	
Read data setup time	t_{RDS}	25	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	25	ns	
Write data delay time	t_{WDD}	—	25	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	25	—	ns	Figure 2.23
WAIT# hold time	t_{WTH}	0	—	ns	

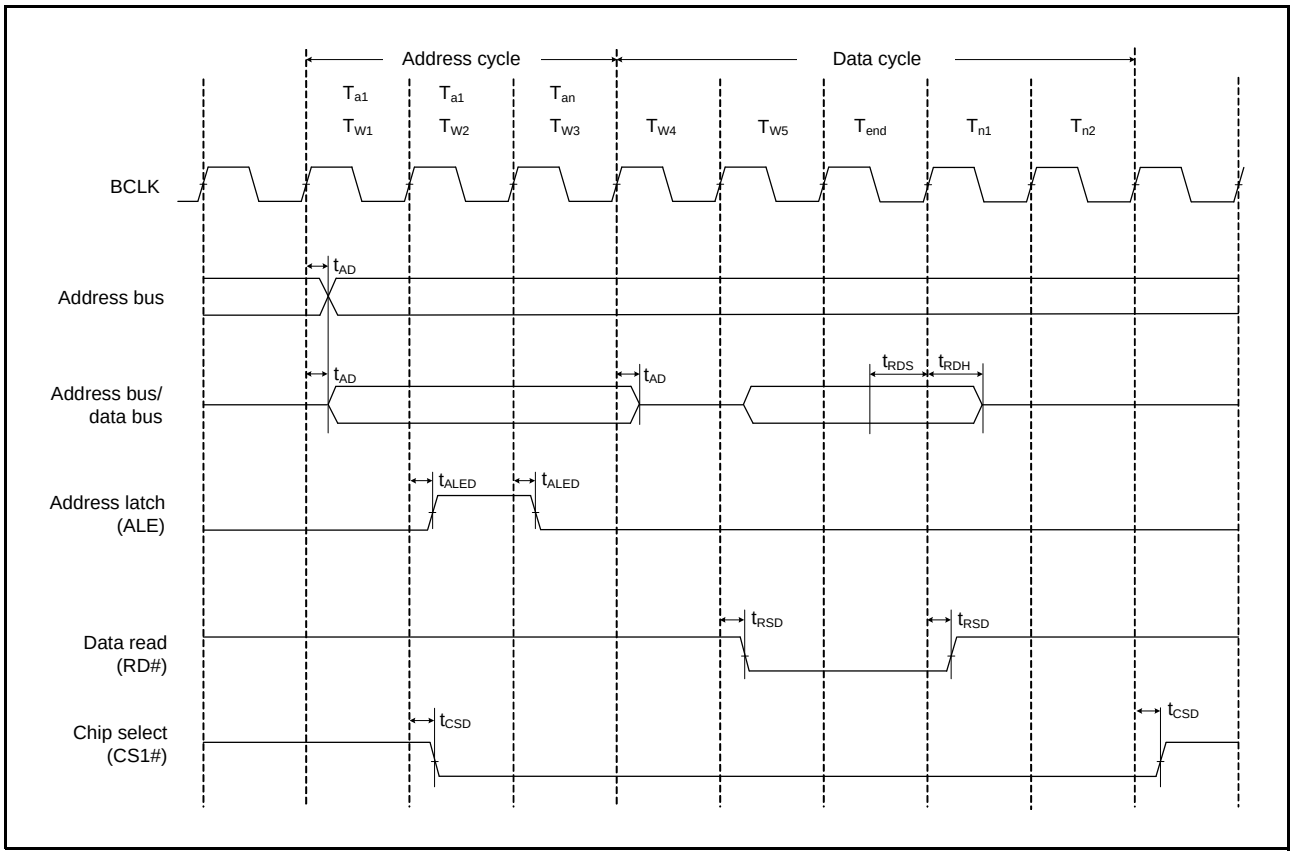


Figure 2.17 Address/Data Multiplexed Bus Read Access Timing

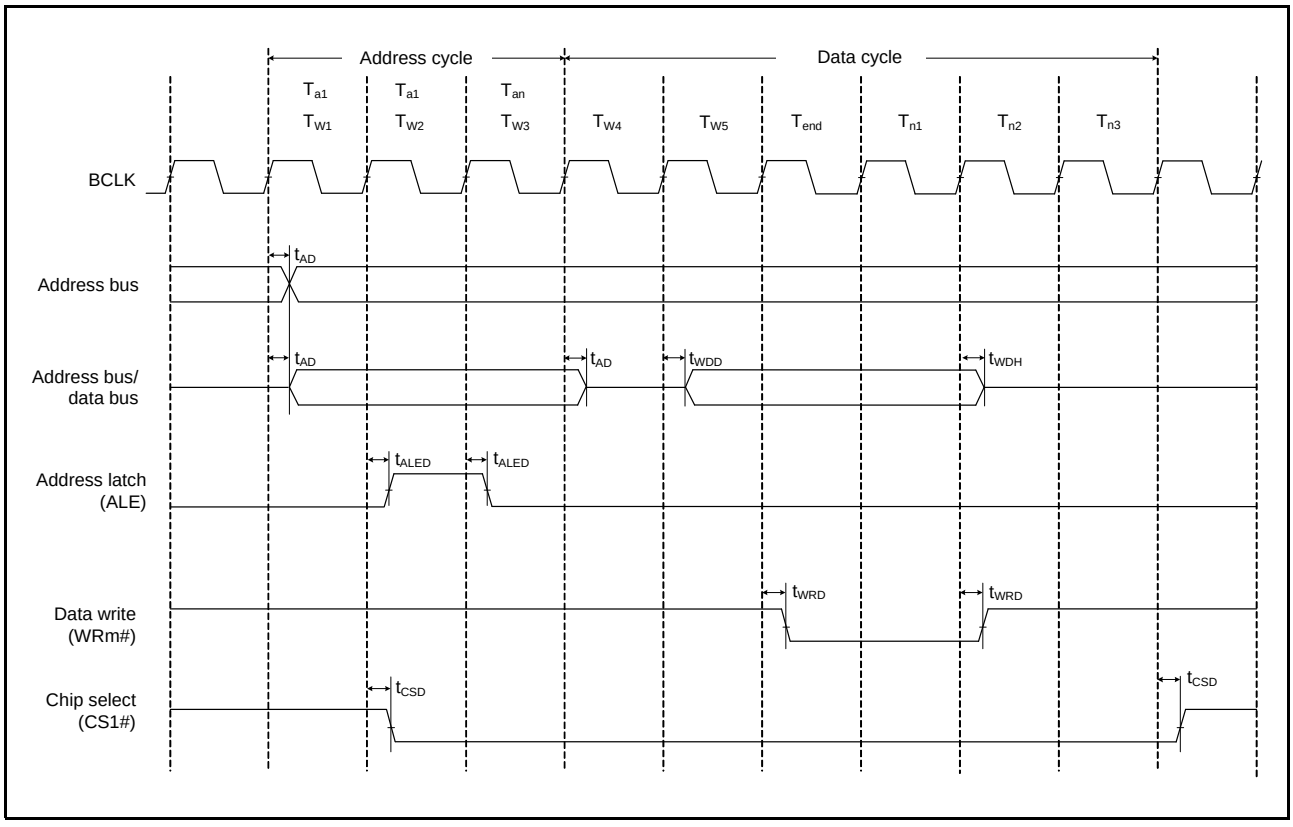


Figure 2.18 Address/Data Multiplexed Bus Write Access Timing

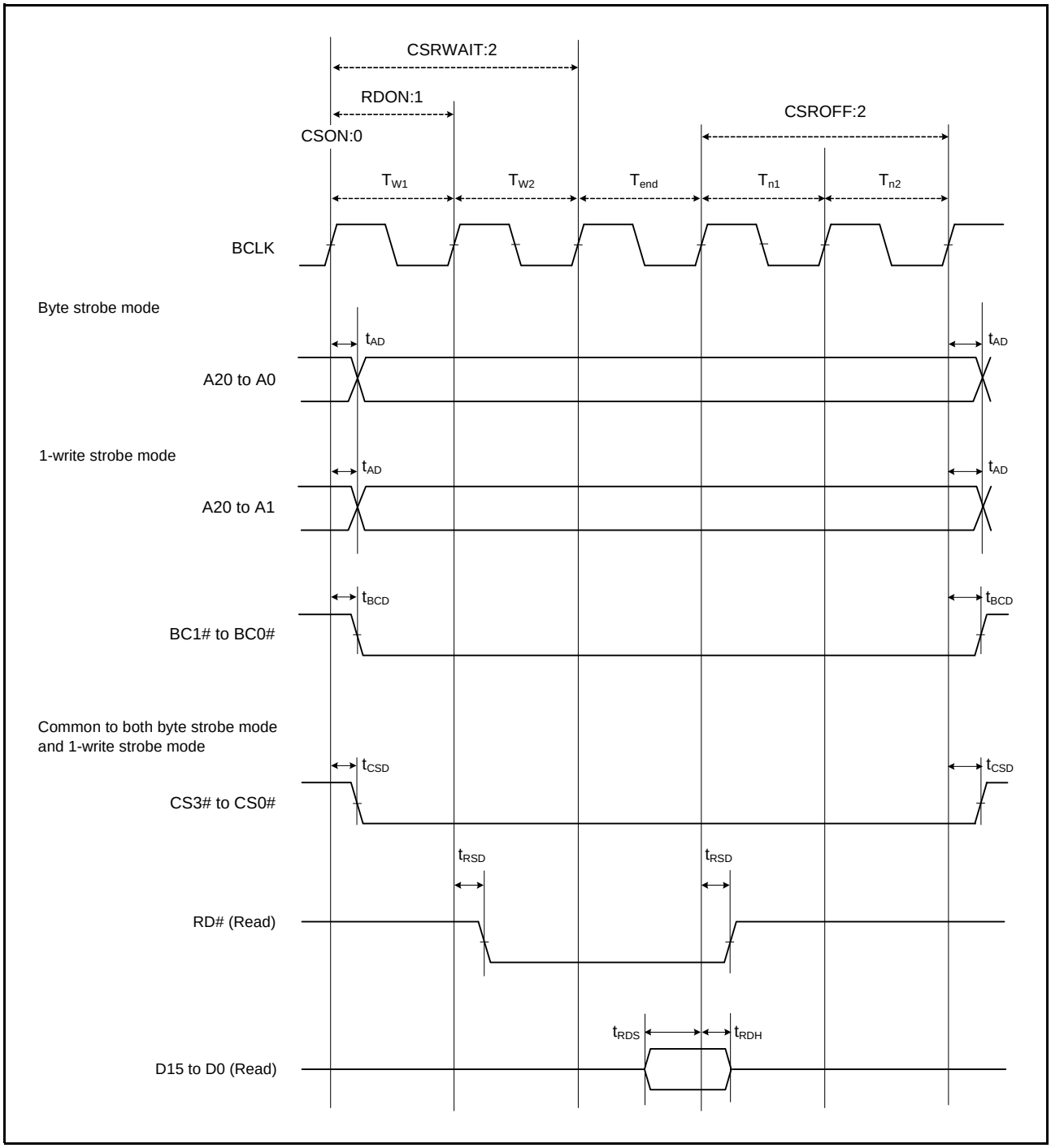
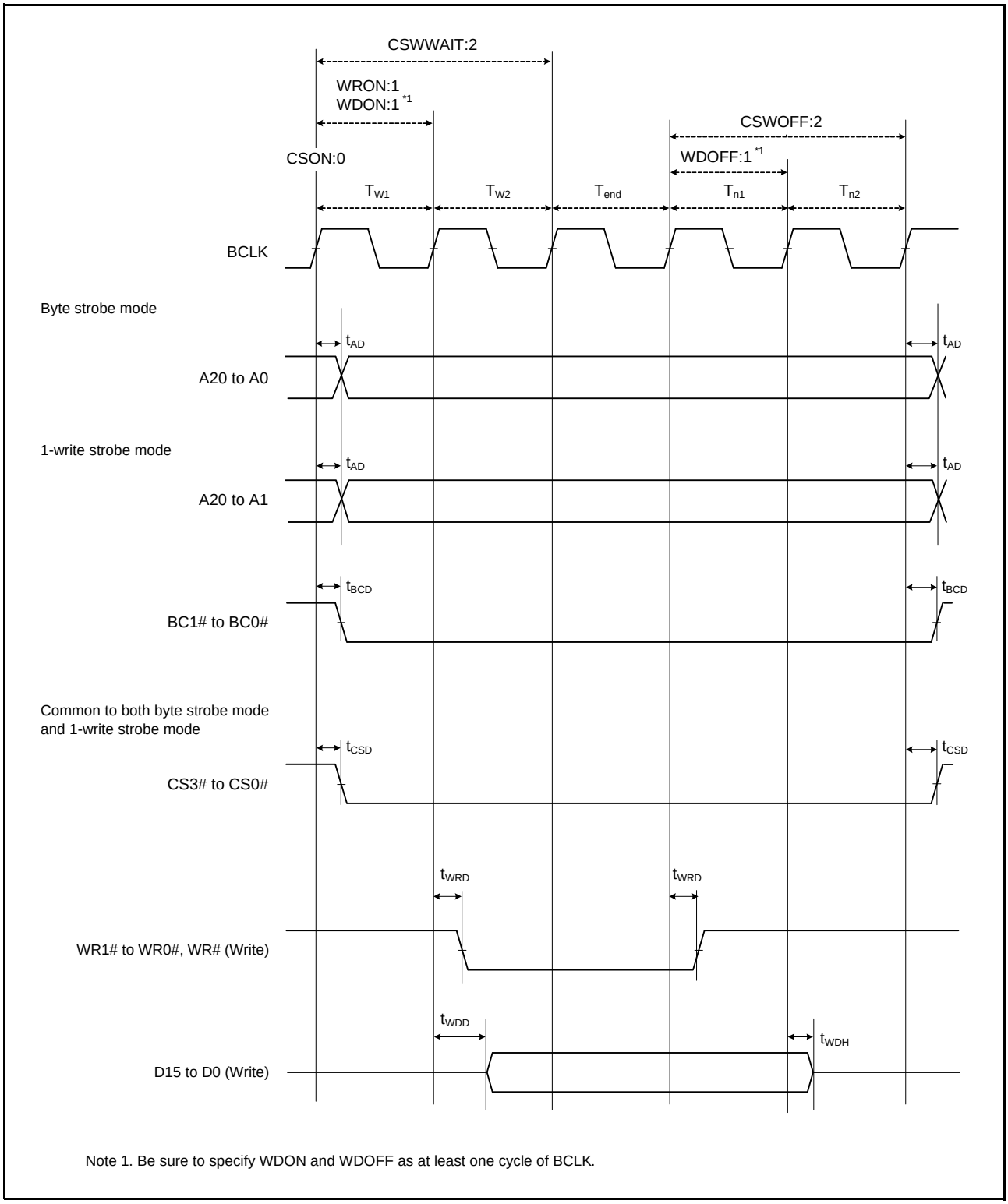


Figure 2.19 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 2.20 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

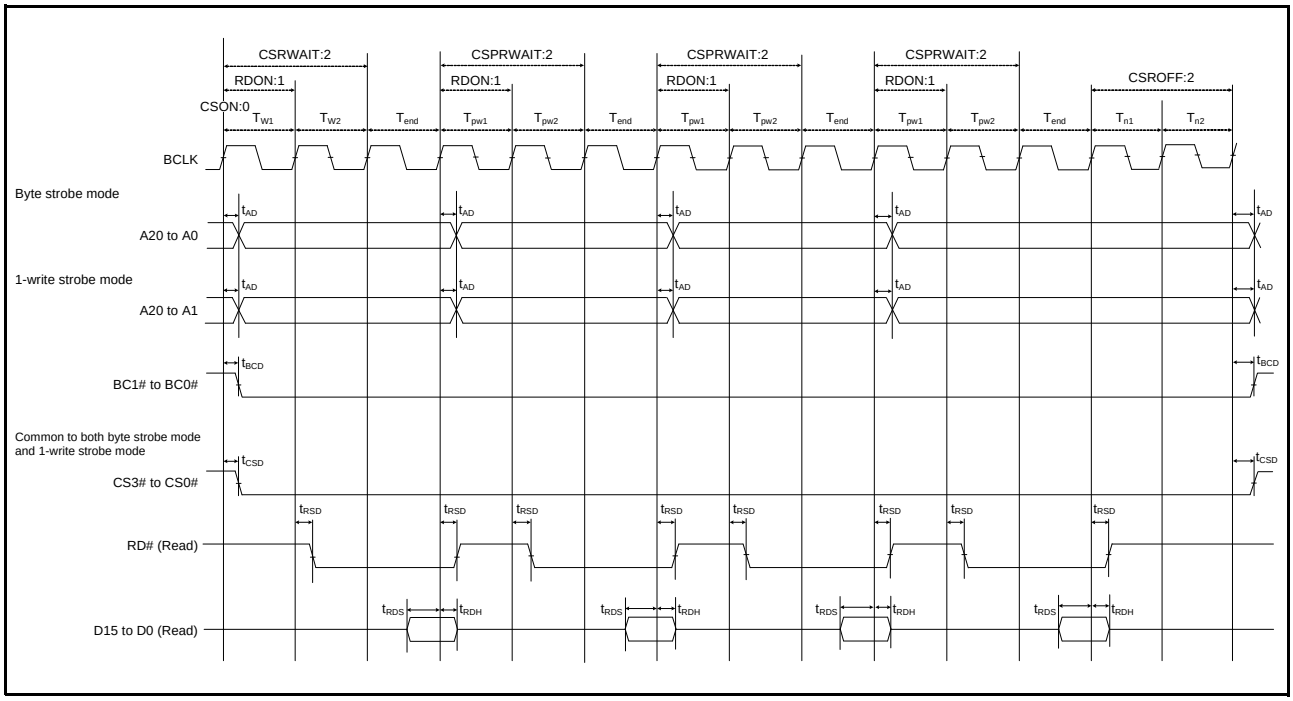
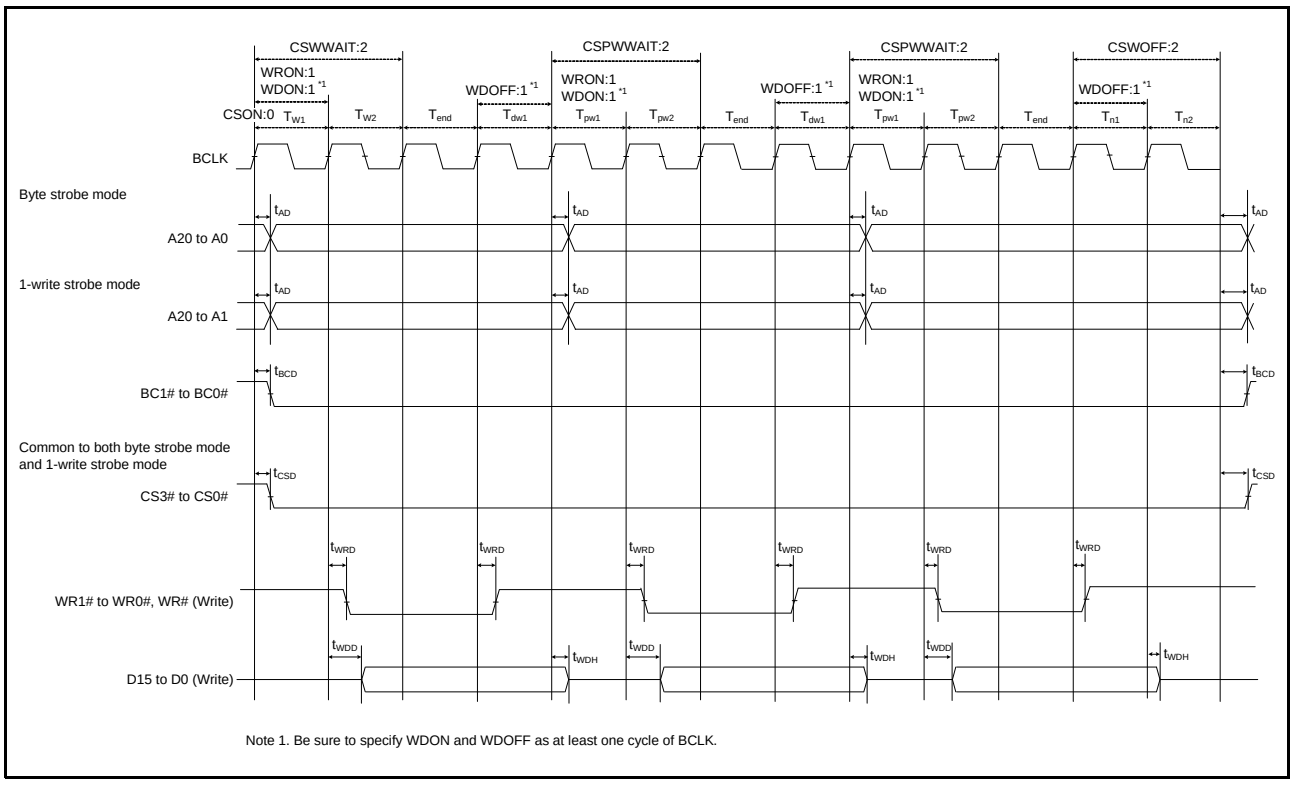


Figure 2.21 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 2.22 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

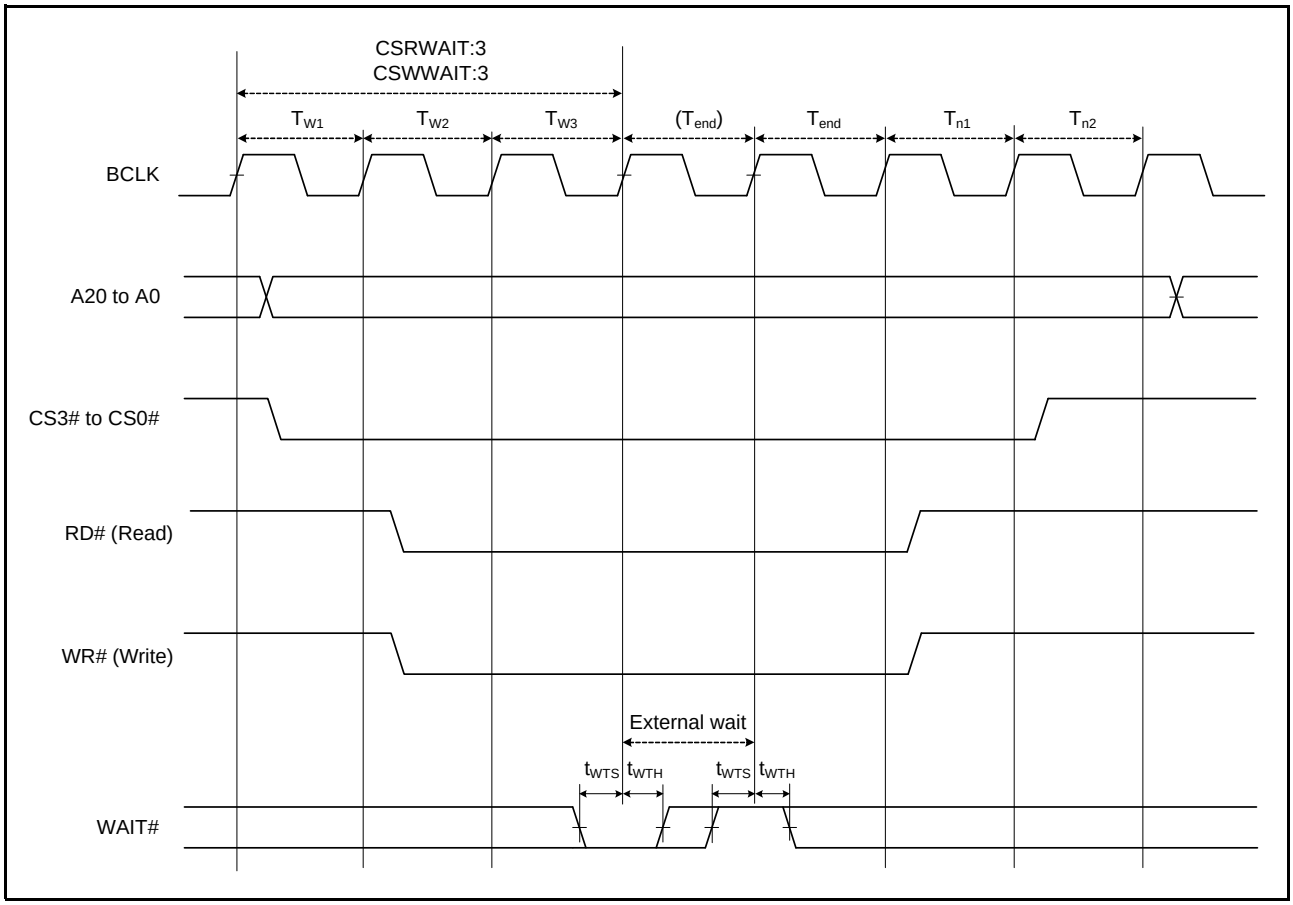


Figure 2.23 External Bus Timing/External Wait Control

2.4.6 Timing of On-Chip Peripheral Modules

2.4.6.1 I/O Port

Table 2.27 I/O Port Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 2.24

Note 1. t_{PBcyc}: PCLKB cycle

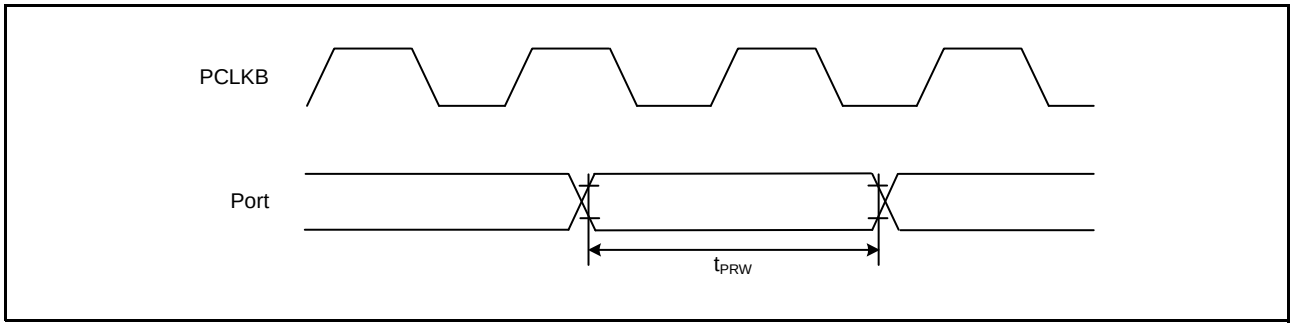


Figure 2.24 I/O Port Input Timing

2.4.6.2 TMR

Table 2.28 TMR Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 2.25
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

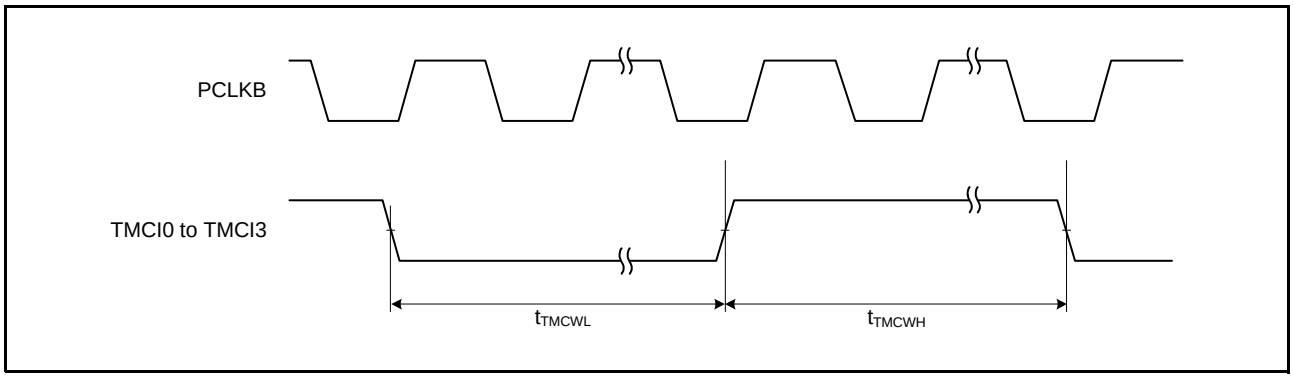


Figure 2.25 TMR Clock Input Timing

2.4.6.3 CMTW

Table 2.29 CMTW Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWTICW}$	1.5	—	t_{PBcyc}	Figure 2.26
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

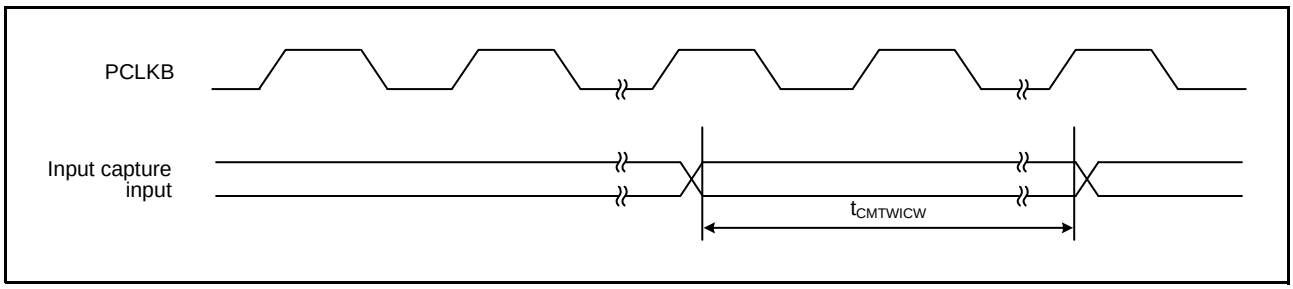


Figure 2.26 CMTW Input Capture Input Timing

2.4.6.4 MTU

Table 2.30 MTU Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PAcyc}	Figure 2.27
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PAcyc}	Figure 2.28
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PAcyc}: PCLKA cycle

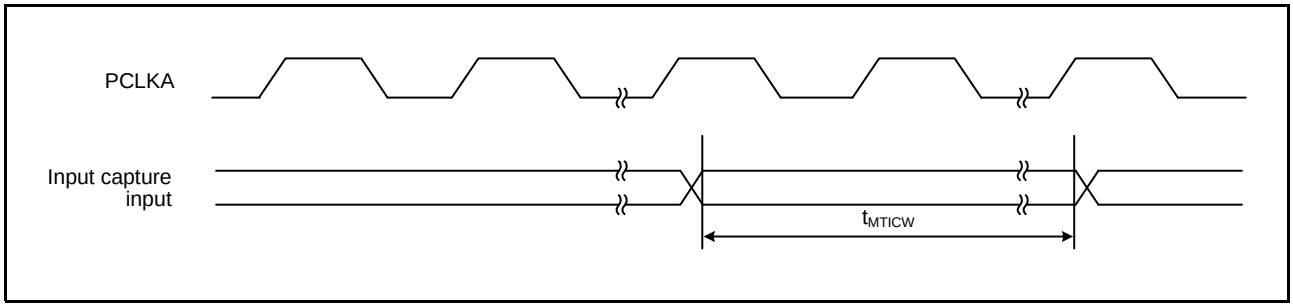


Figure 2.27 MTU Input Capture Input Timing

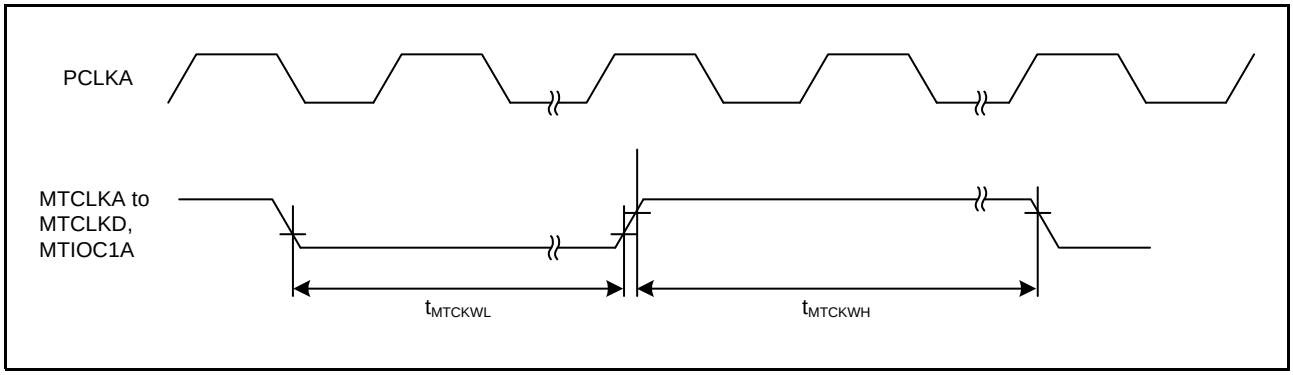


Figure 2.28 MTU Clock Input Timing

2.4.6.5 POE3

Table 2.31 POE3 Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POE	POEn# input pulse width (n = 0, 4, 8, 10, 11)		t_{POEW}	1.5	—	—	t_{PBcyc}	Figure 2.29
	Output disable time	Transition of the POEn# signal level	t_{POEDI}	—	—	5 PCLKB + 0.24	µs	Figure 2.30 When detecting falling edges (ICSRm.POEnM[3:0] = 0000b (m = 1 to 5; n = 0, 4, 8, 10, 11))
		Simultaneous conduction of output pins	t_{POEDO}	—	—	3 PCLKB + 0.2	µs	Figure 2.31
		Register setting	t_{POEDS}	—	—	1 PCLKB + 0.2	µs	Figure 2.32 Time for access to the register is not included.
		Oscillation stop detection	t_{POEDOS}	—	—	21	µs	Figure 2.33

Note 1. t_{PBcyc}: PCLKB cycle

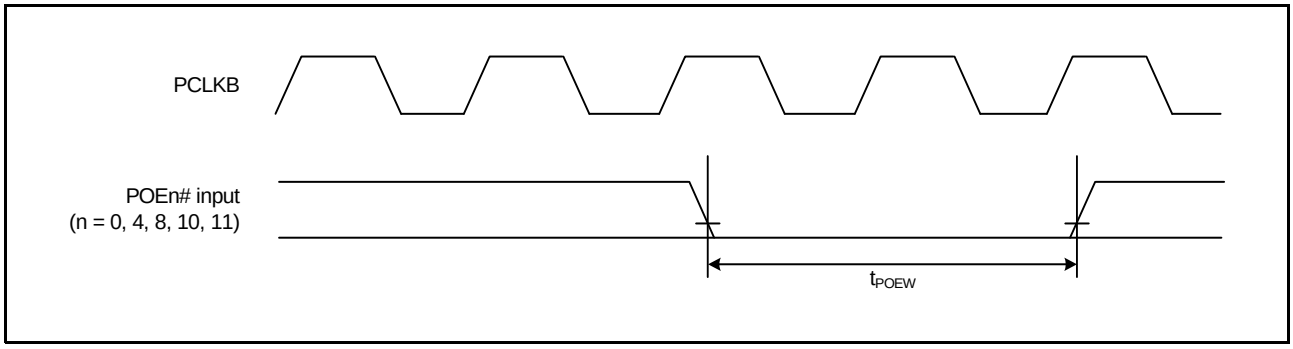


Figure 2.29 POE# Pin Input Timing

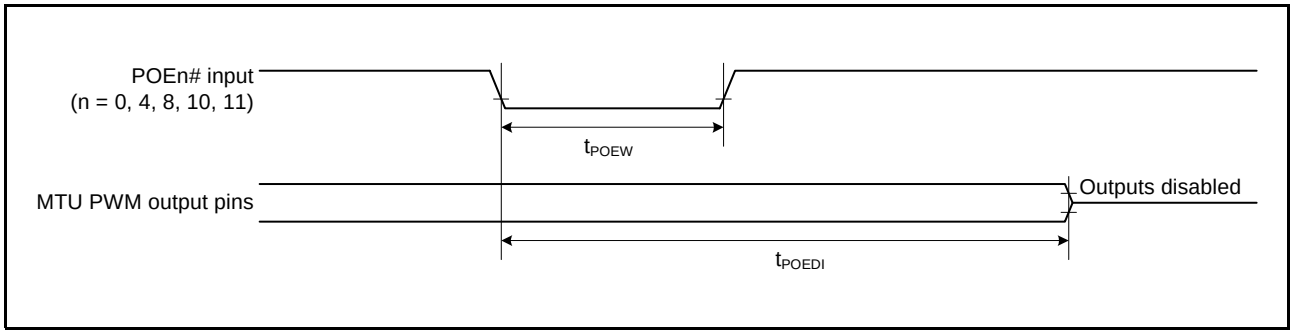
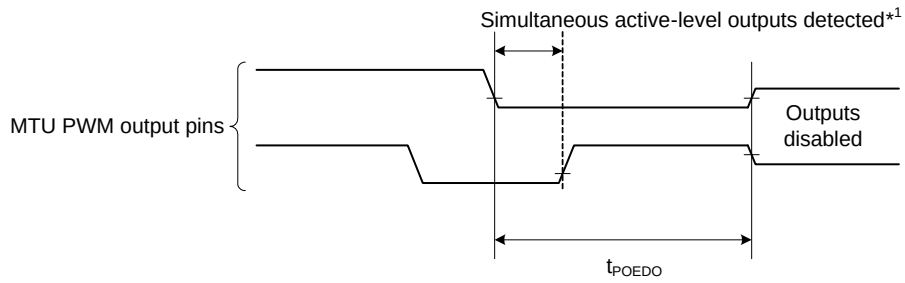


Figure 2.30 Output Disable Time for POE in Response to Transition of the POEn# Signal Level



Note 1. When the active level is set to low.

Figure 2.31 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

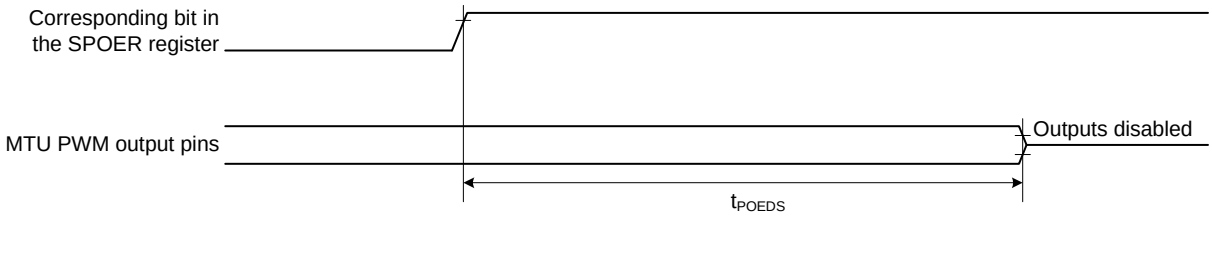


Figure 2.32 Output Disable Time for POE in Response to the Register Setting

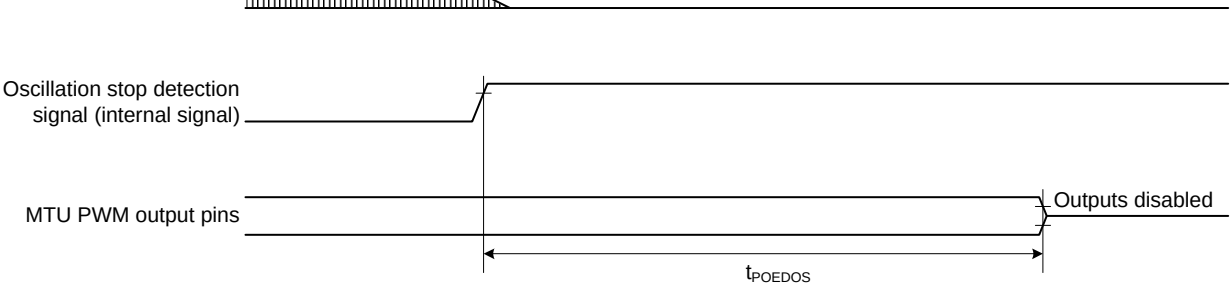


Figure 2.33 Output Disable Time for POE in Response to the Oscillation Stop Detection

2.4.6.6 A/D Converter Trigger

Table 2.32 A/D Converter Trigger Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	t_{TRGW}	1.5	—	t_{PBcyc}	Figure 2.34

Note 1. t_{PBcyc}: PCLKB cycle

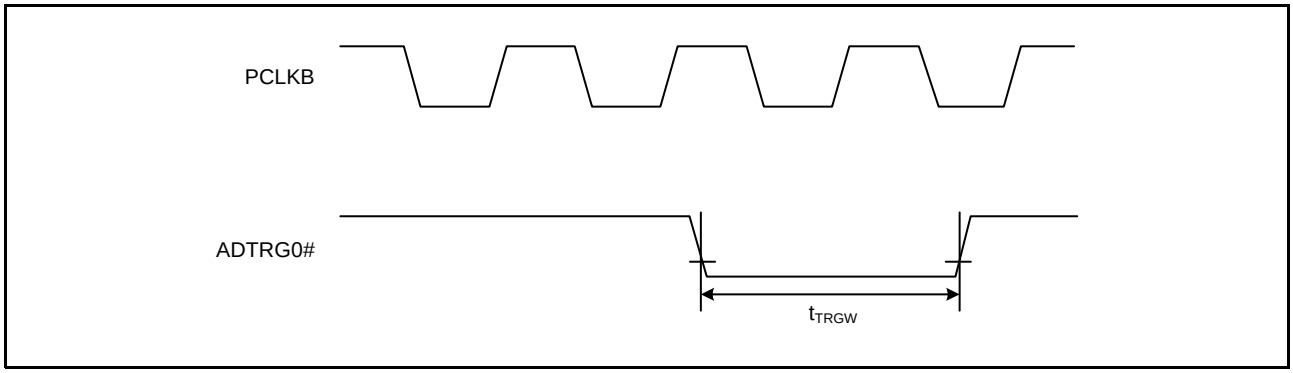


Figure 2.34 A/D Converter Trigger Input Timing

2.4.6.7 CAC

Table 2.33 CAC Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item*1, *2			Symbol	Min.*1, *2	Max.	Unit	Test Conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le t_{CAC}$	t_{CACREF}	$4.5\ t_{CAC} + 3\ t_{PBcyc}$	—	ns	
		$t_{PBcyc} > t_{CAC}$		$5\ t_{CAC} + 6.5\ t_{PBcyc}$	—		

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. t_{CAC}: CAC count clock source cycle

2.4.6.8 SCI

Table 2.34 SCIk, SCIh, and SCIm Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions	
SCIk, SCIh	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PBcyc}	Figure 2.35	
		Clock synchronous		6	—			
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Input clock rise time		t_{SCKr}	—	5	ns		
	Input clock fall time		t_{SCKf}	—	5	ns		
	Output clock cycle	Asynchronous (SCIk)	t_{Scyc}	6	—	t_{PBcyc}		
		Asynchronous (SCIh)		8	—			
		Clock synchronous		4	—			
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Output clock rise time		t_{SCKr}	—	5	ns		
	Output clock fall time		t_{SCKf}	—	5	ns		
	Transmit data delay time	Clock synchronous	t_{TXD}	—	28	ns	VCC ≥ 4.5 V	Figure 2.36
				—	33		VCC < 4.5 V	
	Receive data setup time	Clock synchronous	t_{RXS}	15	—	ns	Figure 2.36	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns		
SCIm	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PAcyc}	Figure 2.35	
		Clock synchronous		6	—			
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Input clock rise time		t_{SCKr}	—	5	ns		
	Input clock fall time		t_{SCKf}	—	5	ns		
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{PAcyc}		
		Clock synchronous		4	—			
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Output clock rise time		t_{SCKr}	—	5	ns		
	Output clock fall time		t_{SCKf}	—	5	ns		
	Transmit data delay time	Master	t_{TXD}	—	15	ns	VCC ≥ 4.5 V	Figure 2.36
				—	20		VCC < 4.5 V	
		Slave		—	28		VCC ≥ 4.5 V	
				—	33		VCC < 4.5 V	
	Receive data setup time	Clock synchronous	t_{RXS}	20	—	ns	Figure 2.36	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns		

Note 1. t_{PBcyc}: PCLKB cycle; t_{PAcyc}: PCLKA cycle

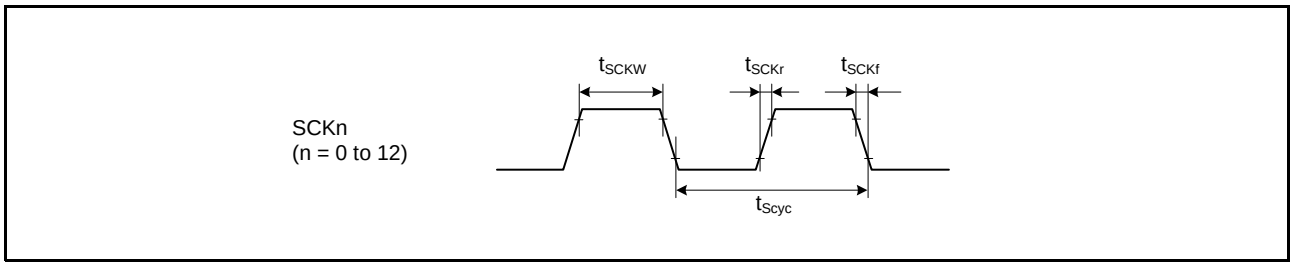


Figure 2.35 SCK Clock Input Timing

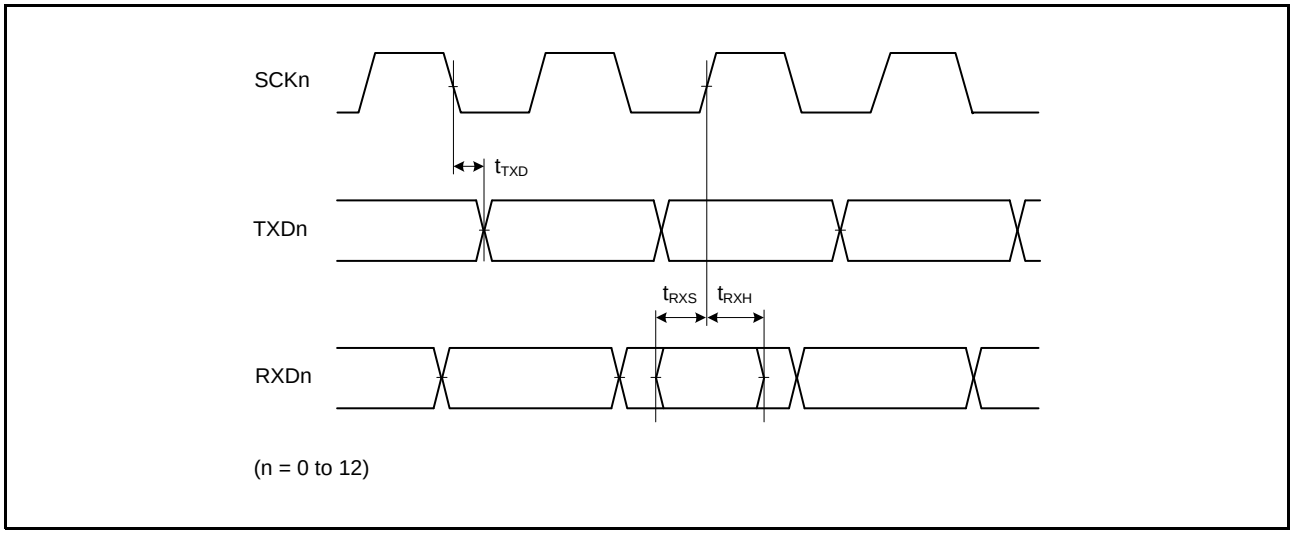


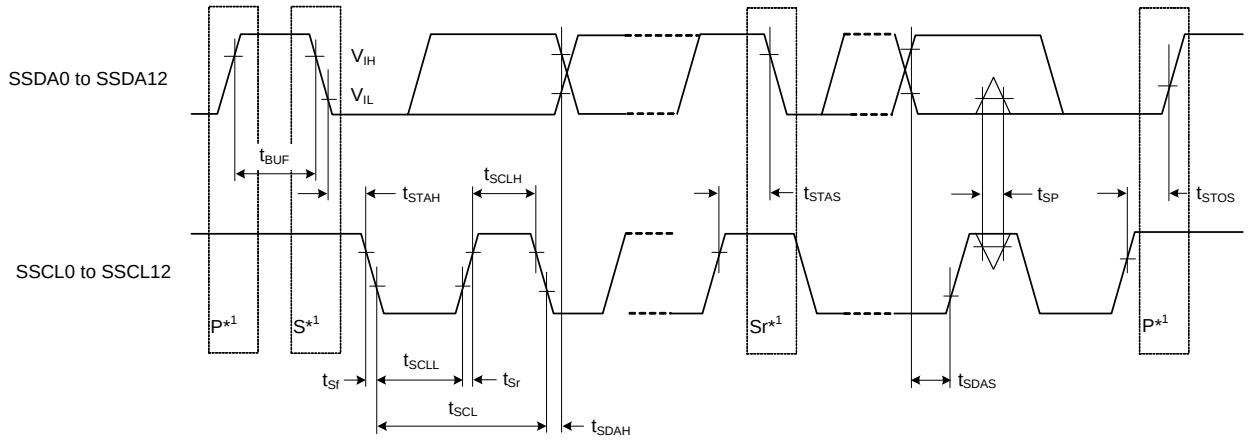
Figure 2.36 SCI Input/Output Timing: Clock Synchronous Mode

Table 2.35 Simple IIC Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SSCL, SSDA input rise time	t_{Sr}	—	1000	ns	Figure 2.37
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	$4 \times t_{Pcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast-mode)	SSCL, SSDA input rise time	t_{Sr}	—	300	ns	
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	$4 \times t_{Pcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	

Note: t_{Pcyc} refers to the period of PCLKA in SCI10 and SCI11, and of PCLKB in SCI0 to SCI9, and SCI12.
Note 1. Cb is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
$V_{IH} = 0.7 \times VCC$, $V_{IL} = 0.3 \times VCC$
$V_{OL} = 0.6$ V, $I_{OL} = 6$ mA

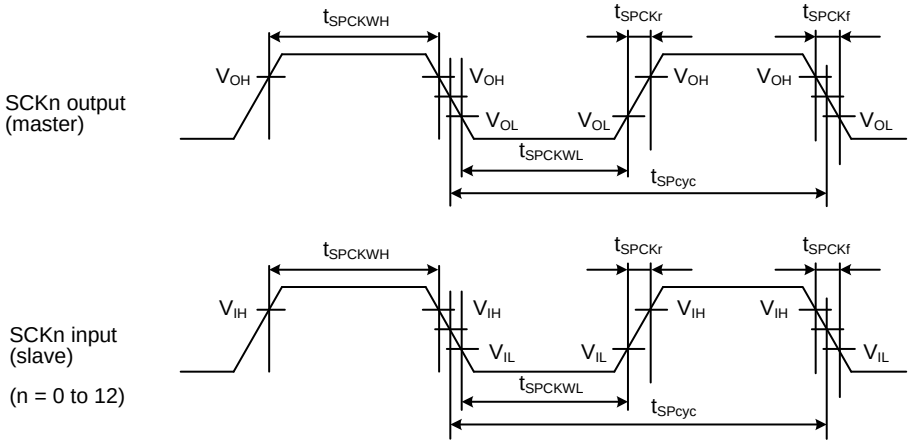
Figure 2.37 Simple IIC Bus Interface Input/Output Timing

Table 2.36 Simple SPI Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	—	t_{Pcyc}	Figure 2.38
	SCK clock cycle input (slave)		6	—		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 2.39 to Figure 2.42
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 2.41, Figure 2.42
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note: t_{Pcyc} refers to the period of PCLKA in SCI10 and SCI11, and of PCLKB in SCI0 to SCI9, and SCI12.



$V_{OH} = 0.7 \times VCC$, $V_{OL} = 0.3 \times VCC$, $V_{IH} = 0.7 \times VCC$, $V_{IL} = 0.3 \times VCC$

Figure 2.38 Simple SPI Clock Timing

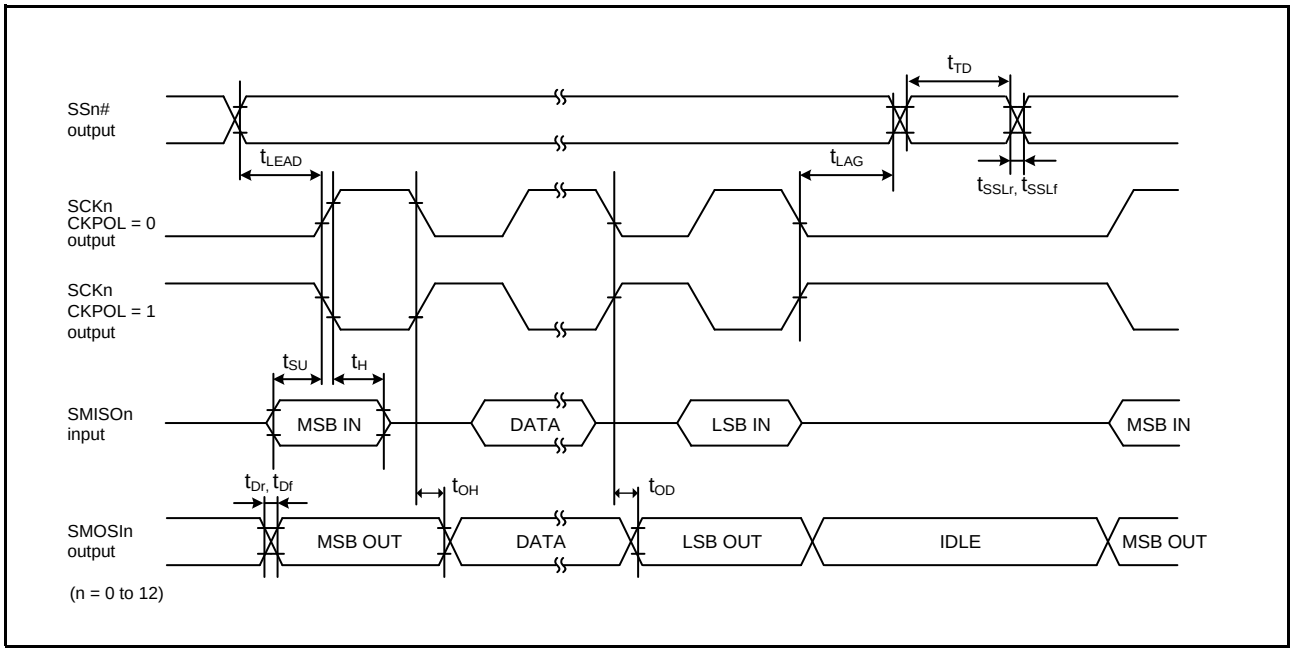


Figure 2.39 Simple SPI Timing (Master, CKPH = 1)

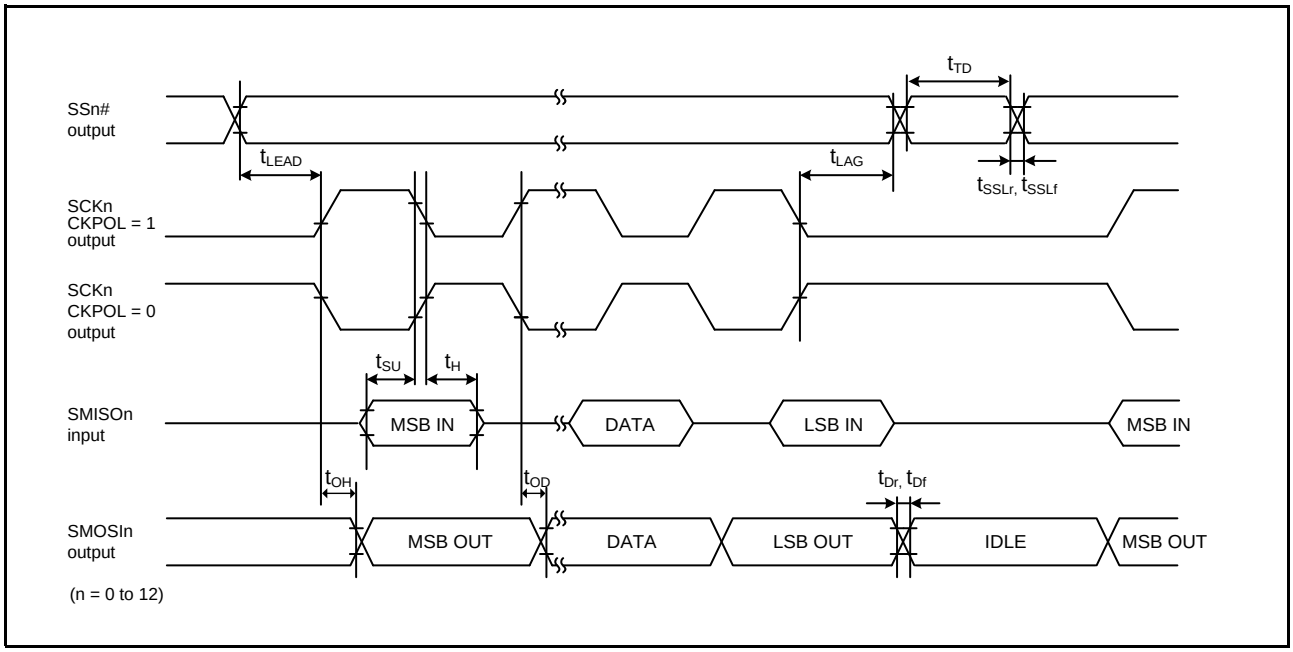


Figure 2.40 Simple SPI Timing (Master, CKPH = 0)

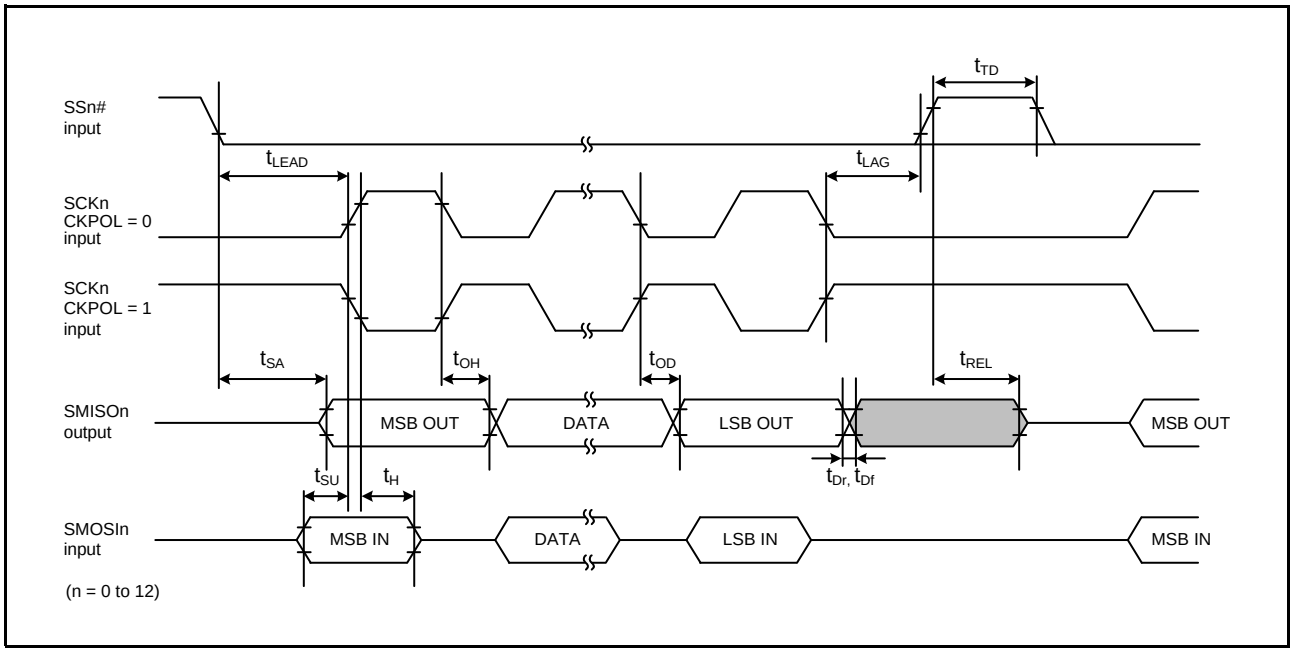


Figure 2.41 Simple SPI Timing (Slave, CKPH = 1)

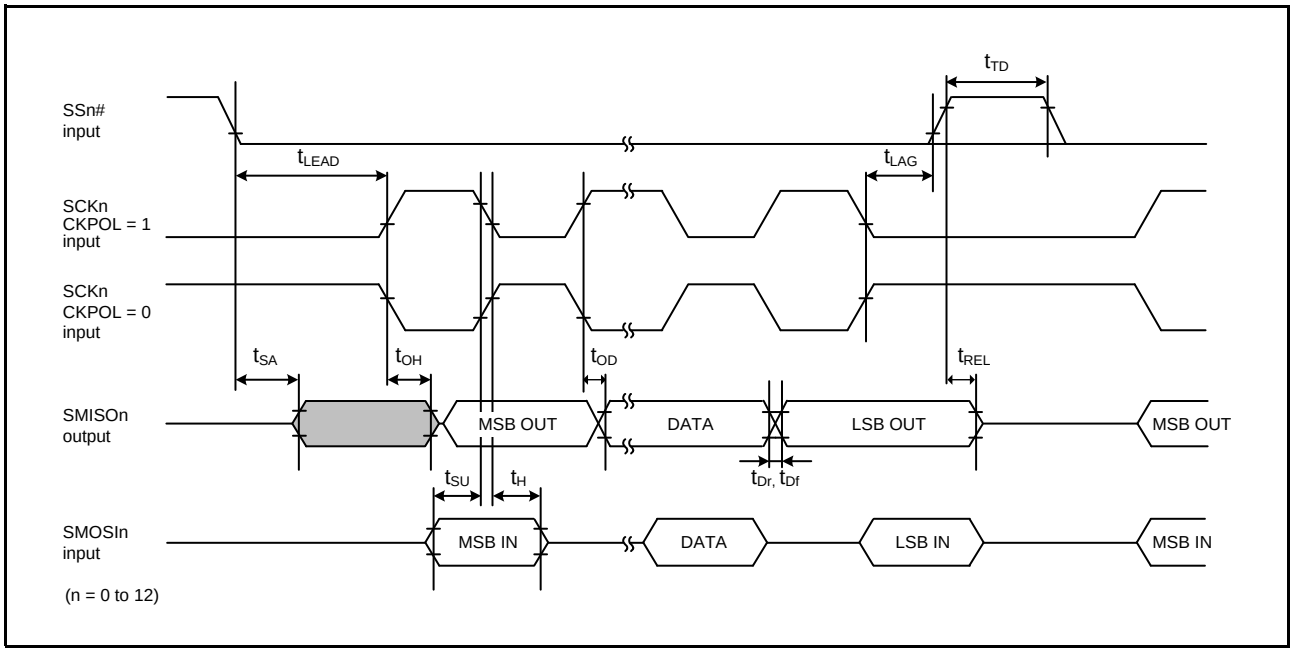


Figure 2.42 Simple SPI Timing (Slave, CKPH = 0)

2.4.6.9 RSCI

Table 2.37 RSCI Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions	
RSCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PAcyc}	Figure 2.43	
		Clock synchronous		2	—			
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Input clock rise time		t_{SCKr}	—	5	ns		
	Input clock fall time		t_{SCKf}	—	5	ns		
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{PAcyc}		
		Clock synchronous		2	—			
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Output clock rise time		t_{SCKr}	—	5	ns		
	Output clock fall time		t_{SCKf}	—	5	ns		
	Receive data setup time	Master	t_{RXS}	–1.5	—	ns	VCC ≥ 4.5 V	Figure 2.44
				3.5	—		VCC < 4.5 V	
		Slave		2.5	—		Figure 2.44	
	Receive data hold time	Master	t_{RXH}	11	—	ns		
		Slave		2.5	—			
	Transmit data delay time	Master	t_{TXD}	—	4	ns		
		Slave		—	17		VCC ≥ 4.5 V	Figure 2.44
				—	22		VCC < 4.5 V	

Note 1. t_{PAcyc}: PCLKA cycle; t_{Scyc}: SCK cycle

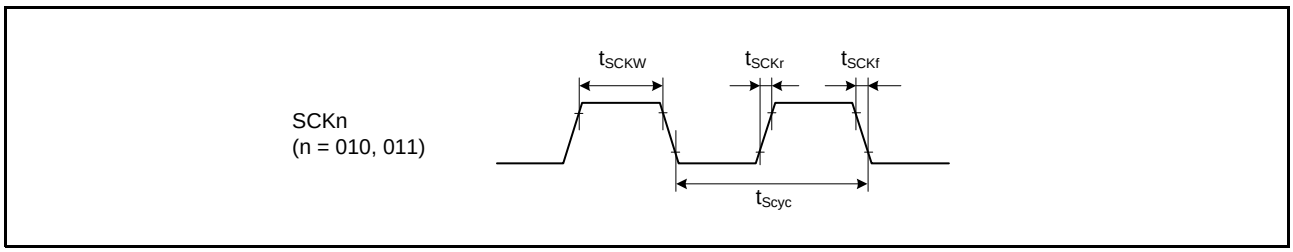


Figure 2.43 SCK Clock Input Timing

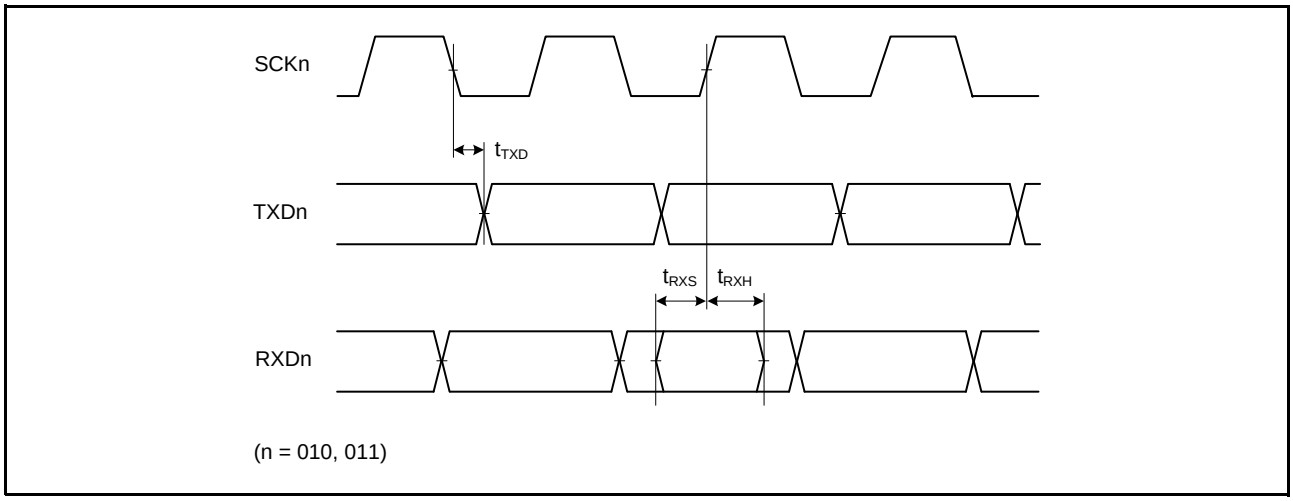


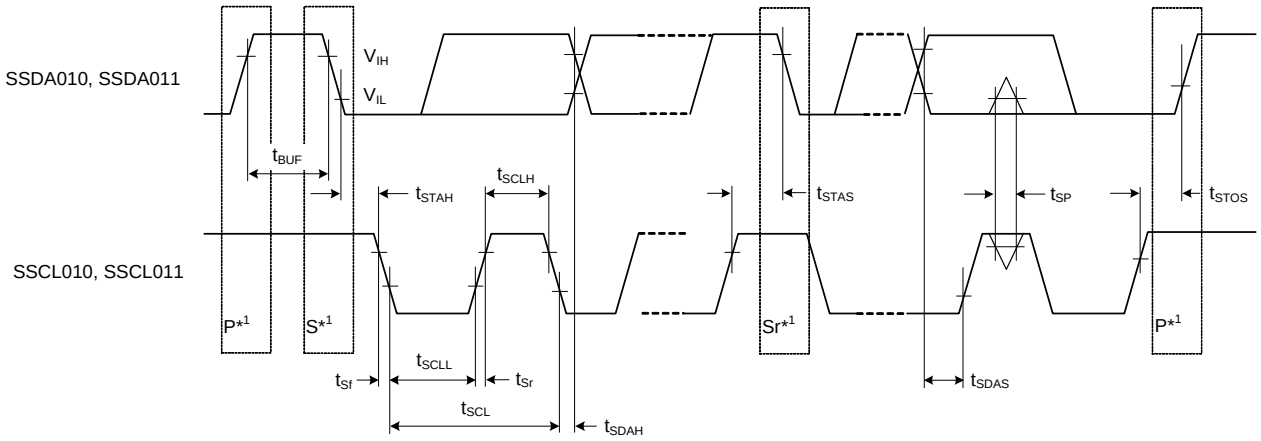
Figure 2.44 RSCI Input/Output Timing: Clock Synchronous Mode

Table 2.38 Simple IIC Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SSCL, SSDA input rise time	t_{Sr}	—	1000	ns	Figure 2.45
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	$4 \times t_{PAcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast-mode)	SSCL, SSDA input rise time	t_{Sr}	—	300	ns	
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	$4 \times t_{PAcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	

Note: t_{PAcyc}: PCLKA cycle
Note 1. Cb is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
$V_{IH} = 0.7 \times VCC$, $V_{IL} = 0.3 \times VCC$
$V_{OL} = 0.6$ V, $I_{OL} = 6$ mA

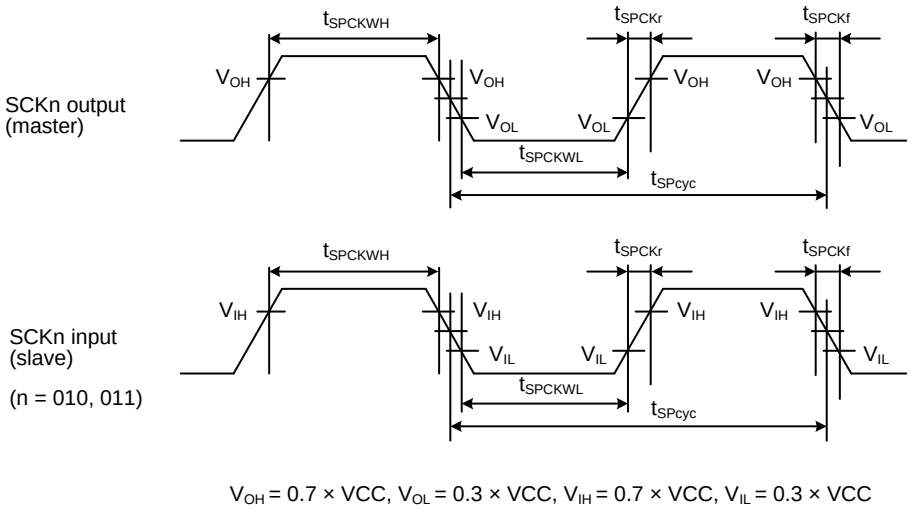
Figure 2.45 Simple IIC Bus Interface Input/Output Timing

Table 2.39 Simple SPI Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	2	—	t_{PAcyc}	Figure 2.46
	SCK clock cycle input (slave)			2	—		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input		—	1	µs	
	Data input setup time	Master	t_{SU}	0.5	—	ns	Figure 2.47 to Figure 2.50
		Slave		2.5	—		
	Data input hold time	Master	t_H	11	—	ns	
		Slave		2.5	—		
	Data output delay time	Master	t_{OD}	—	4	ns	Figure 2.47 to Figure 2.50
		Slave		—	17		VCC ≥ 4.5V: Figure 2.47 to Figure 2.50
				—	22		VCC < 4.5V: Figure 2.47 to Figure 2.50
	Data output hold time	Master	t_{OH}	–1	—	ns	Figure 2.47 to Figure 2.50
		Slave		0	—		
	Data rise/fall time	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	—	
	Slave access time		t_{SA}	—	5	t_{PAcyc}	Figure 2.49, Figure 2.50
	Slave output release time		t_{REL}	—	5	t_{PAcyc}	
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	Figure 2.47 to Figure 2.50
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	1	µs	

Note 1. t_{PAcyc}: PCLKA cycle



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.46 Simple SPI Clock Timing

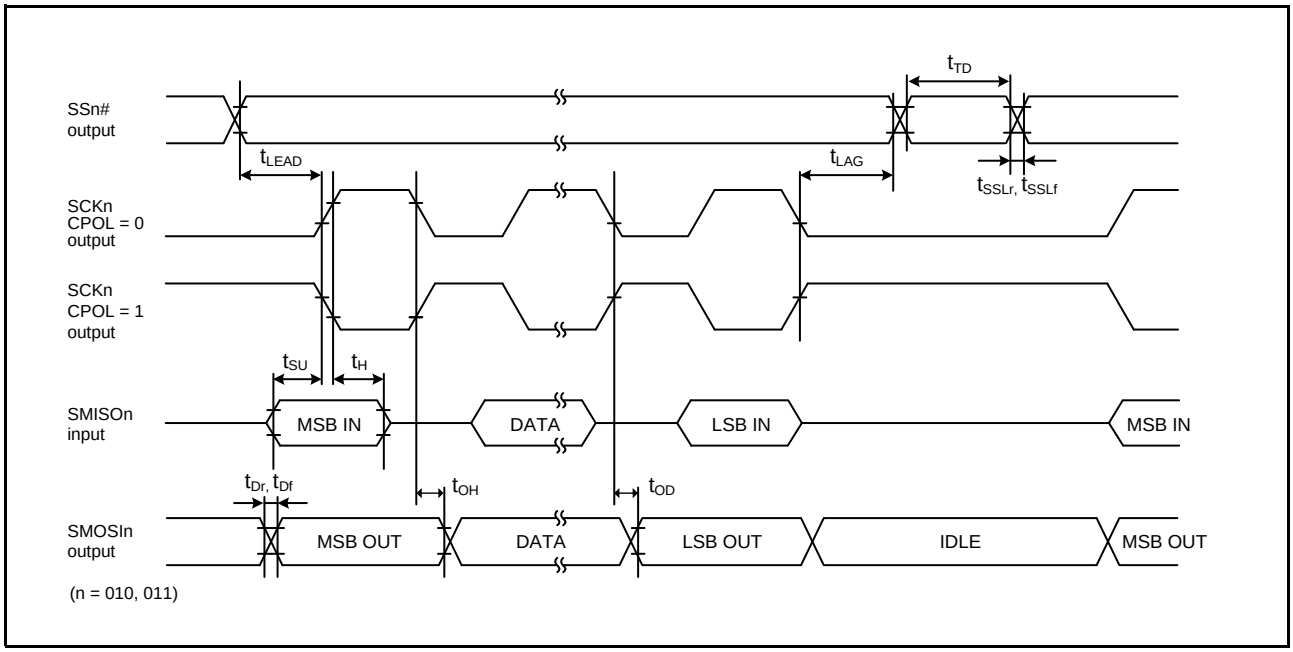


Figure 2.47 Simple SPI Timing (Master, CPHA = 0)

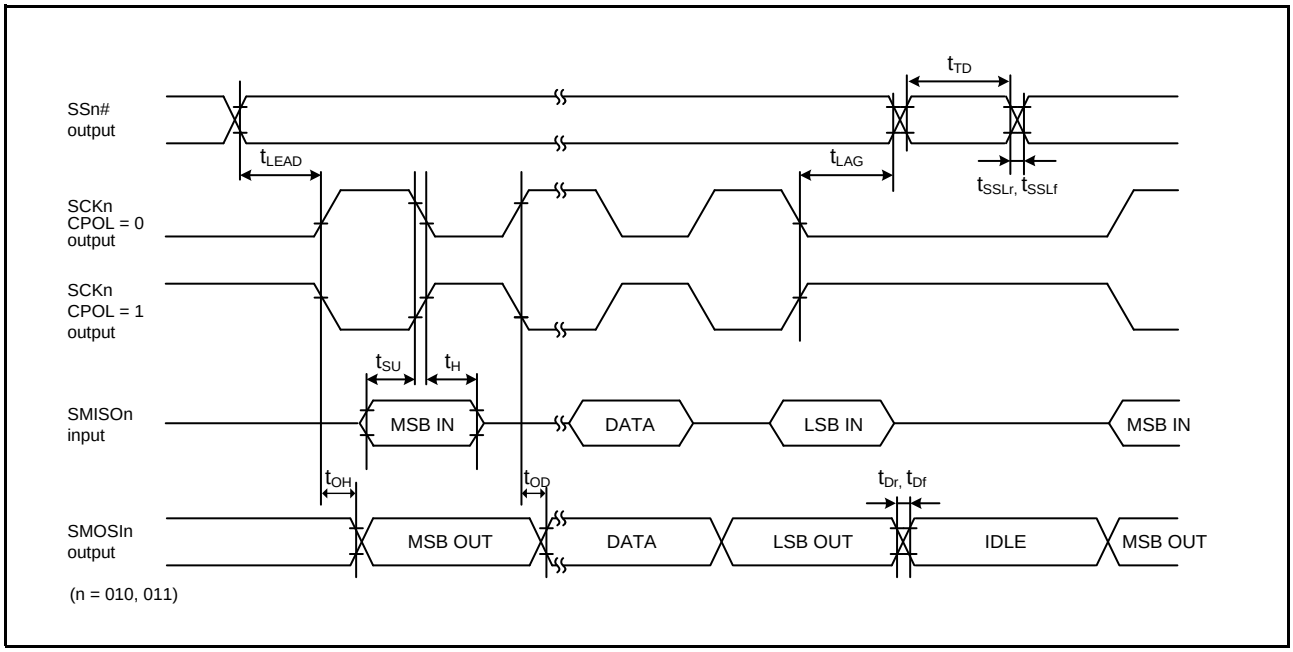


Figure 2.48 Simple SPI Timing (Master, CPHA = 1)

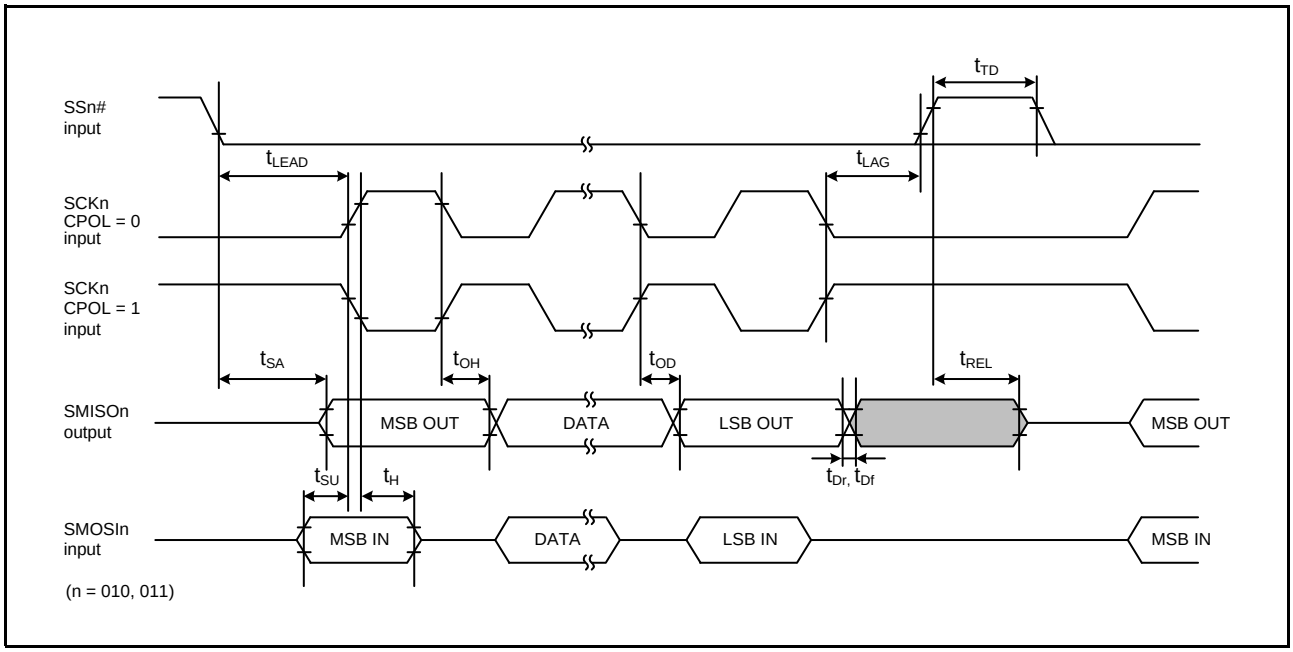


Figure 2.49 Simple SPI Timing (Slave, CPHA = 0)

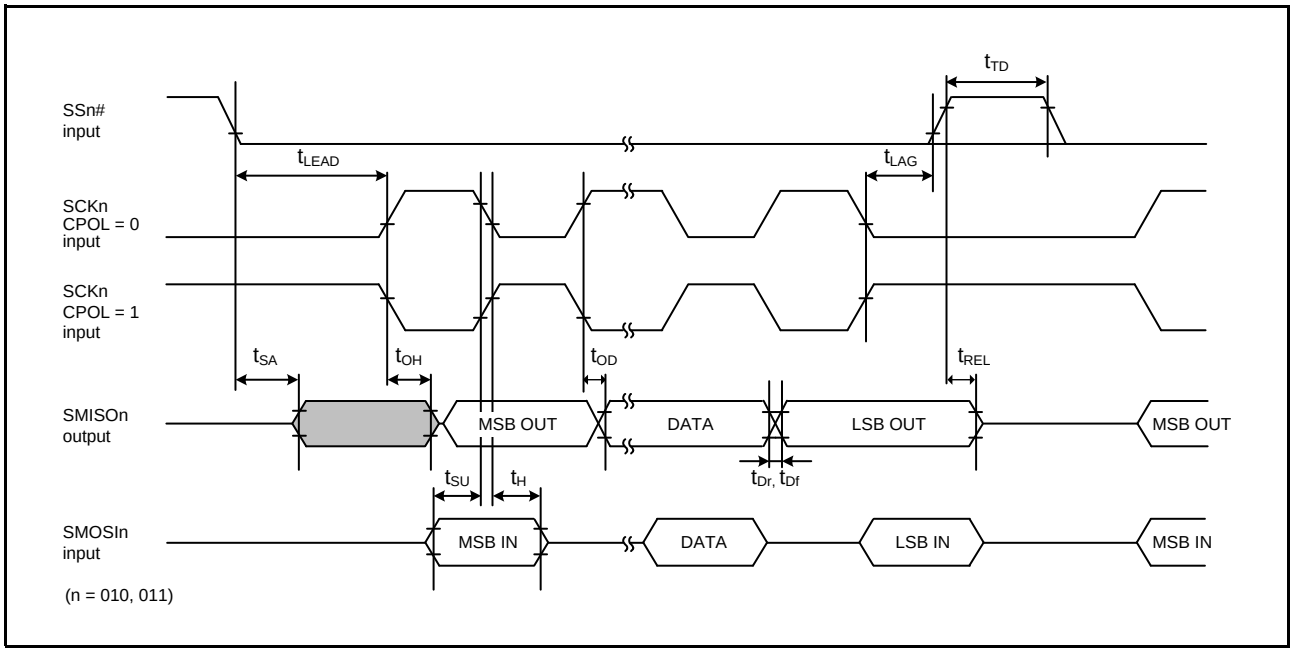


Figure 2.50 Simple SPI Timing (Slave, CPHA = 1)

2.4.6.10 RSPI

Table 2.40 RSPI Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item				Symbol	Min.*1	Max.*1	Unit*1	Test Conditions*2	
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	—	t_{PAcyc}	Figure 2.51	
		Slave			4	—			
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns		
		Slave			0.4	0.6	t_{SPcyc}		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns		
		Slave			0.4	0.6	t_{SPcyc}		
	RSPCK clock rise/ fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns		
		Input			—	1	µs		
	Data input setup time	Master		t_{SU}	6	—	ns	VCC ≥ 4.5 V	Figure 2.52 to Figure 2.57
					11	—		VCC < 4.5 V	
		Slave			8.3	—		Figure 2.52 to Figure 2.57	
	Data input hold time	Master	PCLKA division ratio set to 1/2	t_{HF}	0	—	ns		
			PCLKA division ratio set to a value other than 1/2	t_H	t_{PAcyc}	—	ns		
		Slave			8.3	—			
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}		
		Slave			4	—	t_{PAcyc}		
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}		
		Slave			4	—	t_{PAcyc}		
	Data output delay time	Master		t_{OD}	—	6.3	ns	VCC ≥ 4.5 V	Figure 2.52 to Figure 2.57
					—	11.3		VCC < 4.5 V	
		Slave			—	28		VCC ≥ 4.5 V	
					—	33		VCC < 4.5 V	
	Data output hold time	Master		t_{OH}	0	—	ns	Figure 2.52 to Figure 2.57	
		Slave			0	—			
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns		
		Slave			$4 \times t_{PAcyc}$	—			
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	5	ns		
		Input			—	1	µs		
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	5	ns		
		Input			—	1	µs		
	Slave access time			t_{SA}	—	28	ns	VCC ≥ 4.5 V	Figure 2.56, Figure 2.57
					—	33		VCC < 4.5 V	
	Slave output release time			t_{REL}	—	28	ns	VCC ≥ 4.5 V	
					—	33		VCC < 4.5 V	

Note 1. t_{PAcyc}: PCLKA cycle
Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All RSPI AC timings are measured in combination with the pins in the same group.

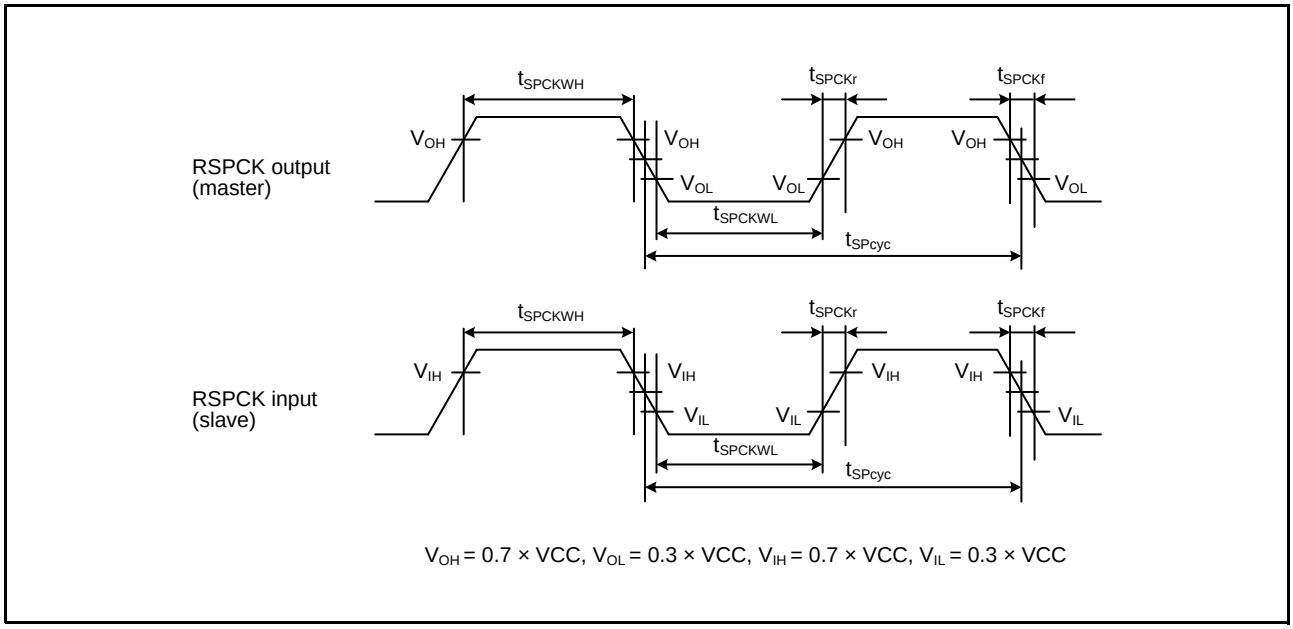


Figure 2.51 RSPI Clock Timing

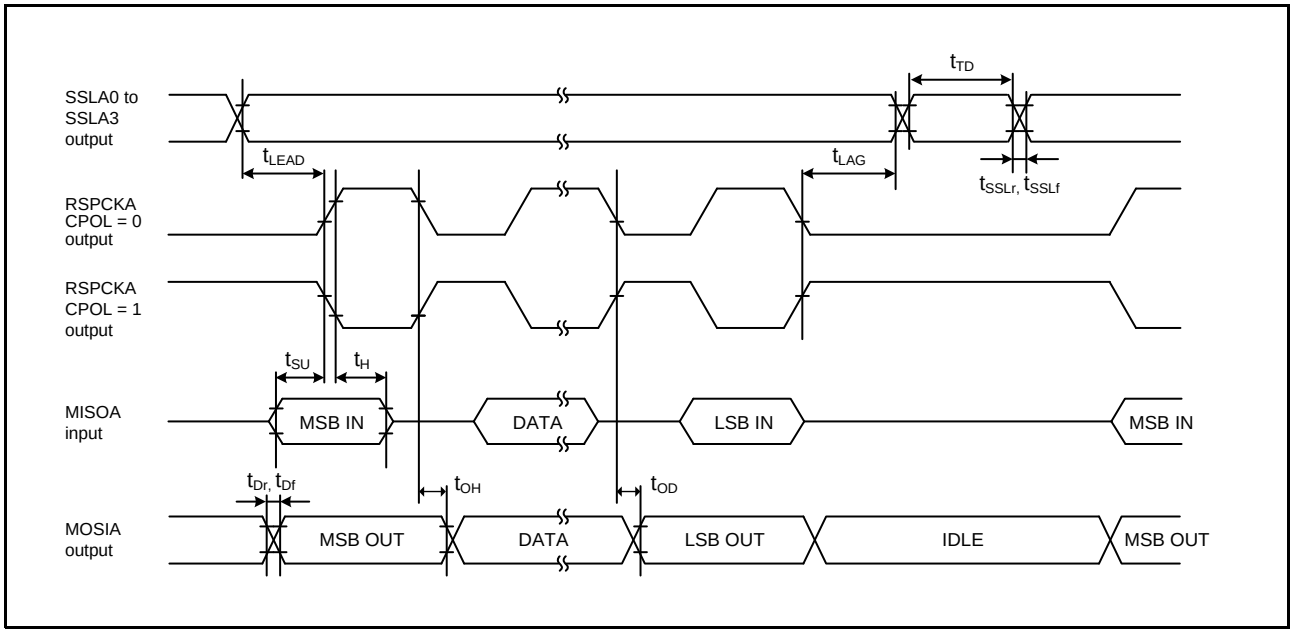


Figure 2.52 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

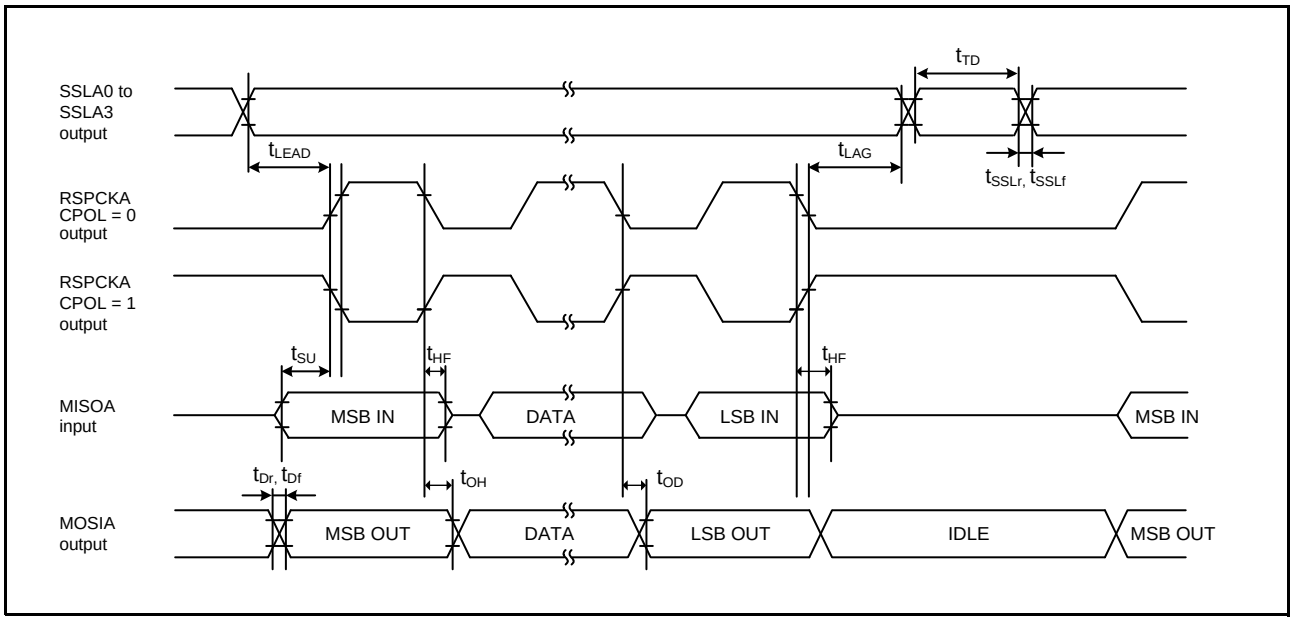


Figure 2.53 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)

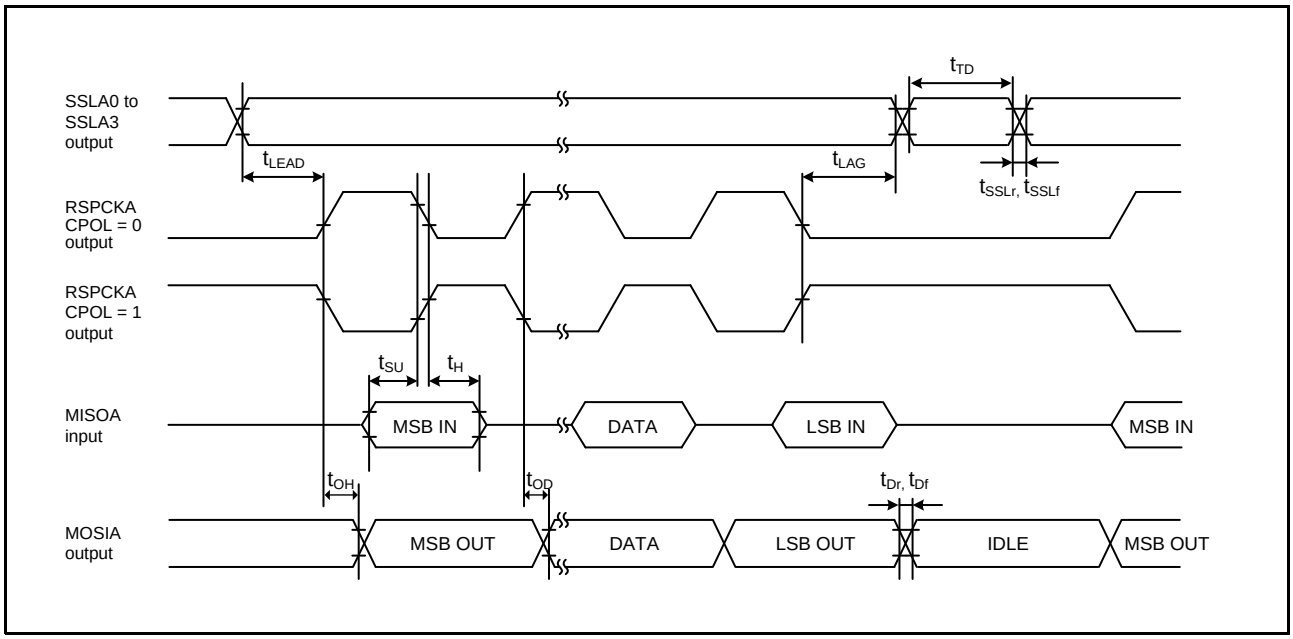


Figure 2.54 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

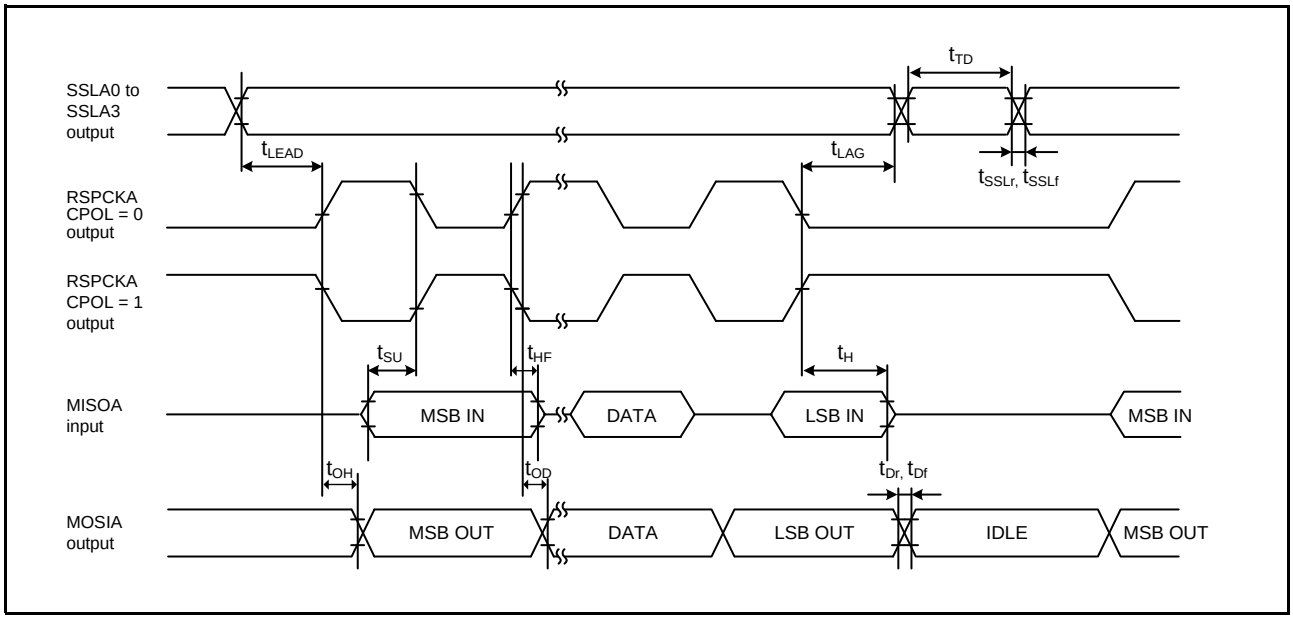


Figure 2.55 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)

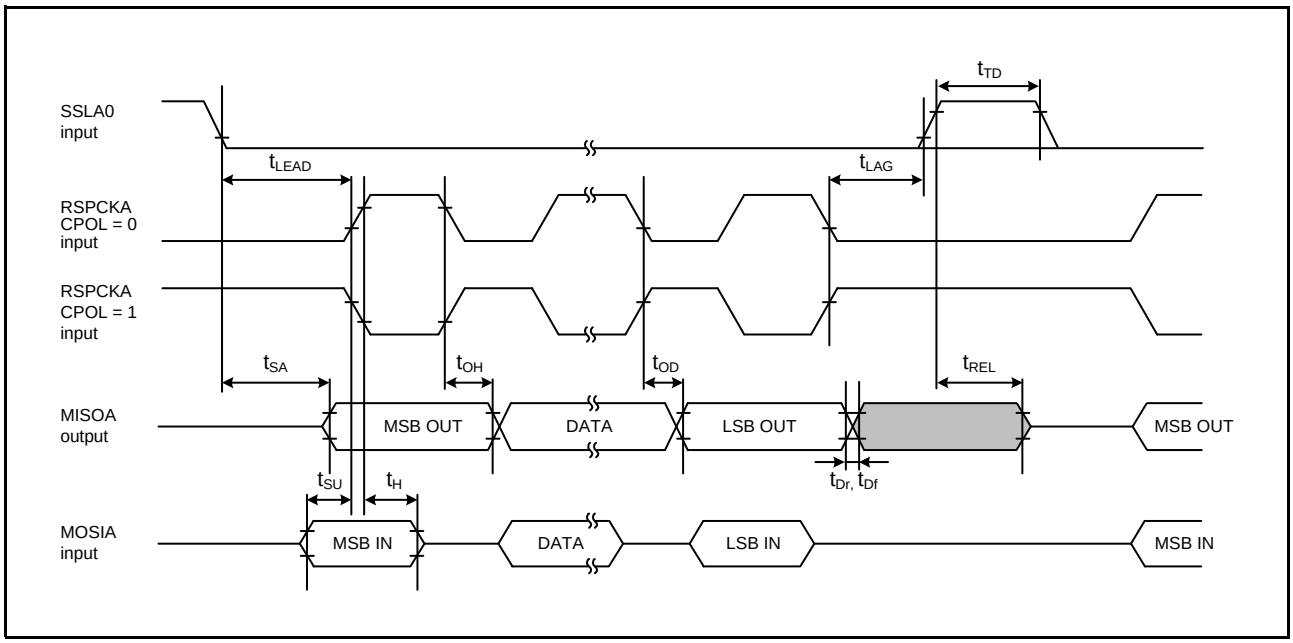


Figure 2.56 RSPI Timing (Slave, CPHA = 0)

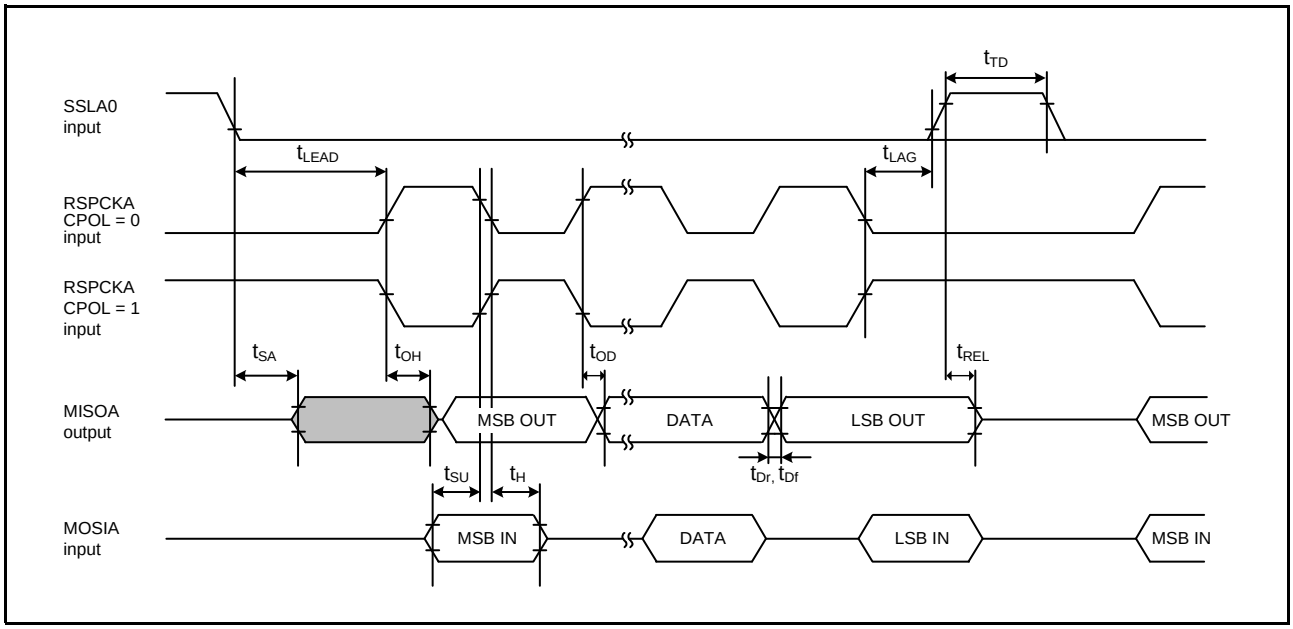


Figure 2.57 RSPI Timing (Slave, CPHA = 1)

2.4.6.11 RIIC

Table 2.41 RIIC Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.*1	Max.	Unit	Test Conditions*3
RIIC (Standard-mode, SMBus)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.58
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. C_b is the total capacitance of the bus lines.
Note 3. When VCC ≥ 4.5V, VOLSR.RICVLS = 0
When VCC < 4.5V, VOLSR.RICVLS = 1

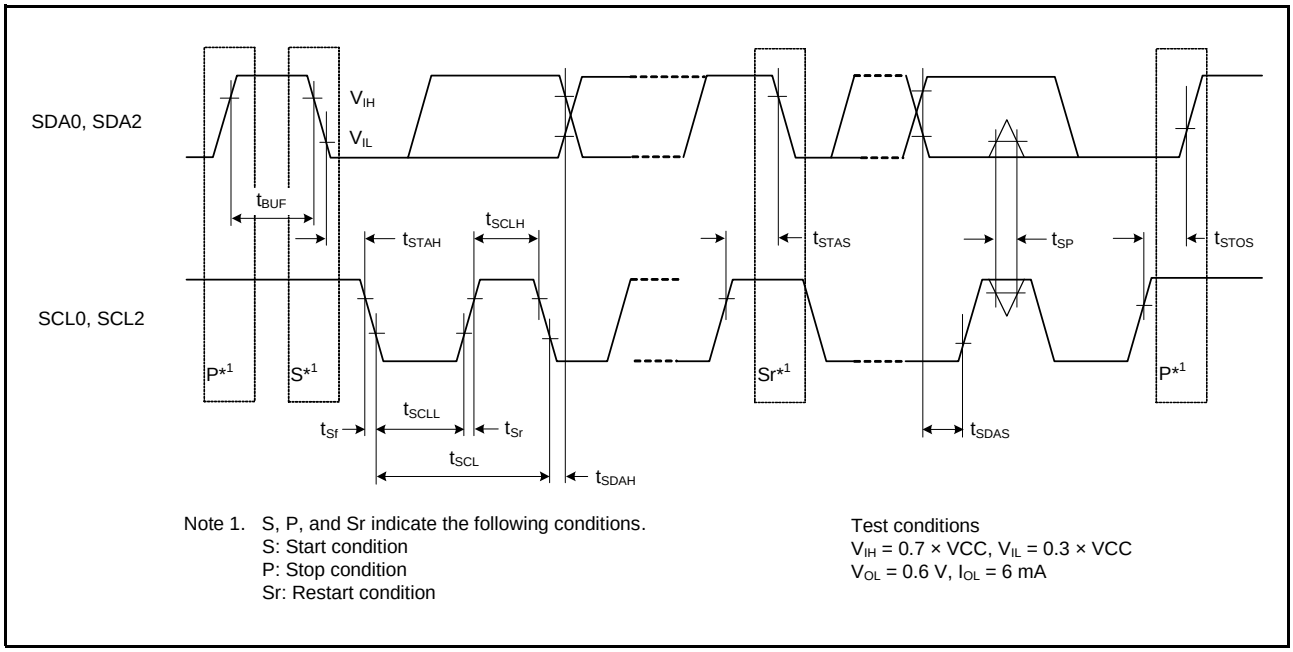


Figure 2.58 RIIC Bus Interface Input/Output Timing

2.4.6.12 CANFD

Table 2.42 CANFD Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Max.	Unit
Classic CAN mode	Bit rate for communications		—	1	Mbps
CAN FD mode	Bit rate for communications		—	1	
	Bit rate for communications (only for data)		—	5	

2.5 A/D Conversion Characteristics

Table 2.43 12-Bit A/D Conversion Characteristics (1)

Conditions: VCC = 2.7 to 5.5 V, 3.0 V ≤ AVCC0 ≤ 5.5 V, AVCC0 – 1.0 ≤ VREFH0 ≤ AVCC0, 3.0 V ≤ VREFH0,
VSS = AVSS0 = VREFL0 = 0 V, $T_a = T_{opr}$, Source impedance = 1.0 kΩ,
The VREFH0 and VREFL0 pins are selected as the reference voltage (ADVREFCR.VREFSEL bit = 1).

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Analog input capacitance		—	—	30	pF	
Conversion time*1 (Operation at PCLKD = 60 MHz)	AN000 to AN007	0.90 (0.50)*2	—	—	µs	Sampling in 30 states
	AN008 to AN015	0.95 (0.55)*2	—	—		Sampling in 33 states
	AN017, AN019, AN021, AN023	0.95 (0.55)*2	—	—		Sampling in 33 states
	AN016, AN018, AN020, AN022	1.05 (0.65)*2	—	—		Sampling in 39 states
Offset error		—	±1.5	±5.0	LSB	
Full-scale error		—	±1.5	±4.5		
Quantization error		—	±0.5	—		
Absolute accuracy		—	±2.5	±5.5		
DNL differential nonlinearity error		—	±1.0	±1.5		
INL integral nonlinearity error		—	±1.5	±2.5		

Note: The characteristics apply when no pin functions other than A/D converter input are used. The absolute accuracy includes the quantization error. The offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error does not include the quantization error.

Note 1. The conversion time includes the sampling time and the comparison time. The numbers of sampling states is indicated as test conditions for the respective items.

Note 2. The value in parentheses indicates the sampling time.

Table 2.44 12-Bit A/D Conversion Characteristics (2) (144-Pin Products)

Conditions: VCC = 2.7 to 5.5 V, 3.0 V ≤ AVCC0 ≤ 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$, Source impedance = 1.0 kΩ,
The AVCC0 and AVSS0 pins are selected as the reference voltage (ADVREFCR.VREFSEL bit = 0).

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Analog input capacitance		—	—	30	pF	
Conversion time*1 (Operation at PCLKD = 60 MHz)	AN000 to AN007	0.90 (0.50)*2	—	—	µs	Sampling in 30 states
	AN008 to AN015	0.95 (0.55)*2	—	—		Sampling in 33 states
	AN017, AN019, AN021, AN023	0.95 (0.55)*2	—	—		Sampling in 33 states
	AN016, AN018, AN020, AN022	1.05 (0.65)*2	—	—		Sampling in 39 states
Conversion time*1 (Operation at PCLKD = 30 MHz)	AN000 to AN007	1.30 (0.50)*2	—	—	µs	Sampling in 15 states
	AN008 to AN015	1.39 (0.60)*2	—	—		Sampling in 18 states
	AN017, AN019, AN021, AN023	1.39 (0.60)*2	—	—		Sampling in 18 states
	AN016, AN018, AN020, AN022	1.49 (0.70)*2	—	—		Sampling in 21 states
Offset error	Operation at PCLKD = 60 MHz	—	±4.0	—	LSB	
	Operation at PCLKD = 30 MHz	—	±1.5	—		
Full-scale error	Operation at PCLKD = 60 MHz	—	±2.5	—		
	Operation at PCLKD = 30 MHz	—	±1.5	—		
Quantization error		—	±0.5	—		
Absolute accuracy	Operation at PCLKD = 60 MHz	—	±7.0	—		
	Operation at PCLKD = 30 MHz	—	±4.0	—		
DNL differential nonlinearity error	Operation at PCLKD = 60 MHz	—	±4.0	—		
	Operation at PCLKD = 30 MHz	—	±1.0	—		
INL integral nonlinearity error	Operation at PCLKD = 60 MHz	—	±4.0	—		
	Operation at PCLKD = 30 MHz	—	±1.5	—		

Note: The characteristics apply when no pin functions other than A/D converter input are used. The absolute accuracy includes the quantization error. The offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error does not include the quantization error.

Note 1. The conversion time includes the sampling time and the comparison time. The numbers of sampling states is indicated as test conditions for the respective items.

Note 2. The value in parentheses indicates the sampling time.

Table 2.45 12-Bit A/D Conversion Characteristics (2) (100-, 80-, and 64-Pin Products)

Conditions: VCC = 2.7 to 5.5 V, 3.0 V ≤ AVCC0 ≤ 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$, Source impedance = 1.0 kΩ,
The AVCC0 and AVSS0 pins are selected as the reference voltage (ADVREFCR.VREFSEL bit = 0).

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Analog input capacitance		—	—	30	pF	
Conversion time*1 (Operation at PCLKD = 60 MHz)	AN000 to AN007	0.90 (0.50)*2	—	—	µs	Sampling in 30 states
	AN008 to AN015	0.95 (0.55)*2	—	—		Sampling in 33 states
	AN017, AN019, AN021, AN023	0.95 (0.55)*2	—	—		Sampling in 33 states
	AN016, AN018, AN020, AN022	1.05 (0.65)*2	—	—		Sampling in 39 states
Conversion time*1 (Operation at PCLKD = 30 MHz)	AN000 to AN007	1.30 (0.50)*2	—	—	µs	Sampling in 15 states
	AN008 to AN015	1.39 (0.60)*2	—	—		Sampling in 18 states
	AN017, AN019, AN021, AN023	1.39 (0.60)*2	—	—		Sampling in 18 states
	AN016, AN018, AN020, AN022	1.49 (0.70)*2	—	—		Sampling in 21 states
Offset error	Operation at PCLKD = 60 MHz	—	±2.5	—	LSB	
	Operation at PCLKD = 30 MHz	—	±1.5	—		
Full-scale error	Operation at PCLKD = 60 MHz	—	±2.5	—		
	Operation at PCLKD = 30 MHz	—	±1.5	—		
Quantization error		—	±0.5	—		
Absolute accuracy	Operation at PCLKD = 60 MHz	—	±4.5	—		
	Operation at PCLKD = 30 MHz	—	±2.5	—		
DNL differential nonlinearity error	Operation at PCLKD = 60 MHz	—	±1.5	—		
	Operation at PCLKD = 30 MHz	—	±1.0	—		
INL integral nonlinearity error	Operation at PCLKD = 60 MHz	—	±2.5	—		
	Operation at PCLKD = 30 MHz	—	±1.5	—		

Note: The characteristics apply when no pin functions other than A/D converter input are used. The absolute accuracy includes the quantization error. The offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error does not include the quantization error.

Note 1. The conversion time includes the sampling time and the comparison time. The numbers of sampling states is indicated as test conditions for the respective items.

Note 2. The value in parentheses indicates the sampling time.

Table 2.46 12-Bit A/D Conversion Characteristics (2) (48-Pin Products)

Conditions: VCC = 2.7 to 5.5 V, 3.0 V ≤ AVCC0 ≤ 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$, Source impedance = 1.0 kΩ,
The AVCC0 and AVSS0 pins are selected as the reference voltage (ADVREFCR.VREFSEL bit = 0).

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Analog input capacitance		—	—	30	pF	
Conversion time*1 (Operation at PCLKD = 60 MHz)	AN000 to AN002, AN005 to AN007	0.90 (0.50)*2	—	—	µs	Sampling in 30 states
	AN009 to AN012	0.95 (0.55)*2	—	—		Sampling in 33 states
Offset error		—	±1.5	—	LSB	
Full-scale error		—	±1.5	—		
Quantization error		—	±0.5	—		
Absolute accuracy		—	±2.5	—		
DNL differential nonlinearity error		—	±1.0	—		
INL integral nonlinearity error		—	±1.5	—		

Note: The characteristics apply when no pin functions other than A/D converter input are used. The absolute accuracy includes the quantization error. The offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error does not include the quantization error.
Note 1. The conversion time includes the sampling time and the comparison time. The numbers of sampling states is indicated as test conditions for the respective items.
Note 2. The value in parentheses indicates the sampling time.

Table 2.47 A/D Internal Reference Voltage Characteristics

Conditions: VCC = 2.7 to 5.5 V, 3.0 V ≤ AVCC0 ≤ 5.5 V, AVCC0 – 1.0 ≤ VREFH0 ≤ AVCC0, 3.0 V ≤ VREFH0,
VSS = AVSS0 = VREFL0 = 0 V, $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.20	1.25	1.30	V	

Note: The above specification values apply during normal operations.

2.6 D/A Conversion Characteristics

Table 2.48 D/A Conversion Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	12	12	12	Bit	
Absolute accuracy	—	—	±6.0	LSB	2-MΩ resistive load 10-bit conversion
Differential nonlinearity error (DNL)	—	±1.0	±2.0	LSB	2-MΩ resistive load
Output resistance (R_O)	—	5.7	—	kΩ	
Conversion time	—	—	3	µs	20-pF capacitive load

2.7 Temperature Sensor Characteristics

Table 2.49 Temperature Sensor Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	–2.0	—	mV/°C	
Output voltage	—	0.63	—	V	T_a = 25°C
Temperature sensor start time	—	—	200	µs	
Sampling time*1	3	—	—	µs	

Note 1. Set the S12AD.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

2.8 Comparator Characteristics

Table 2.50 Comparator Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input offset voltage	V_{IO}	—	8	40	mV	
Reference input voltage range	V_{ref}	0	—	VCC	V	
Analog input voltage rang	V_{ain}	0	—	VCC	V	
Response time	$t_{tot(r)}$	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS[1:0] = 00b Figure 2.59
	$t_{tot(f)}$	—	—	200		
Waiting time for stabilization following switching of the input	t_{cwait}	300	—	—	ns	
Operation stabilization time	t_{cmp}	—	—	1	µs	

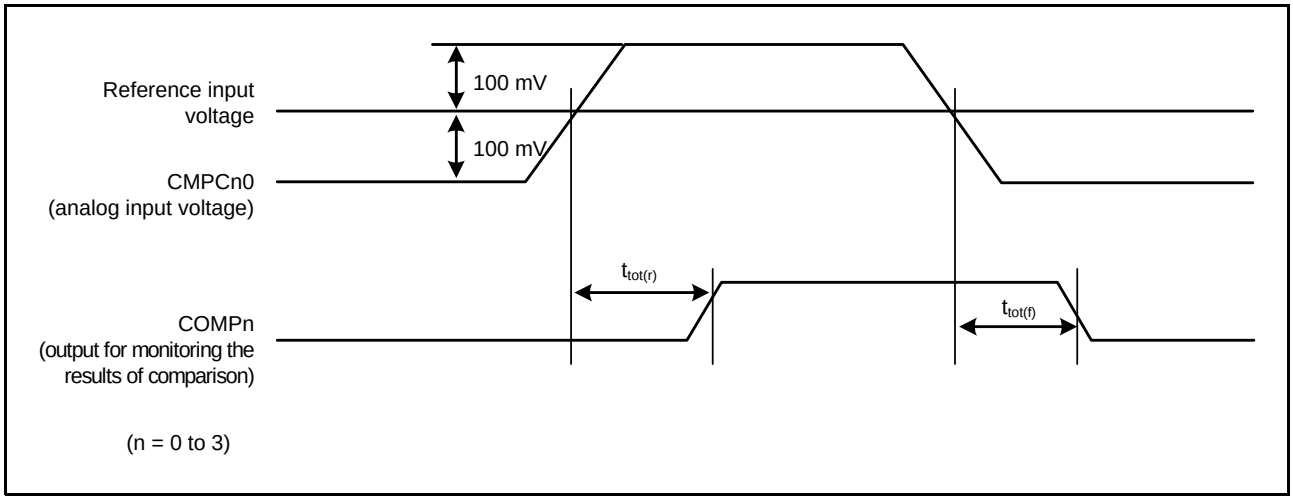


Figure 2.59 Comparator Response Time

2.9 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 2.51 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.46	2.58	2.70	V	Figure 2.60
	Voltage detection circuit (LVD0)	V_{det0_1}	4.04	4.22	4.40		Figure 2.61
		V_{det0_2}	2.71	2.83	2.95		
	Voltage detection circuit (LVD1)	V_{det1_0}	4.39	4.57	4.75		Figure 2.62
		V_{det1_1}	4.29	4.47	4.65		
		V_{det1_2}	4.14	4.32	4.50		
		V_{det1_3}	2.81	2.93	3.05		
		V_{det1_4}	2.76	2.88	3.00		
	Voltage detection circuit (LVD2)	V_{det2_0}	4.39	4.57	4.75		Figure 2.63
		V_{det2_1}	4.29	4.47	4.65		
		V_{det2_2}	4.14	4.32	4.50		
		V_{det2_3}	2.81	2.93	3.05		
		V_{det2_4}	2.76	2.88	3.00		
Internal reset time	Power-on reset time	t_{POR}	—	15.5	—	ms	Figure 2.60
	LVD0 reset time	t_{LVD0}	—	0.70	—		Figure 2.61
	LVD1 reset time	t_{LVD1}	—	0.57	—		Figure 2.62
	LVD2 reset time	t_{LVD2}	—	0.57	—		Figure 2.63
Minimum VCC down time		t_{VOFF}	200	—	—	µs	Figure 2.60, Figure 2.61
Response delay time		t_{det}	—	—	200	µs	Figure 2.60 to Figure 2.63
LVD operation stabilization time (after LVD is enabled)		$t_{d(E-A)}$	—	—	20	µs	Figure 2.62, Figure 2.63
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

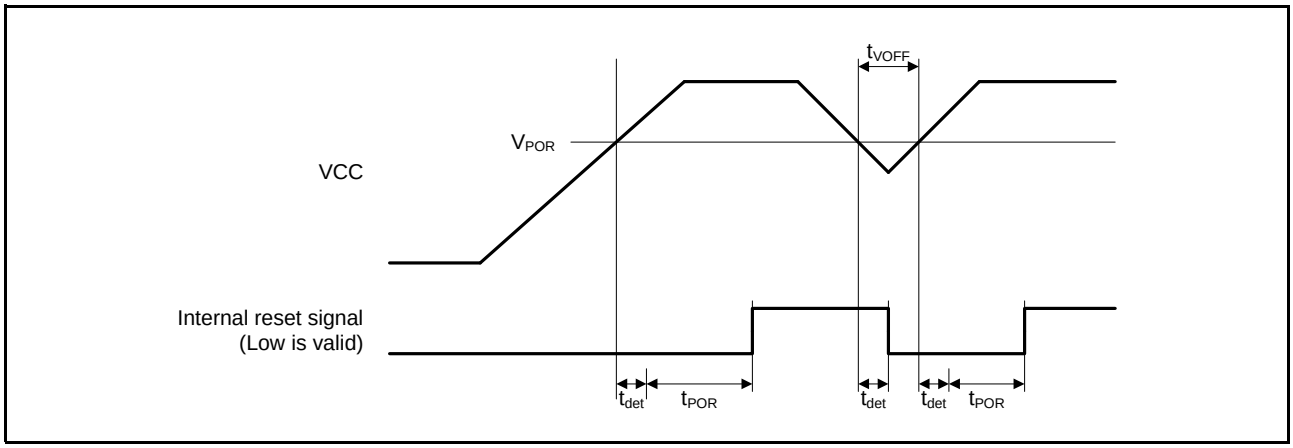


Figure 2.60 Power-on Reset Timing

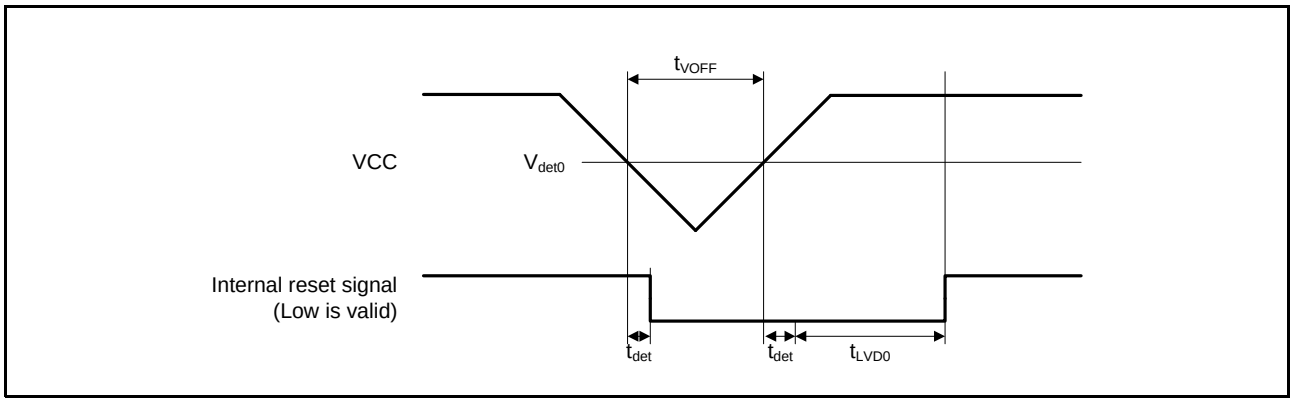


Figure 2.61 Voltage Detection Circuit Timing (V_{det0})

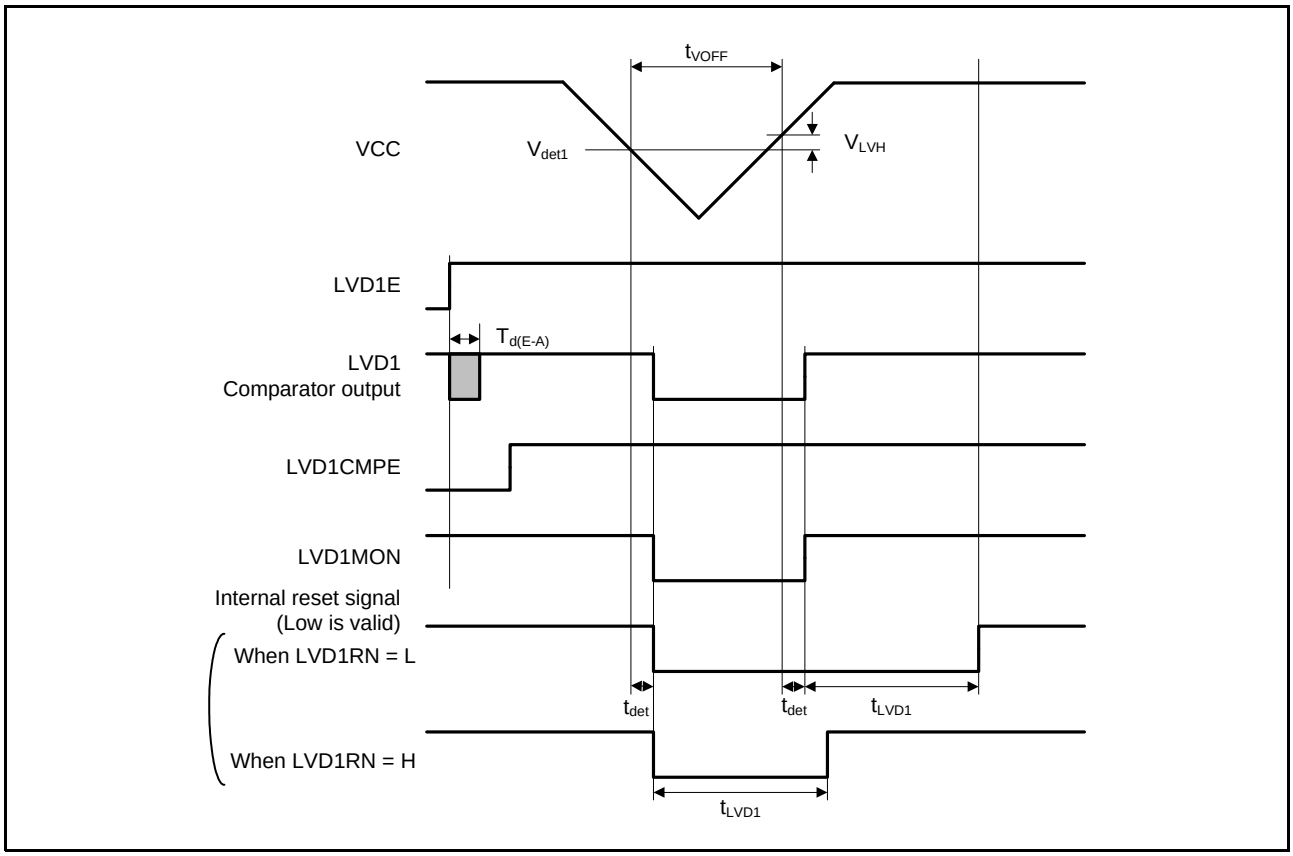


Figure 2.62 Voltage Detection Circuit Timing (V_{det1})

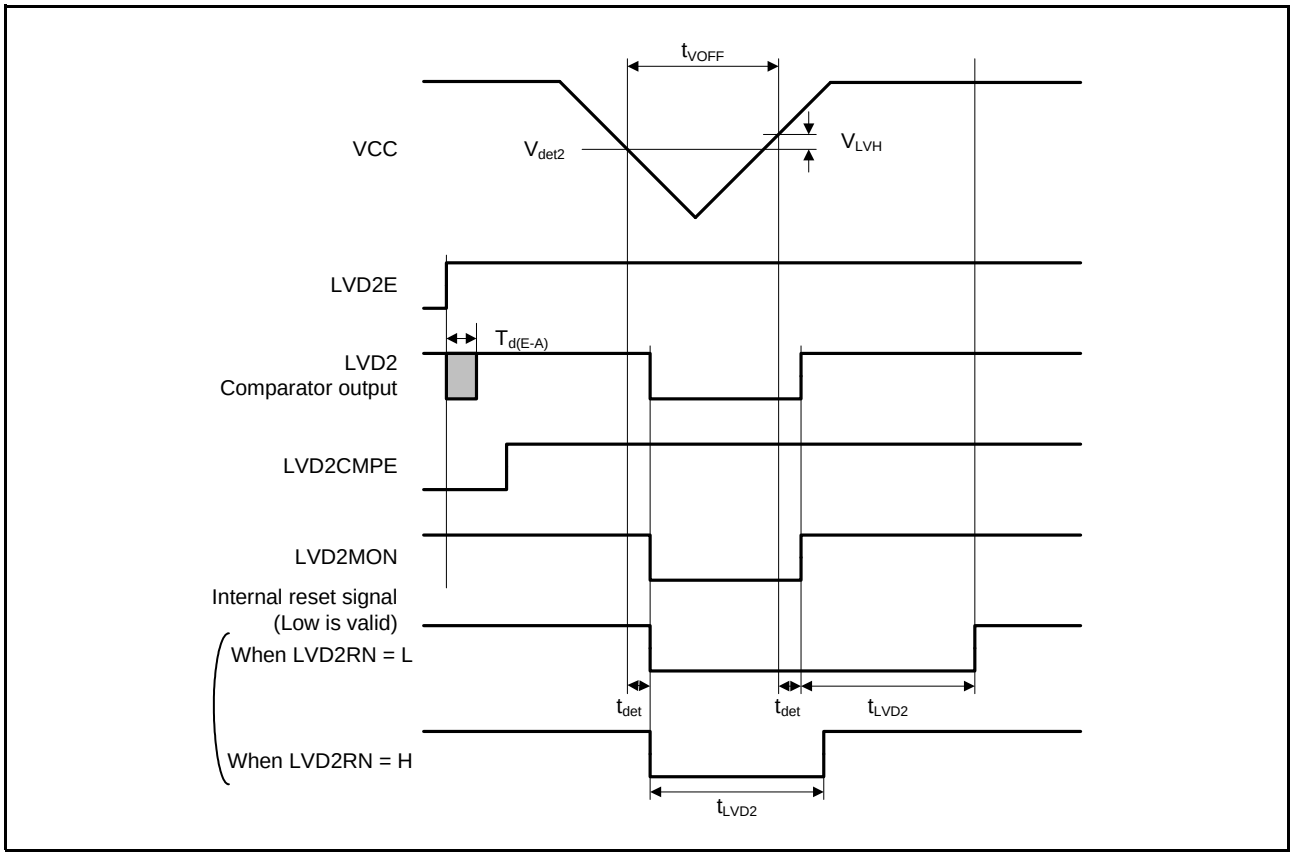


Figure 2.63 Voltage Detection Circuit Timing (V_{det2})

2.10 Oscillation Stop Detection Timing

Table 2.52 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.64

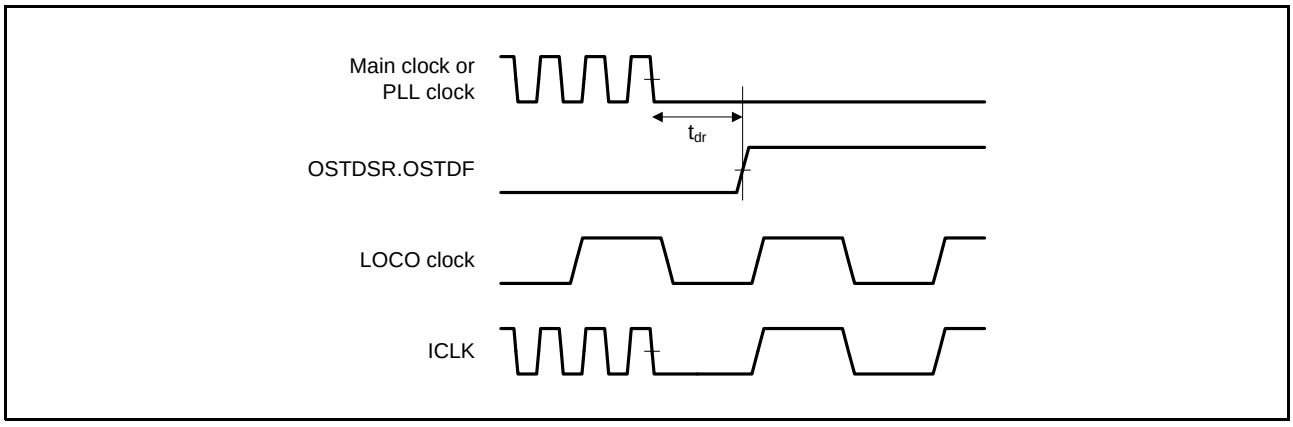


Figure 2.64 Oscillation Stop Detection Timing

2.11 Flash Memory Characteristics

Table 2.53 Code Flash Memory Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time N_{PEC} ≤ 100 times	256 bytes	t_{P256}	—	0.9	13.2	—	0.4	6	ms	
	8 Kbytes	t_{P8K}	—	29	176	—	13	80	ms	
	32 Kbytes	t_{P32K}	—	116	704	—	52	320	ms	
Programming time N_{PEC} > 100 times	256 bytes	t_{P256}	—	1.1	15.8	—	0.5	7.2	ms	
	8 Kbytes	t_{P8K}	—	35	212	—	16	96	ms	
	32 Kbytes	t_{P32K}	—	140	848	—	64	384	ms	
Erasure time N_{PEC} ≤ 100 times	8 Kbytes	t_{E8K}	—	71	216	—	39	120	ms	
	32 Kbytes	t_{E32K}	—	254	864	—	141	480	ms	
Erasure time N_{PEC} > 100 times	8 Kbytes	t_{E8K}	—	85	260	—	47	144	ms	
	32 Kbytes	t_{E32K}	—	304	1040	—	169	576	ms	
Reprogramming/erasure cycle*1		N_{PEC}	1000*2	—	—	1000*2	—	—	Times	
Suspend delay time during programming		t_{SPD}	—	—	264	—	—	120	µs	
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	216	—	—	120	µs	
Second suspend delay time during erasure (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay time during erasure (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	ms	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*3, *4		t_{DRP}	20	—	—	20	—	—	Year	T_a ≤ 85°C
			10	—	—	10	—	—		T_a ≤ 105°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 256-byte program is performed 32 times for different addresses in 8-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

Table 2.54 Data Flash Memory Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = 3.0 to 5.5 V,
VSS = AVSS0 = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
Erasure time	64 bytes	t_{DP64}	—	3.1	18	—	1.7	10	ms	
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	30	µs	
	64 bytes	t_{DBC64}	—	—	280	—	—	100	µs	
	2 Kbytes	t_{DBC2K}	—	—	6160	—	—	2200	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	Times	
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	120	µs	
First suspend delay time during erasure (in suspend priority mode)		t_{DSESD1}	—	—	216	—	—	120	µs	
Second suspend delay time during erasure (in suspend priority mode)		t_{DSESD2}	—	—	300	—	—	300	µs	
Suspend delay time during erasure (in erasure priority mode)		t_{DSEED}	—	—	300	—	—	300	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*3, *4		t_{DDRP}	20	—	—	20	—	—	Year	$T_a \leq 85°C$
			10	—	—	10	—	—		$T_a \leq 105°C$

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 512 times for different addresses in 2-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

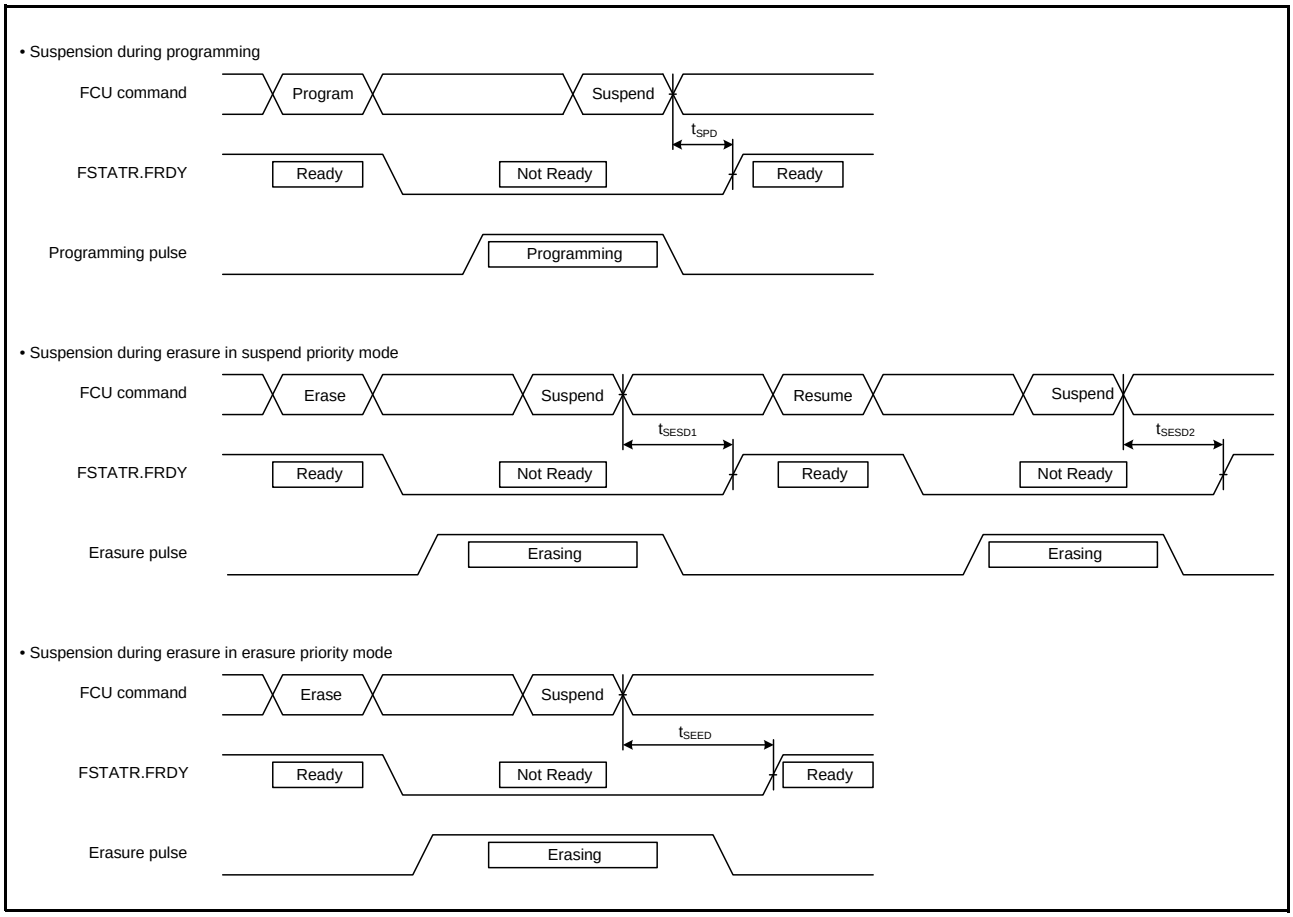


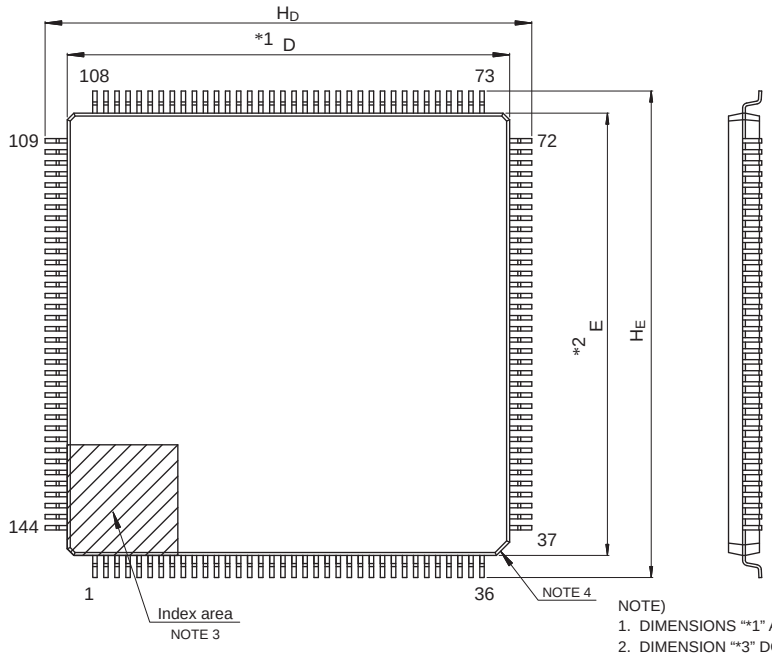
Figure 2.65 Flash Memory Programming/Erasure Suspension Timing

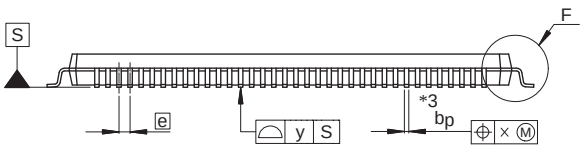
Appendix 1. Package Dimensions

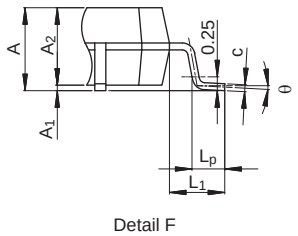
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm







Detail F

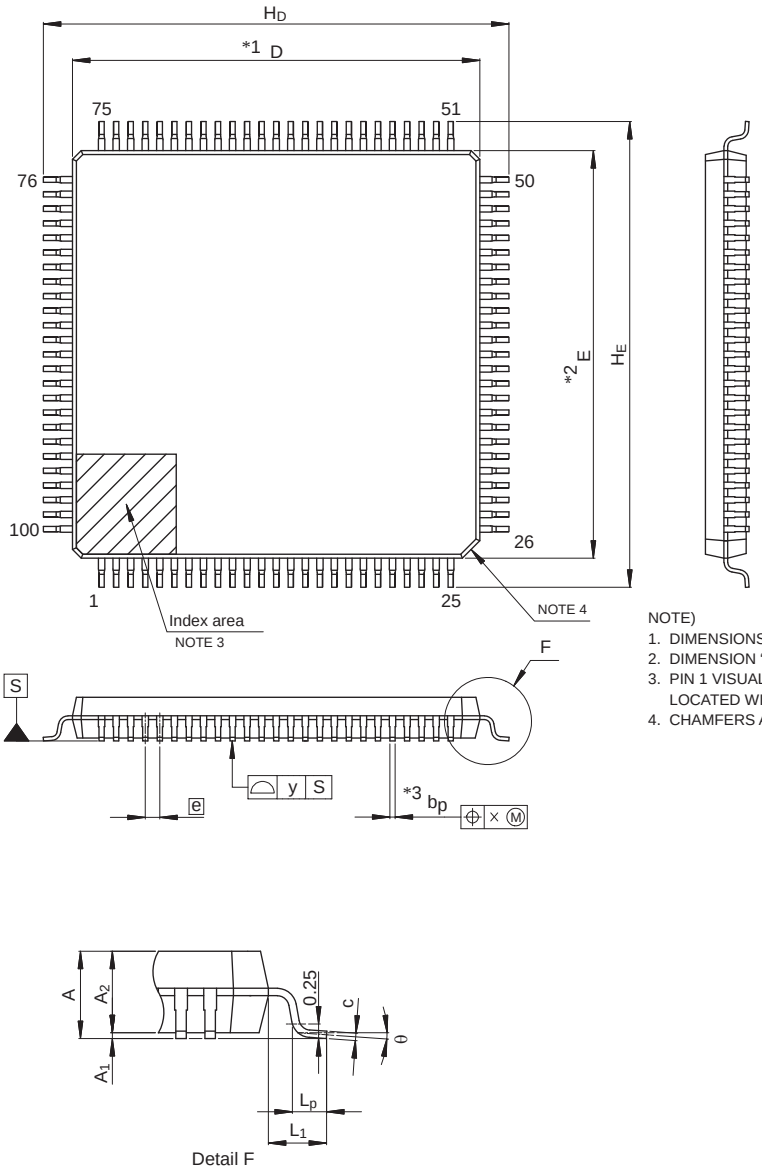
NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A 144-Pin LFQFP (PLQP0144KA-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



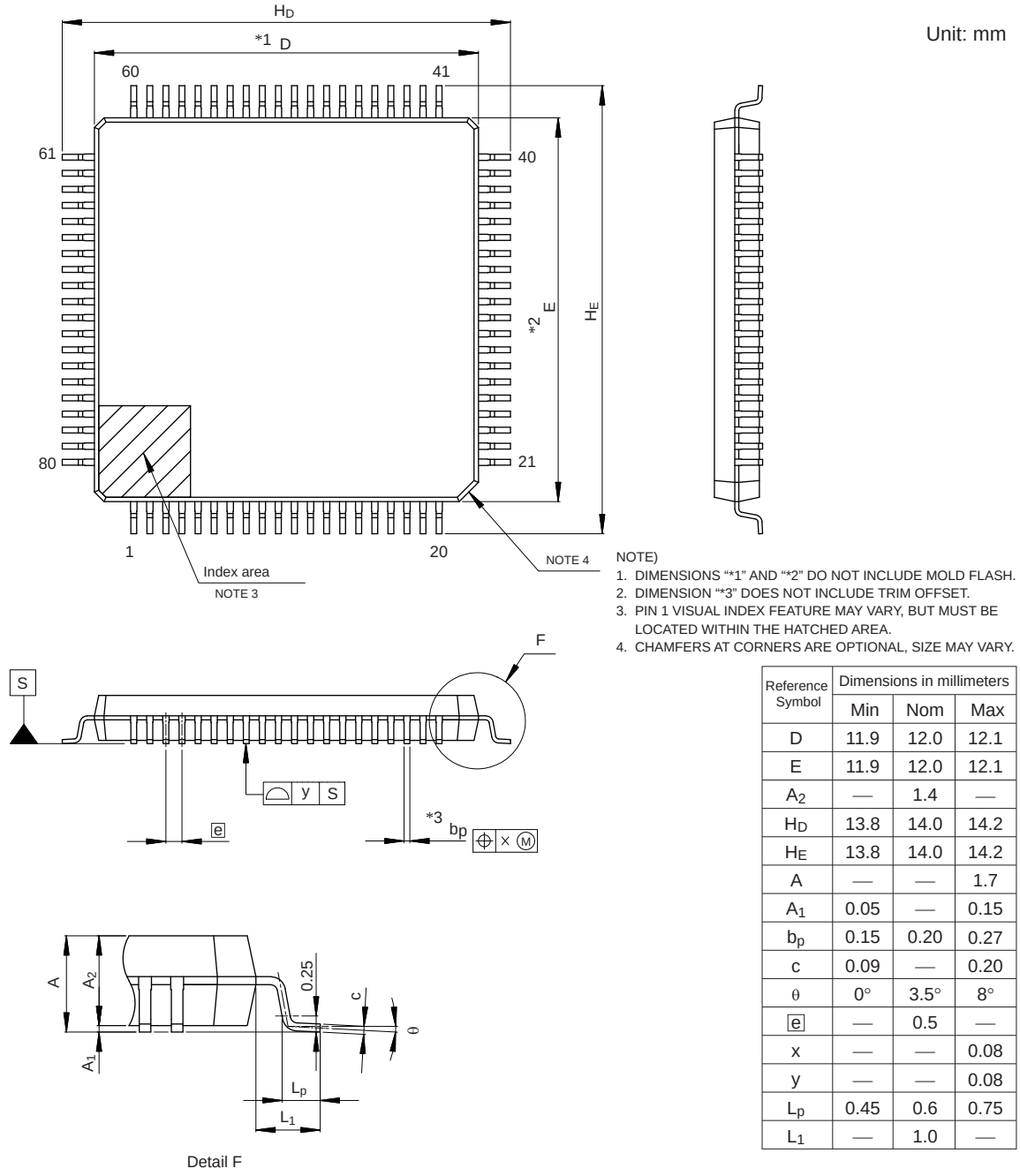
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure B 100-Pin LFQFP (PLQP0100KB-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5

Unit: mm



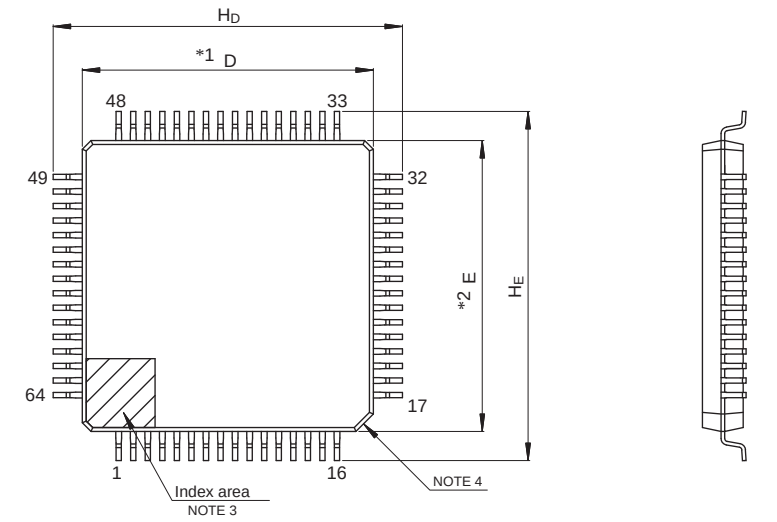
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

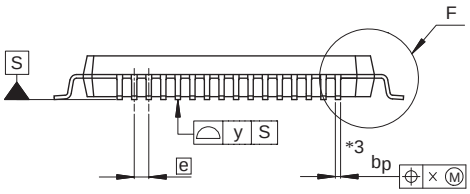
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

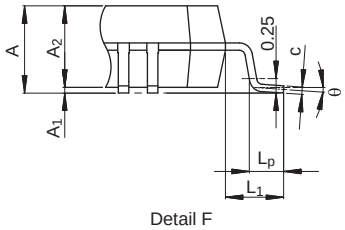
Figure C 80-Pin LFQFP (PLQP0080KB-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm







Detail F

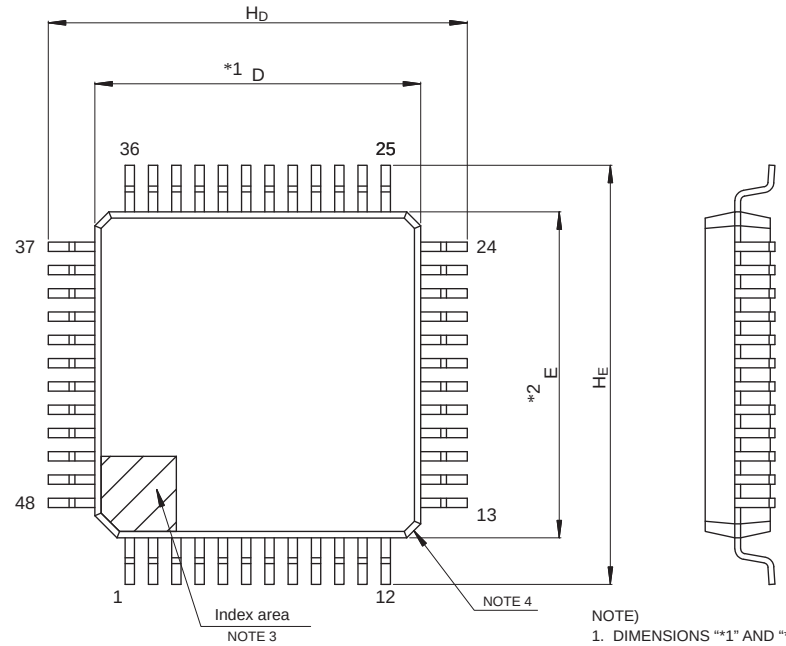
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

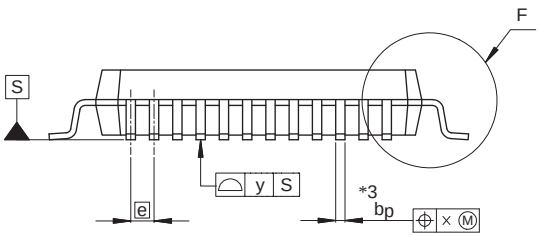
Figure D 64-Pin LFQFP (PLQP0064KB-C)

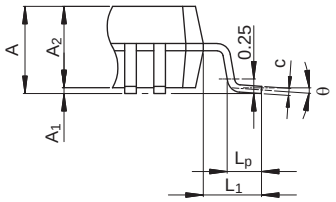
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.





Detail F

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure E 48-Pin LFQFP (PLQP0048KB-B)

REVISION HISTORY	RX660 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Mar 18, 2022	—	First edition, issued	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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