JST12/JST12i Series 12A TRIACs

DESCRIPTION:

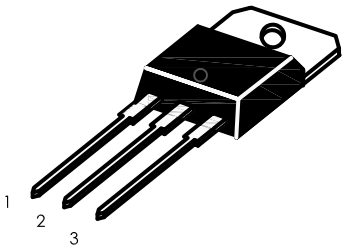
high current density due to double mesa technology; SIPOS and Glass Passivation.

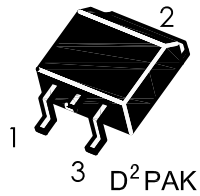
JST12/JST12i series triacs is suitable for general purpose AC switching. They can be used as an ON/OFF Function in applications such as static relays, heating regulation, induction motor stating circuits... or for phase contol operation light dimmers, motorspeed controllers.

JST12/JST12i-×××TW、-×××SW、-×××CW、-×××BW are 3 Quadrants triacs, They are specially recommended for use on inductive loads.

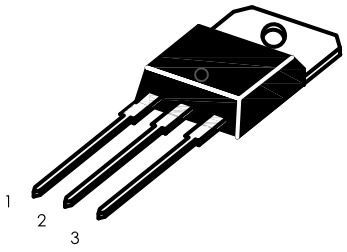
JST12i are isolated internally, they provides a 2500V RMS isolation voltage from all three terminals to extemal heetsink.

TO-220AB(JST12)

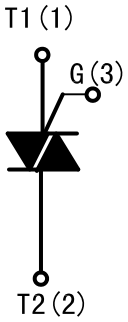




D^2PAK



TO-220AB insulated
(JST12i)



MAIN FEATURES

Symbol	Value	Unit
$I_{T(RMS)}$	12	A
V_{DRM}/V_{RRM}	600and800	V
V_{TM}	≤1.55	V

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Storage junction temperature range Operrating junction temperature range		Tstg Tj	-40 to +150 -40 to +125	℃
Repetitive Peak Off-state Voltage Repetitive Peak Reverse Voltage	Tj=25℃	V_{DRM} V_{RRM}	600and800 600and800	V
Non repetitive Surge Peak Off-state Voltage Non repetitive Peak Reverse Voltage	Tj=25℃	V_{DSM} V_{RSM}	700and900 700and900	V
RMS on-state current (full sine wave)	D^2PAK / TO-220AB Tc=105℃ TO-220AB Ins Tc=90℃	$I_{T(RMS)}$	12	A
Non repetitive surge peak on-state current (full cycle, Tj=25℃)	f = 50 Hz t=20ms f = 60 Hz t=16.7ms	I_{TSM}	120 126	A
I^2t Value for fusing	tp=10ms	I^2t	78	A^2s
Critical rate of rise of on-state current $I_G=2\times I_{GT}$, tr≤100 ns, f=120Hz, Tj=125℃		dI /dt	50	A/us
Peak gate current	tp=20us, Tj=125℃	I_{GM}	4	A
Average gate power dissipation	Tj=125℃	$P_{G(AV)}$	1	W

ELECTRICAL CHARACTERISTICS(Tj=25℃ unless otherwise specified)

● 3 Quadrants

Symbol	Test Condition	Quadrant		JST12/JST12i				Unit
				TW	SW	CW	BW	
I_{GT}	V_D=12V R_L=30Ω	I - II - III	MAX.	5	10	35	50	mA
V_{GT}		I - II - III	MAX.	1.3				V
V_{GD}	V_D=V_{DRM} R_L=3.3KΩ Tj=125℃	I - II - III	MIN..	0.2				V
I_L	I_G=1.2I_{GT}	I - III	MAX.	10	25	50	70	mA
		II		15	30	60	80	
I_H	I_T=100mA		MAX.	10	15	35	50	mA
dV/dt	V_D=67%V_{DRM} gate open Tj=125℃		MIN.	20	40	500	1000	V/μs
(dI/dt)c	(dV/dt) c=0.1V/μs Tj=125℃		MIN.	3.5	6.5	----	----	A/ms
	(dV/dt) c=10V/μs Tj=125℃			1.0	2.9	----	----	
	Without snubber Tj=125℃			----	----	6.5	12	

● 4 Quadrants

Symbol	Test Condition	Quadrant		JST12/JST12i		Unit
				C	B	
I_{GT}	V_D=12V R_L=30Ω	I - II - III IV	MAX.	25 50	50 100	mA
V_{GT}		ALL	MAX.	1.3		V
V_{GD}	V_D=V_{DRM} R_L=3.3KΩ Tj=125℃	ALL	MIN.	0.2		V
I_L	I_G=1.2I_{GT}	I - III - IV	MAX.	40	50	mA
		II		80	100	
I_H	I_T=100mA		MAX.	25	50	mA
dV/dt	V_D=67%V_{DRM} gate open Tj=125℃		MIN.	200	400	V/μs
(dI/dt)c	(dV/dt) c=0.1V/μs Tj=125℃		MIN.	----	----	
	(dV/dt) c=10V/μs Tj=125℃			----	----	
	Without snubber Tj=125℃			----	----	

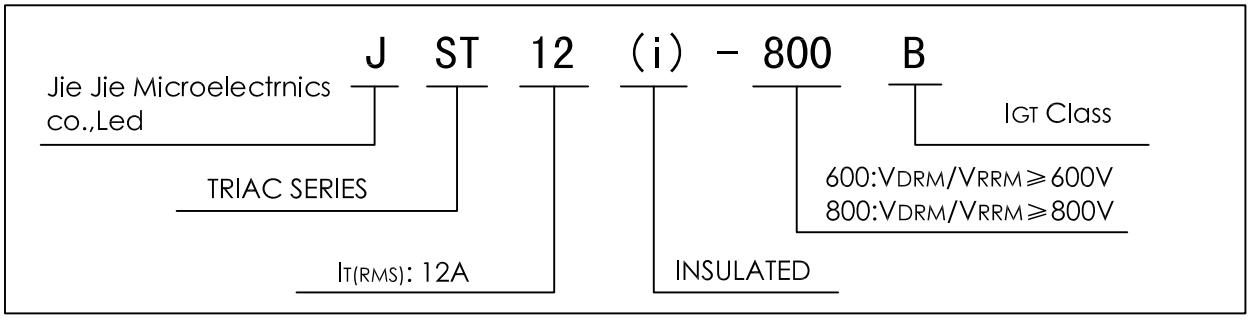
STATIC CHARACTERISTICS

Symbol	Test Conditions		Value (MAX)	Unit
V_{TM}	I_{TM}=17A, tp=380uS	Tj=25℃	1.55	V
I_{DRM}	$V_D=V_{DRM}$	Tj=25℃	5	uA
I_{RRM}	$V_R=V_{RRM}$	Tj=125℃	1	mA

THERMAL RESISTANCES

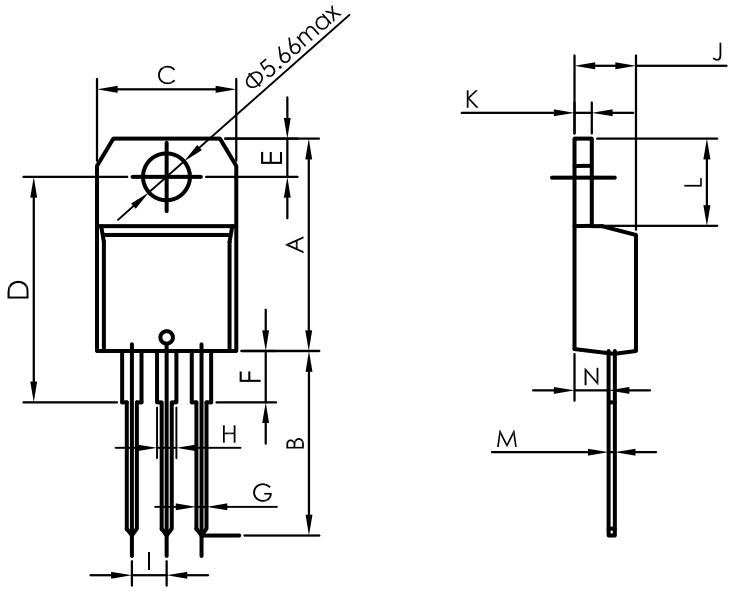
Symbol	Parameter		Value	Unit
Rth(j-c)	Junction to case (AC)	D^2PAK/TO-220AB	1.4	℃/W
		TO-220AB Insulated	2.3	

ORDERING INFORMATION



PACKAGE MECHANICAL DATA

TO-220AB

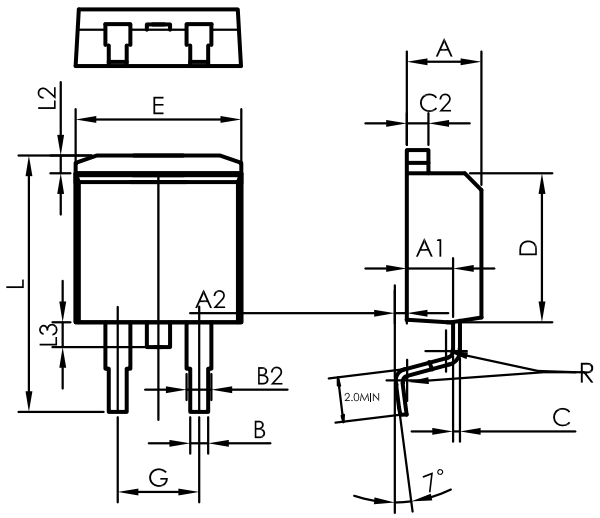


T1T2G

DIMENSIONS (mm)

	A	B	C	D	E	F	G	H	I	J	K	L	M	N
MAX	15.9	14.0	10.4	16.8	2.95		0.88	1.70	2.70	4.60	1.32	6.60	0.70	2.72
TYP				16.4		3.75								
MIN	15.2	13.0	10.0	15.8	2.65		0.61	1.14	2.40	4.40	1.23	6.20	0.49	2.40

D2PAK



DIMENSIONS (mm)

	A	A1	A2	B	B2	C	C2	D	E	G	L	L2	L3	R
MIN	4.30	2.49	0.03	0.70	1.25	0.45	1.21	8.95	10.0	4.88	15.0	1.27	1.40	
TYP					1.40									0.40
MAX	4.60	2.69	0.23	0.93		0.60	1.36	9.35	10.28	5.28	15.85	1.40	1.75	

Fig. 1: Maximum power dissipation versus RMS on-state current(full cycle)

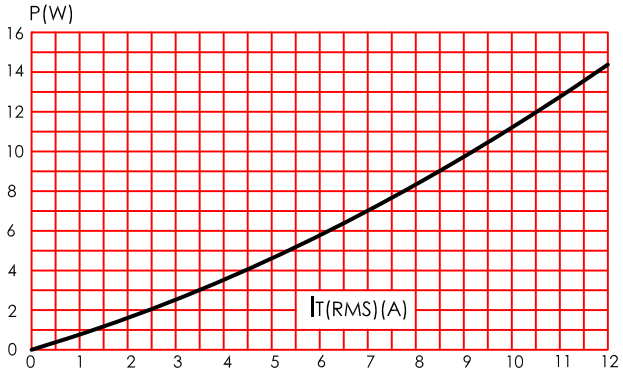


Fig. 2: RMS on-state current versus case temperrature(full cycle)

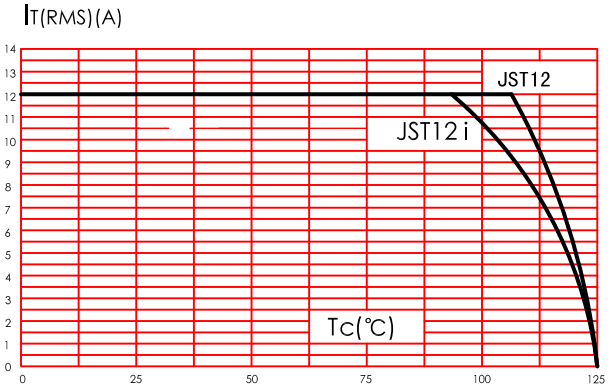


Fig. 3: on-state characteristics (maximum values)

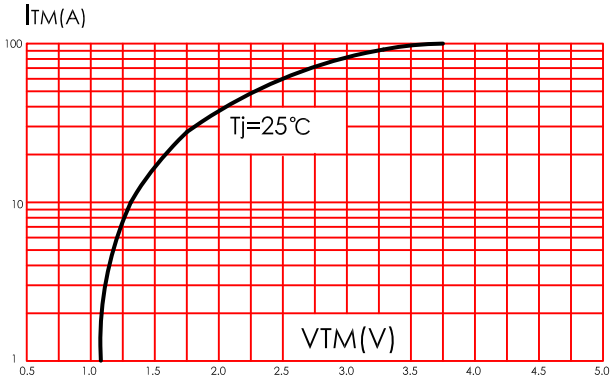


Fig. 4: Surge peak on-state current versus number of cycyles

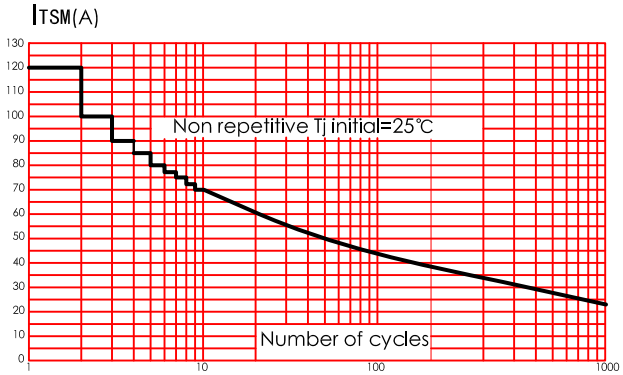


Fig. 5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10mS

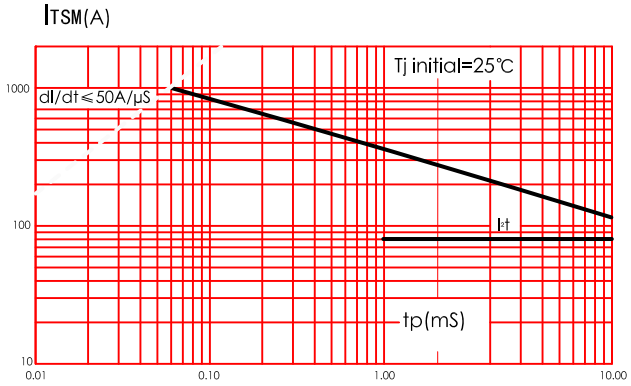


Fig. 6: **Relative variation** of gate trigger currunt, holding current and latching current versus junction temperature(typical values)