

Digital Satellite Network Interface Module 115-T-7121TPA

APPLICATIONS

- Set-Top Box applications for DVB-S and DSS
- Digital Satellite MODEM

FEATURES

- 950 ~ 2150 MHz tuning range
- 1 ~ 45M symbol rate supported, thus suitable for SCPC and MCPC application
- Internal AGC monitor out
- I2C-bus control for tuner PLL and for LINK IC
- Loop through output
- Both parallel and serial output transport stream interface
- 22KHz tone output for LNB and DiSEqC
- Viterbi BER monitoring
- Regulated transport interface, DATA_CLK polarity selection supported
- System clock generation PLL with low frequency external clock

History

| | |
|-----------------|--|
| Initial Release | |
| Release 1.0 | Nov. 15 1999 |
| Release 1.1 | Nov. 5. 2000, port switching @ 1500Mhz |
| Release 1.2 | Feb. 2. 2001, pin#10(PORT2) to GND |

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1. General Specification of RF Tuner¹

1.1 Power Supply

| ITEM | MIN | TYPICAL | MAX | UNIT |
|--------------------|------|---------|------|------|
| 5V Supply Voltage | 4.75 | 5 | 5.25 | V |
| 5V Supply Current | | 230 | 260 | mA |
| Tuning Voltage | 28 | 30 | 33 | V |
| Tuning Current | | | 2 | mA |
| LNB Voltage | | | | |
| LNB Supply Current | | | 500 | mA |

1.2 Ambient Conditions

| ITEM | MIN | TYPICAL | MAX | UNIT |
|-----------------------|-----|---------|-----|------|
| Operating Temperature | 0 | | 60 | °C |
| Storage Temperature | -20 | | 70 | °C |
| Operating Humidity | | | 85 | % |
| Storage Humidity | | | 90 | % |

1.3 Antenna Terminal

- RF Input: f-type, 75Ω
- RF Loop-through: f-type, 75Ω

1.4 Down Conversion

- Broad band IQ down conversion, integrated in ZIF IC

1.5 I/Q Demodulator

- Integrated in ZIF IC

1.6 AGC Voltage

- 0 ~ 5V DC

¹ See Fig. 1 for block diagram.

2. Electrical Specification of RF Tuner

Test Condition

Supply voltage

B+(5V): 5V±0.1V

VT(30V): 28V±0.1V

Ambient temperature: 25°C±5°C

Ambient humidity: 65%±10%

| ITEM | MIN | TYPICAL | MAX | UNIT | CONDITION |
|--|-----|------------|------------|--------|-------------------------|
| 2.1 Input Level | -65 | | -25 | dBm | |
| 2.2 Input VSWR | | 2 | 3 | | |
| 2.3 Noise Figure | | 6 | 12 | dB | |
| 2.4 3 rd Order Inter modulation Rejection Ratio | 40 | | | dB | -25dBm level difference |
| 2.5 Local Oscillation Signal Leakage at RF Input Terminal | | -65 | -50 | dBm | |
| 2.6 Gain Deviation | | 5 | 10 | dB | 950~2150MHz |
| 2.7 Phase Noise @10KHz @100KHz | | -75 -95 | -70 -90 | dBc/Hz | |
| 2.8 I/Q Level Imbalance | | | ±1 | dB | I relative |
| 2.9 I/Q Phase Error | | | ±3 | DEG | |
| 2.10 I/Q Baseband Flatness | | | ±3 | dB | |
| 2.11 I/Q Output Level | | 600 | | mVp-p | 1KΩ, 15pF load |
| 2.12 I/Q Output Impedance | | 250 | | Ω | |

3. Tuner Synthesizer PLL Information

3.1 IC adopted : SP5769

3.2 I2C address: 0xC2, fixed internally

3.3 Write Registers

| | | | | | | | | | | |
|---------------|-------|-----|-----|-----|-----|-----|-----|----|-----|---|
| | | MSB | | | | | | | LSB | |
| Prog. divider | Byte1 | 0 | N14 | N13 | N12 | N11 | N10 | N9 | N8 | A |
| Prog. divider | Byte2 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 | A |
| Control data | Byte3 | 1 | T2 | T1 | T0 | R3 | R2 | R1 | R0 | A |
| Control data | Byte4 | C1 | C0 | RE | RS | P3 | P2 | P1 | P0 | A |

A: Acknowledge bit

N14~N0: Programmable divider bits

$$N = N14 \times 2^{14} + N13 \times 2^{13} + \dots + N1 \times 2^1 + N0$$

R3,R2,R1,R0: Reference Division Ratio(See Table 1)

C0,C1: Charge pump current(See Table 2)

RE, RS: Not used, for normal operation RE=0 and RS=don't care

T2,T1,T0: Test mode control, for normal operation T2=0 and T1=T0=don't care

P3,P2,P1,P0: Port output states, for normal operation P3=P2=P0=don't care, P1 is used for switching local oscillator, i.e. if $f_{LO} < 1500\text{MHz}$ then P1=1, else P1=0

Table 1 Reference Division Ratio (4MHz external reference)

| R3 | R2 | R1 | R0 | Ratio | Comparison frequency |
|----|----|----|----|-------|----------------------|
| 0 | 0 | 0 | 0 | 2 | 2MHz |
| 0 | 0 | 0 | 1 | 4 | 1MHz |
| 0 | 0 | 1 | 0 | 8 | 500KHz |
| 0 | 0 | 1 | 1 | 16 | 250KHz |
| 0 | 1 | 0 | 0 | 32 | 125KHz |
| 0 | 1 | 0 | 1 | 64 | 62.5KHz |
| 0 | 1 | 1 | 0 | 128 | 31.25KHz |
| 0 | 1 | 1 | 1 | 256 | 15.62KHz |
| 1 | 0 | 0 | 0 | 24 | 166.67KHz |
| 1 | 0 | 0 | 1 | 5 | 800KHz |
| 1 | 0 | 1 | 0 | 10 | 400KHz |
| 1 | 0 | 1 | 1 | 20 | 200KHz |
| 1 | 1 | 0 | 0 | 40 | 100KHz |
| 1 | 1 | 0 | 1 | 80 | 50KHz |
| 1 | 1 | 1 | 0 | 160 | 25KHz |
| 1 | 1 | 1 | 1 | 320 | 12.5KHz |

* Recommended, 125KHz

Table 2 Charge Pump Current

| C1 byte 5, bit 1 | C0 byte 5, bit 2 | CURRENT(uA) | | |
|---------------------|---------------------|-------------|---------|-------|
| | | MIN | TYPICAL | MAX |
| 0 | 0 | ±98 | ±130 | ±162 |
| 0 | 1 | ±210 | ±280 | ±350 |
| 1 | 0 | ±450 | ±600 | ±750 |
| 1 | 1 | ±975 | ±1300 | ±1625 |

* Recommended, C1=1, C0=0

Example for determining programmable divider

Desired channel frequency =

LO frequency(f_{LO}) =

1200MHz

if f_{REF} =125KHz

thus ratio = 32, R3=0, R2=1, R1=0, R0=0

then Programmable divider =

$$f_{LO} (1/f_{REF}) =$$

$$(1200.0E6/1)(1/125.0E3) =$$

$$9600 = 0x2580$$

3.4 Read Register

| | | MSB | | | | | | | LSB | |
|-------------|-------|-----|----|---|---|---|---|---|-----|---|
| Status byte | Byte1 | POR | FL | 0 | 0 | 0 | 0 | 0 | 0 | A |

A: Acknowledge bit

POR: Power-On reset indicator

FL: PLL lock flag (FL=1 if locked)

* PLL lock-up time: TBD

4. General Specification of LINK IC²

4.1 IC adopted: HDM8513A³

² See Fig. 2 for block diagram.

³ Register information is not included in this specification, see *HDM8513A Users Manual* for detail

4.2 I2C address: 0xe8, fixed internally

4.3 Power Supply

| | MIN | TYPICAL | MAX | UNIT |
|---------------------|-----|-------------------------------|-----|------|
| 3.3V Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| 3.3V Supply Current | | 367 (@30Msps, 1/2 inner rate) | 420 | mA |

4.4 Ambient Conditions

| ITEM | MIN | TYPICAL | MAX | UNIT |
|-----------------------|-----|---------|-----|------|
| Operating Temperature | -10 | | 70 | °C |
| Storage Temperature | -65 | | 150 | °C |

4.5 LINK IC functionality

| ITEM | DESCRIPTION | NOTE |
|-------------------------|---|-------------|
| ADC | 6 bit dual sigma-delta ADC | 60MHz |
| System Clock Generation | Internal PLL with external reference clock | |
| QPSK Demodulation | <ul style="list-style-type: none"> - Root-raised cosine filter with roll-off 0.35 - Digital carrier recovery loop (autonomous sweep functionality) - Digital symbol recovery loop - Digital AGC (0~3V DC) | |
| Viterbi Decoding | 1/2, 2/3, 3/4, 5/6, 7/8 with constraint length K=7 | 6/7 for DSS |
| Deinterleaving | interleaving depth I=12 | |
| ReedSolomon Decoding | (204, 188, 8) | |
| Descrambling | Energy dispersal descrambling | |
| Viterbi BER Indicator | Number of errors among 2 ²⁰ data bits | |

description.

Maximum symbol rate consideration @60MHz CLK

| Viterbi rate | MAX RATE[Msp/s] | Notes |
|--------------|-----------------|--------------------------------|
| 1/2 | 45 | due to antialiasing limitation |
| 2/3 | 45 | " |
| 3/4 | 40 | due to system clock limitation |
| 5/6 | 36 | " |
| 7/8 | 34.2 | " |

5. Electrical Specification of LINK IC

5.1 BER vs Eb/No characteristics

| INNER RATE | Eb/No THRESHOLD | CRITERION |
|------------|-----------------|--|
| 1/2 | << 4.5dB | Eb/No at BER=2x10 ⁻⁴ @ Viterbi decoder output |
| 2/3 | << 5.0dB | |
| 3/4 | << 5.5dB | |
| 5/6 | << 6.0dB | |
| 7/8 | << 6.4dB | |

6. NIM Configuration⁴

6.1 Host Interface

- Only I2C host interface is supported

6.2 WAGC Configuration

- level translation circuit to adjust dynamic range difference between ZIF IC and LINK IC
- Higher value corresponds to higher gain

6.3 I2C Bypass

- Tuner PLL can be accessed via I2C bypass out of LINK IC(internally connected)

⁴ See Fig. 3 and Fig. 4 for output stream timing diagram.

6.4 Pin Description

| PIN NO. | MARK | DESCRIPTION | CURRENT(typ) | RIPPLE(max) |
|---------|------------|---|--------------|-------------|
| 1 | LNBA | Power input for LNB A | | |
| 2 | LNBB | Power input for LNB B | | |
| 3 | 5V_RF | 5V for RF-AMP and loop through | 20mA | 20mVp-p |
| 4 | AGC | AGC monitor | | |
| 5 | 5V_ZIF | 5V for 2 nd AMP and ZIF IC | * | 20mVp-p |
| 6 | VT | 30V tuning voltage | | |
| 7 | 5V_PLL | 5V for ZIF IC, PLL IC and OSC | * | 20mVp-p |
| 8 | I | I signal monitor | | |
| 9 | Q | Q signal monitor | | |
| 10 | GND | Ground | | |
| A | 5VAGC | Power of AGC AMP | 10mA | 20mVp-p |
| B | GND | Ground | | |
| C | 3.3V | Power of LINK IC | 200mA | 20mVp-p |
| D | F22 | 22KHz tone output | | |
| E | NC | Not connected | | |
| F | RESET | Reset (active LOW) | | |
| G | ERROUT | Frame error output (active HIGH) | | |
| H | FRAME_SYNC | Frame sync. (active HIGH) | | |
| I | DATA_VALID | Data valid (active HIGH) | | |
| J | DATA_CLK | Data clock (falling or rising edge triggering) | | |
| K~R | DATA0~7 | Byte data | | |
| S | SDA | I2C serial data | | |
| T | SCL | I2C serial clock | | |

* PIN 5,7 TOTAL CURRENT: 200mA(TYP.)

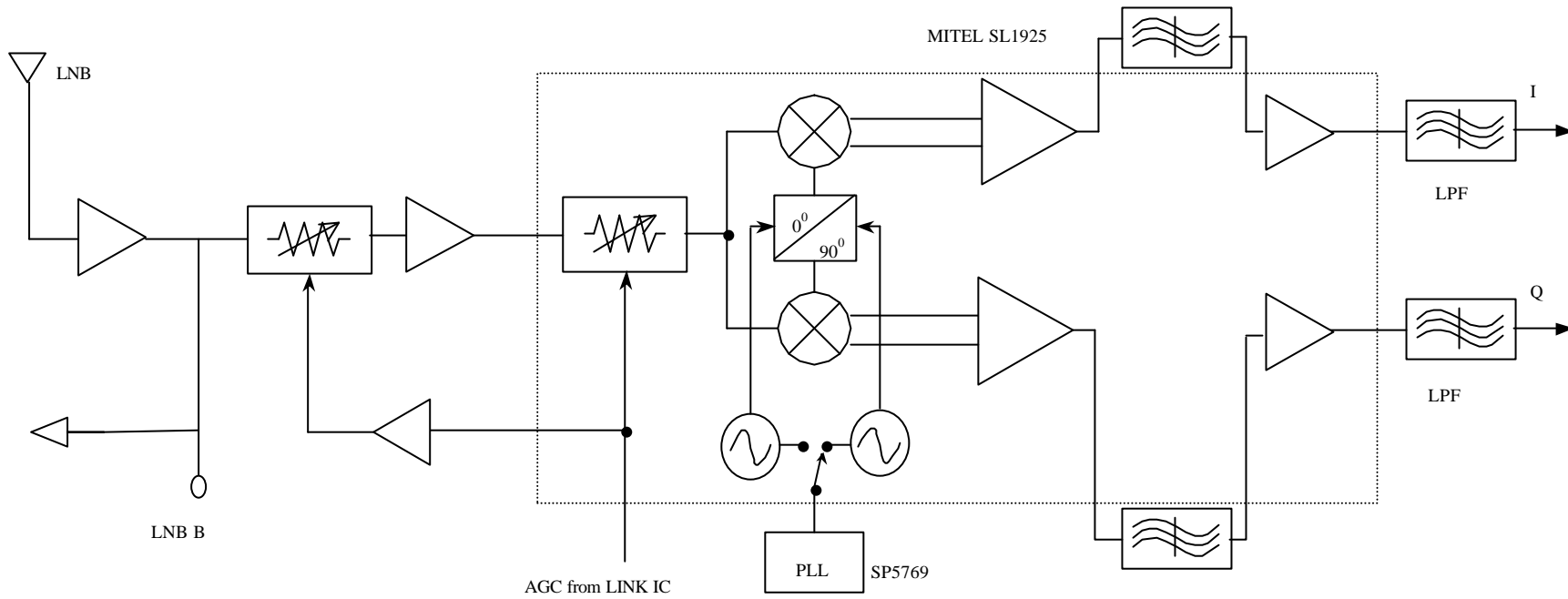


Fig. 1 RF Tuner Block Diagram(ZIF version)

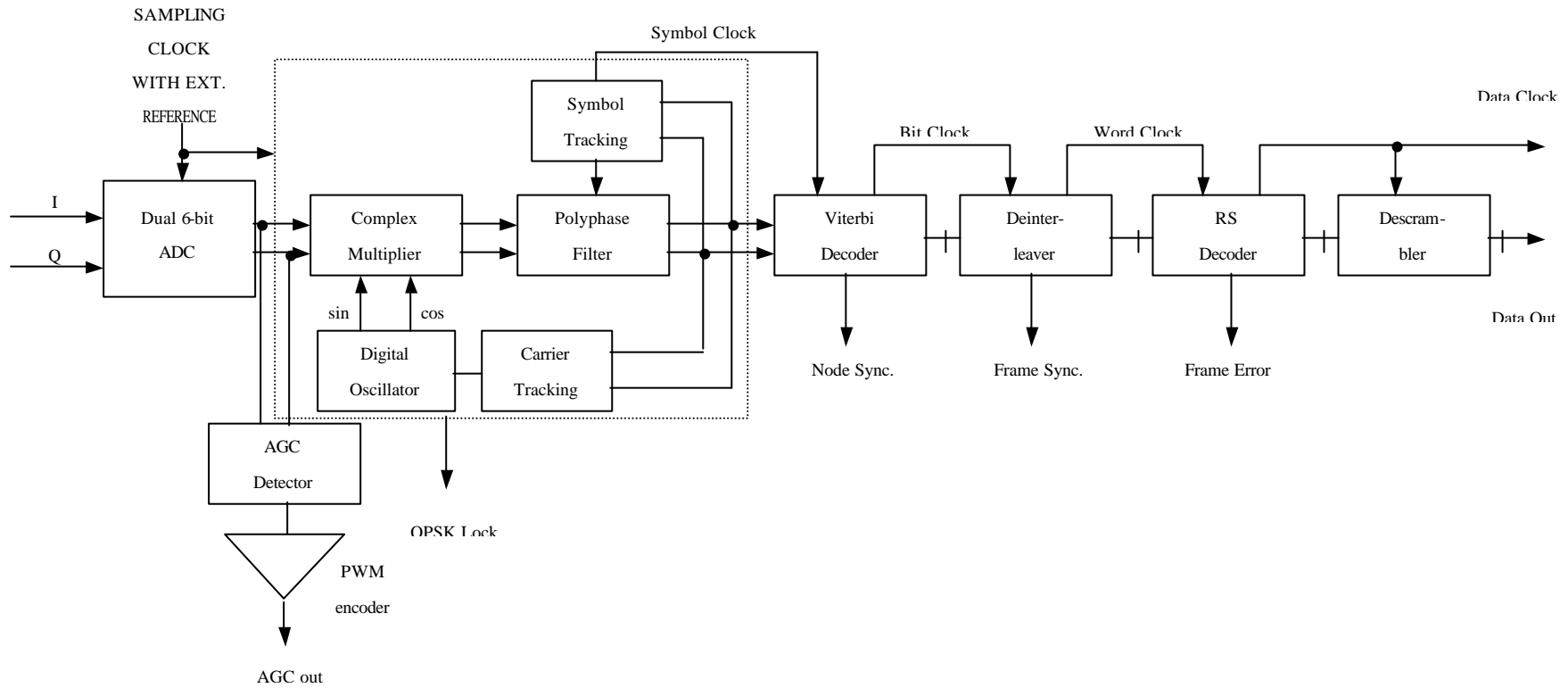


Fig. 2 LINK IC(HDM8513A) block diagram

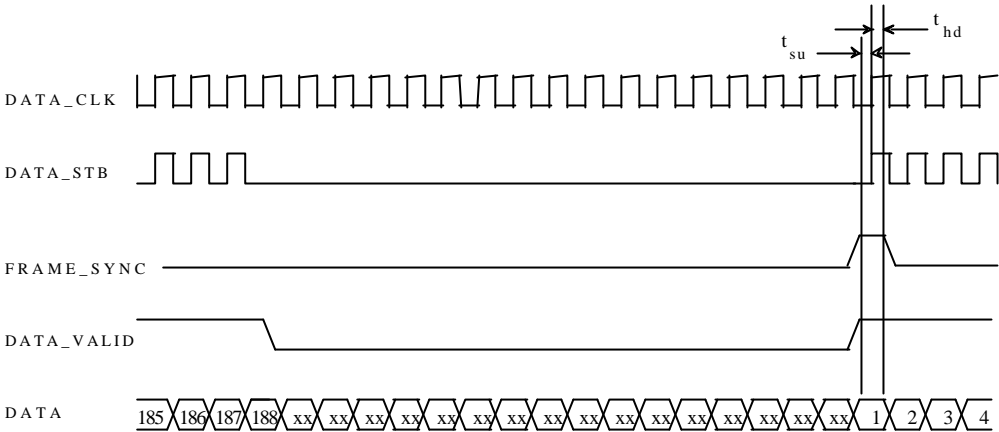


Fig. 3 Output Timing Diagram for DVB

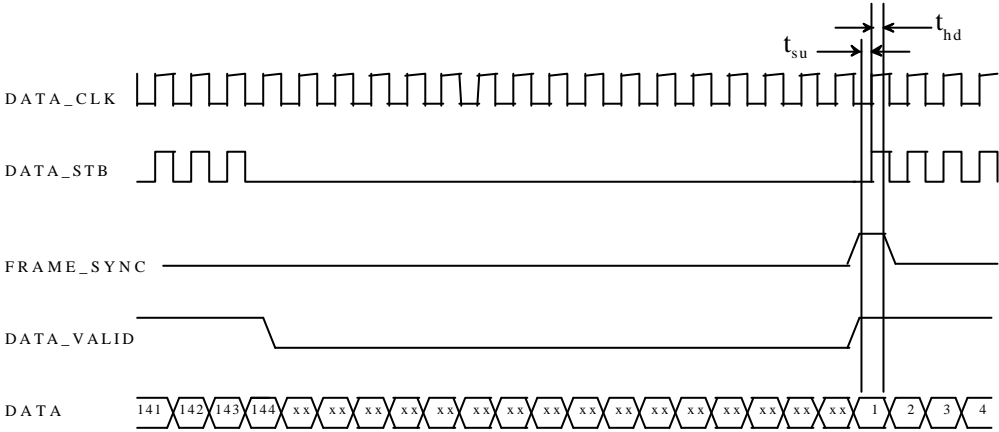


Fig. 4 Output Timing Diagram for DSS