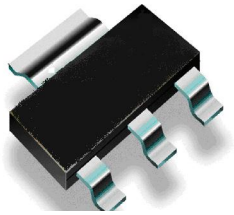
SSF1502G5

150V N-Channel MOSFET

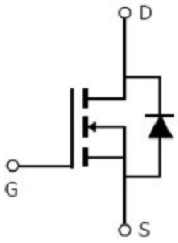
Main Product Characteristics

V_{DSS}	150V
R_{DS}(on)	0.14Ω(typ)
I_D	6A



SOT223

Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced trench MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175℃ operating temperature
- Lead free product

Description

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V	6 ①	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V	4.2 ①	
I_{DM}	Pulsed Drain Current ②	24	
P_D @TC = 25°C	Power Dissipation ③	12	W
	Linear Derating Factor	0.08	W/°C
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C

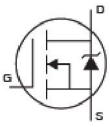
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	13	℃/W
$R_{\theta JA}$	Junction-to-Ambient (t ≤ 10s)④	—	62	℃/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	40	℃/W

Electrical Characteristics @T_A=25℃ unless otherwise specified

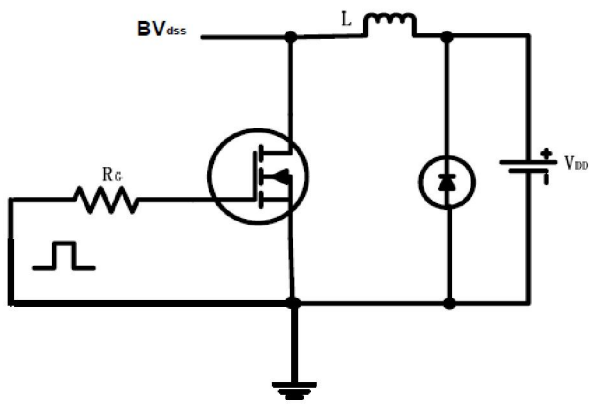
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	150	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.14	0.2	Ω	V_{GS}=10V,I_D = 2.8A
		—	0.32	—		T_J = 125°C
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
		—	2.63	—		T_J = 125°C
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	V_{DS} =120V, V_{GS} =0V
		—	—	50		T_J = 125°C
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS} =20V
	Gate-to-Source reverse leakage	-100	—	—		V_{GS} = -20V
Q_g	Total gate charge	—	30.9	—	nC	I_D = 2.8A
Q_{gs}	Gate-to-Source charge	—	6.5	—		V_{DD}=75V
Q_{gd}	Gate-to-Drain("Miller") charge	—	10.6	—		V_{GS} = 10V
$t_{d(on)}$	Turn-on delay time	—	11.8	—	nS	V_{GS}=10V, V_{DS} =75V,
t_r	Rise time	—	5.7	—		R_L=26Ω,
$t_{d(off)}$	Turn-Off delay time	—	29.3	—		R_{GEN}=6Ω
t_f	Fall time	—	6.0	—		I_D =2.8A
C_{iss}	Input capacitance	—	1230	—	pF	V_{GS} = 0V
C_{oss}	Output capacitance	—	47	—		V_{DS} = 75V
C_{rss}	Reverse transfer capacitance	—	31	—		f =1MHz

Source-Drain Ratings and Characteristics

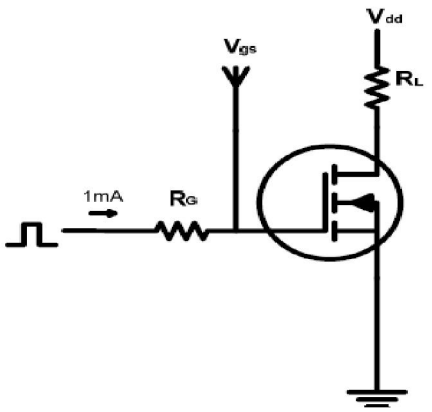
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	6	A	MOSFET symb showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	24	A	
V_{SD}	Diode Forward Voltage	—	0.81	1.5	V	I_S=2.8A, V_{GS}=0V,T_J= 25°C
t_{rr}	Reverse Recovery Time	—	54.8	—	nS	T_J = 25°C, I_F =2.8A, di/dt = 100A/μs
Q_{rr}	Reverse Recovery Charge	—	133.9	—	nC	

Test Circuits and Waveforms

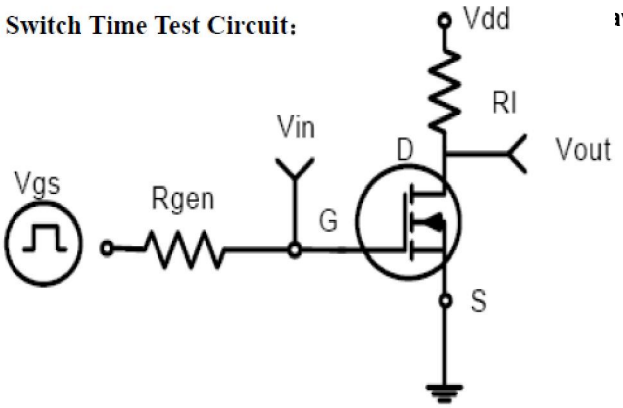
EAS test circuits:



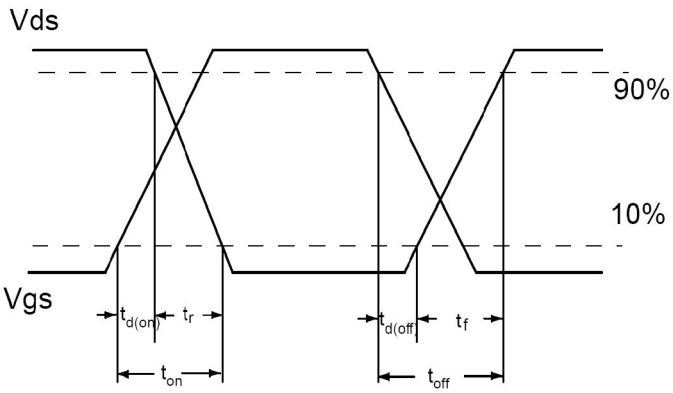
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Notes:

①Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

④The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C

⑤These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

Typical Electrical and Thermal Characteristics

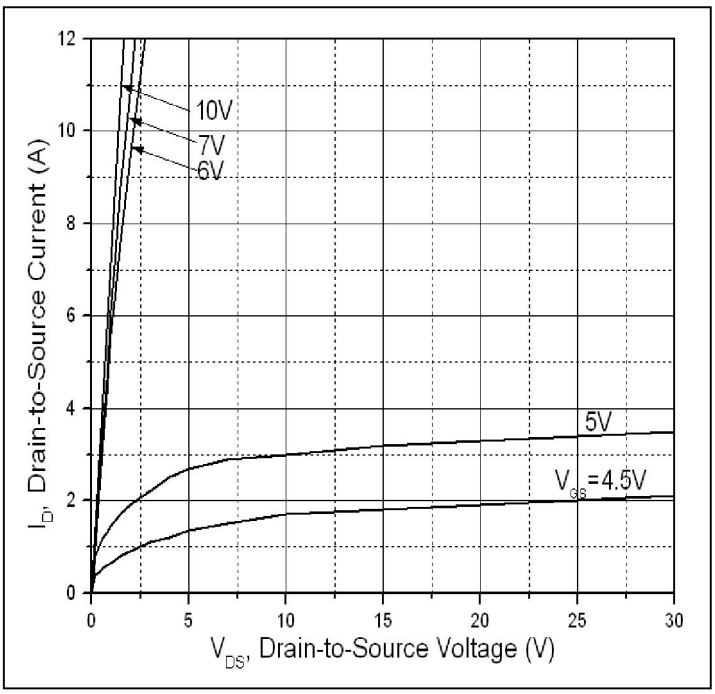


Figure 1: Typical Output Characteristics

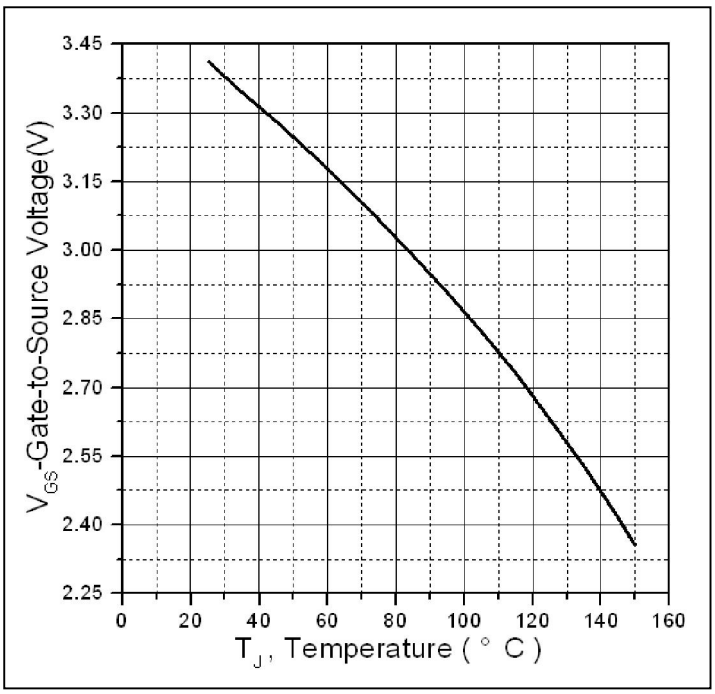


Figure 2. Gate to source cut-off voltage

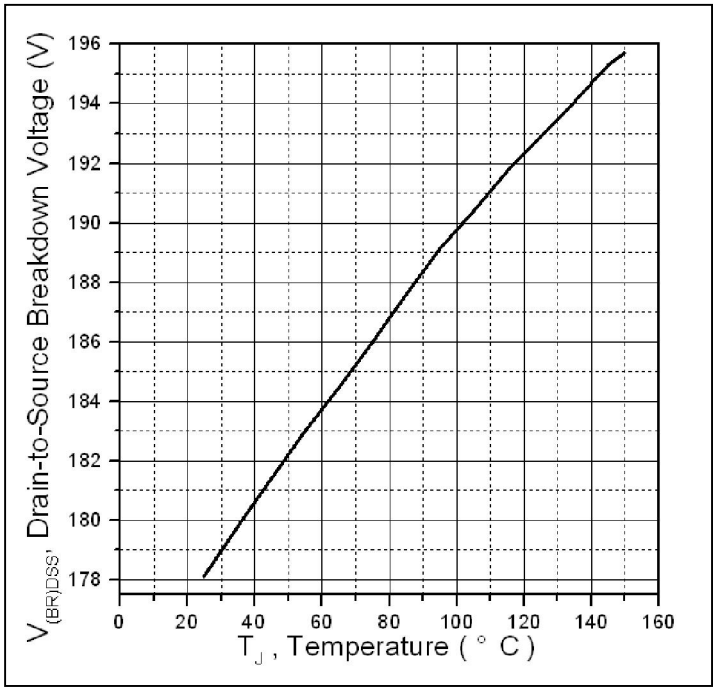


Figure 3. Drain-to-Source Breakdown Voltage vs. Temperature

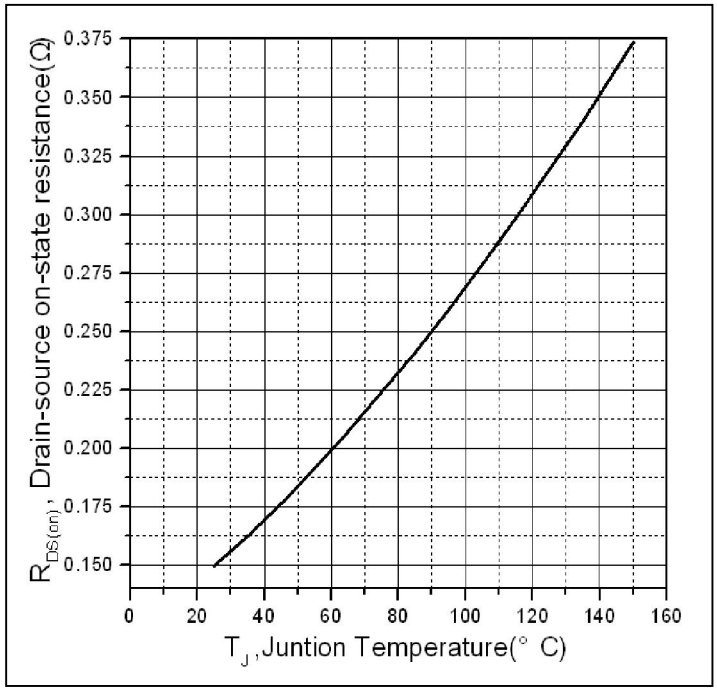


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical Electrical and Thermal Characteristics

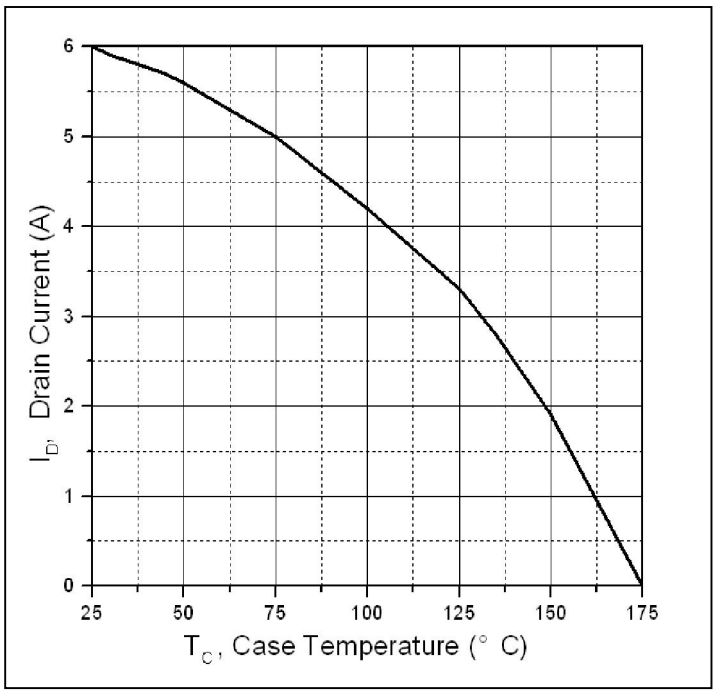


Figure 5. Maximum Drain Current Vs. Case Temperature

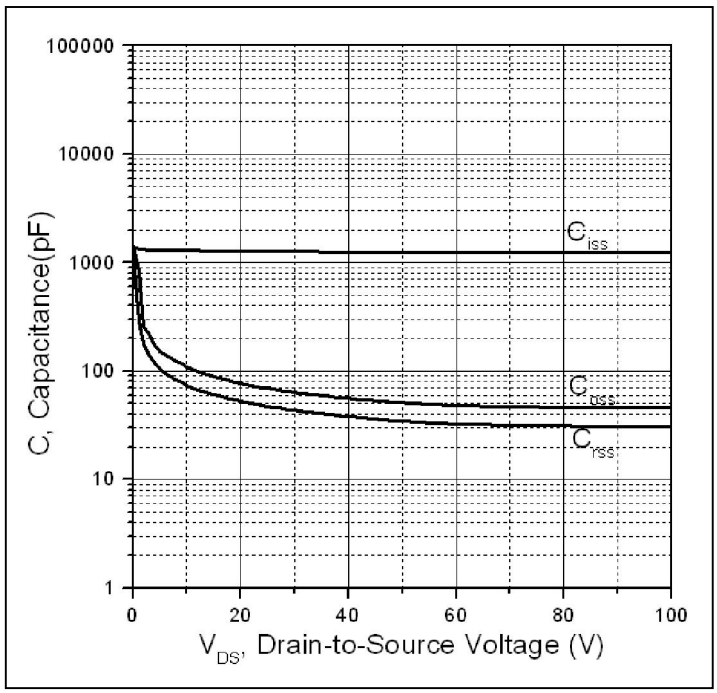


Figure 6.Typical Capacitance Vs. Drain-to-Source Voltage

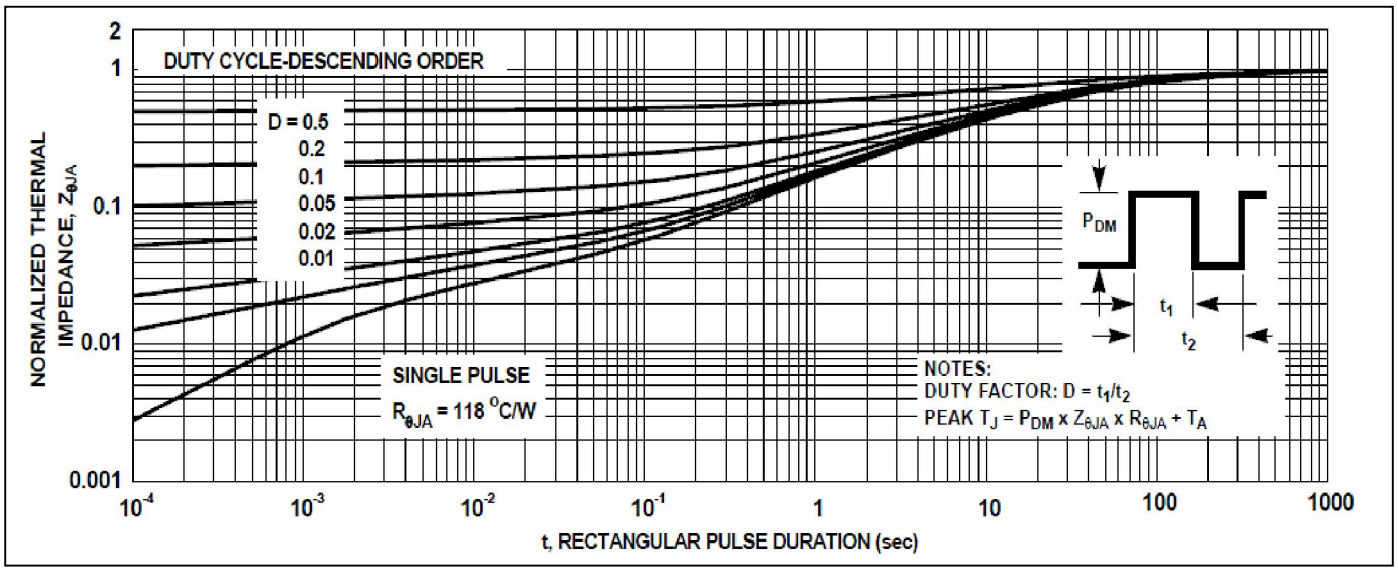
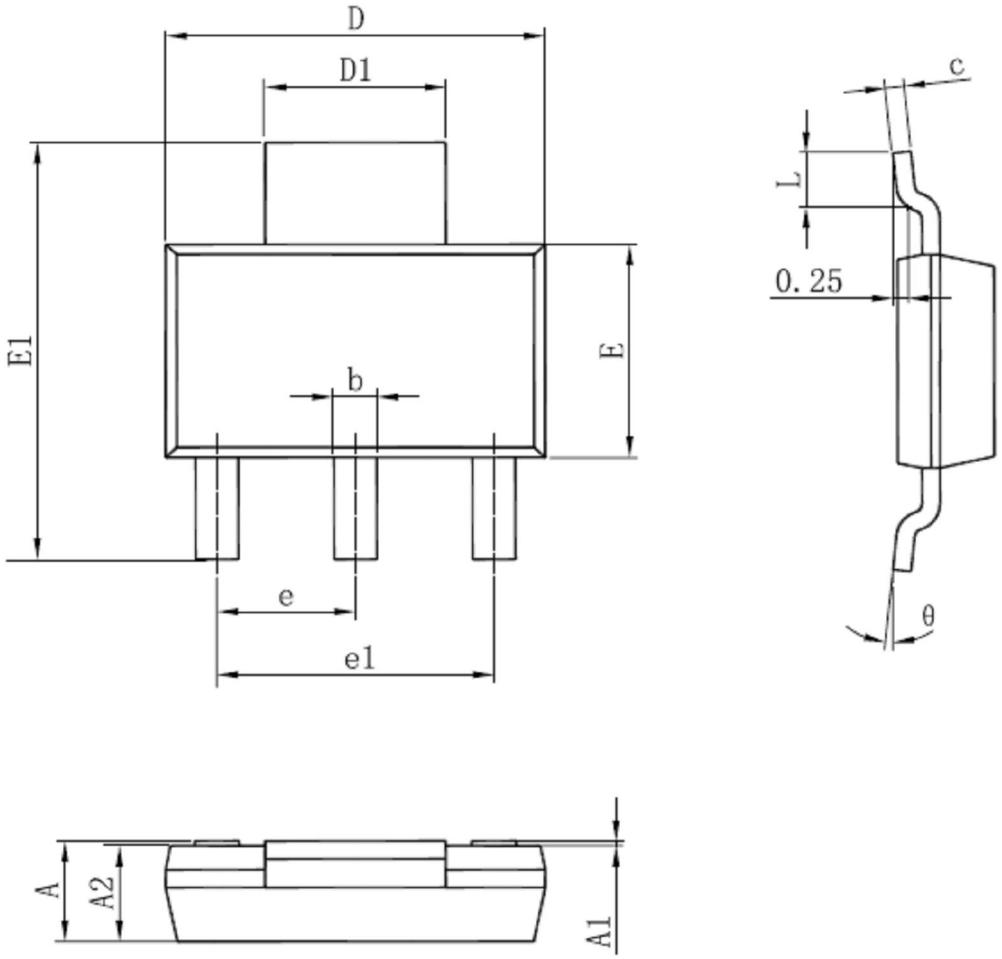


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data

SOT223 PACKAGE OUTLINE DIMENSION:



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.520	1.800	0.060	0.071
A1	0.000	0.100	0.000	0.004
A2	1.500	1.700	0.059	0.067
b	0.660	0.820	0.026	0.032
c	0.250	0.350	0.010	0.014
D	6.200	6.400	0.244	0.252
D1	2.900	3.100	0.114	0.122
E	3.300	3.700	0.130	0.146
E1	6.830	7.070	0.269	0.278
e	2.300(BSC)		0.091(BSC)	
e1	4.500	4.700	0.177	0.185
L	0.900	1.150	0.035	0.045
θ	0°	10°	0°	10°

Ordering and Marking Information

Device Marking: 1502G5

Package (Available)

SOT223

Operating Temperature Range

C : -55 to 175 ºC

Devices per Unit

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
SOT223	3000	10	30000	4	120000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ to 175℃ @ 80% of Max V_{DSS}/V_{CES}/VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=150℃ or 175℃ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices