IN1232

MICROMONITOR CHIP

DESCRIPTION

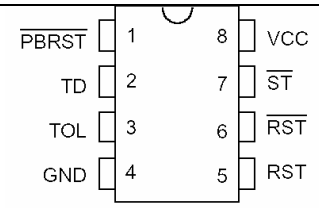
The IN1232 MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature–compensated reference and comparator cir-

cuit monitors the status of V_{CC}. When an out–of–tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in–tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

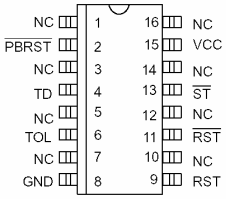
The second function the IN1232 performs is pushbutton reset control. The IN1232 debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The IN1232 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to time–out. The watchdog timer function can be set to operate on time–out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

FEATURES

- Halts and restarts an out–of–control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- Eliminates the need for discrete components



Dip-8



SO-14

PIN DESCRIPTION

PBRST	Pushbutton Reset Input
TD	Time Delay Set
TOL	Selects 5% or 10% V_{CC} Detect
GND	Ground
RST	Reset Output (Active High)
RST	Reset Output (Active Low, open drain)
ST	Strobe Input
V_{CC}	+5 Volt Power
NC	No Connections

INTEGRAL

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS *(0°C to 70°C)*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
ST and PBRST Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
ST and PBRST Input Low Level	V_{IL}	–0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	–1.0		+1.0	µA	3
Output Current @ 2.4V	I_{OH}	–8	–10		mA	5
Output Current @ 0.4V	I_{OL}	8	10		mA	
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1,7
Operating Current	I_{CC}		0.5	2.0	mA	2
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V + 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PBRST = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
ST Pulse Width	t_{ST}	20			ns	6, 8
V_{CC} Fail Detect to RST and RST	t_{RPD}		100	175	µs	
V_{CC} Slew Rate 4.75V to 4.25V	t_F	300			µs	
V_{CC} Detect to RST and RST Transition	t_{RPU}	250	610	1000	ms	4
V_{CC} Slew Rate 4.25V to 4.75V	t_R	0	5		µs	
PBRST Stable Low to RST and RST	t_{PDLY}			20	ms	

NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open.
3. PBRST is internally pulled up to V_{CC} with an internal impedance of 10K typical.
4. t_R = 5 µs.

5. RST is an open drain output.
6. Must not exceed t_{TD} minimum. See Table 1.
7. RST remains within 0.5V of V_{CC} on power–down until V_{CC} drops below 2.0V. RST remains within 0.5V of GND on power–down until V_{CC} drops below 2.0V.
8. Watchdog can not be disabled. It must be strobed to avoid resets.

OPERATION – POWER MONITOR

The IN1232 detects out–of–tolerance power supply conditions and warns a processor–based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL (Pin 3), the V_{CC} comparator outputs the signals RST (Pin 5) and RST (Pin 6). When TOL is connected to ground, the RST and RST signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC}, the RST and RST signals become active as V_{CC} falls below 4.5 volts. The RST and RST are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power–up, RST and RST are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

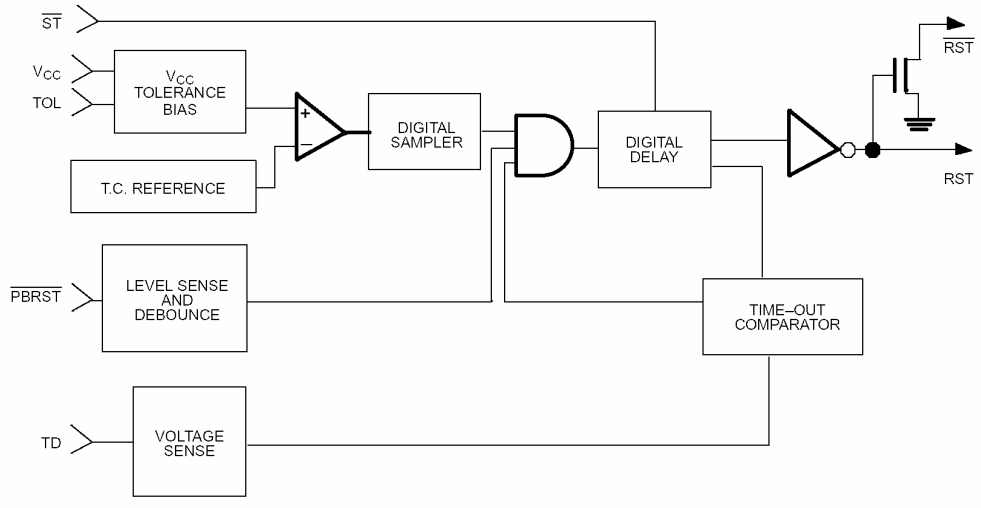
OPERATION – PUSHBUTTON RESET

The IN1232 provides an input pin for direct connection to a pushbutton (Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is de-bounced and timed such that RST and RST signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

OPERATION – WATCHDOG TIMER

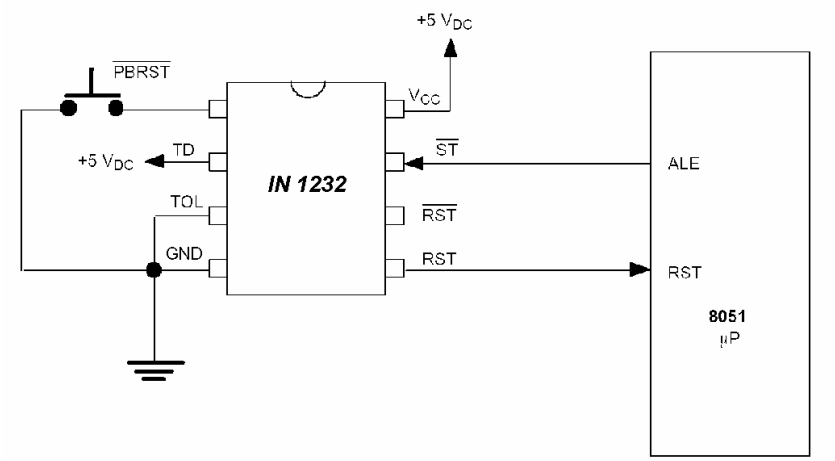
A watchdog timer function forces RST and RST signals to the active state when the ST input is not stimulated for a predetermined time period. The time period is set by the TD input to be typically 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and RST are inactive. If a high–to–low transition occurs on the ST input pin prior to time–out, the watchdog timer is reset and begins to time–out again. If the watchdog timer is allowed to time-out, then the RST and RST signals are driven to the active state for 250 ms minimum. The ST input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time–out. To guarantee that the watchdog timer does not time–out, a high–to–low transition must occur at or less than the minimum shown in Table 1. A typical circuit example is shown in Figure 3.

MICROMONITOR BLOCK DIAGRAM

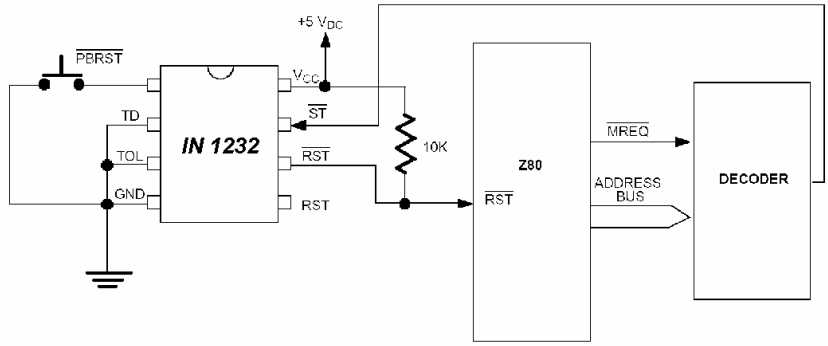


INTEGRAL

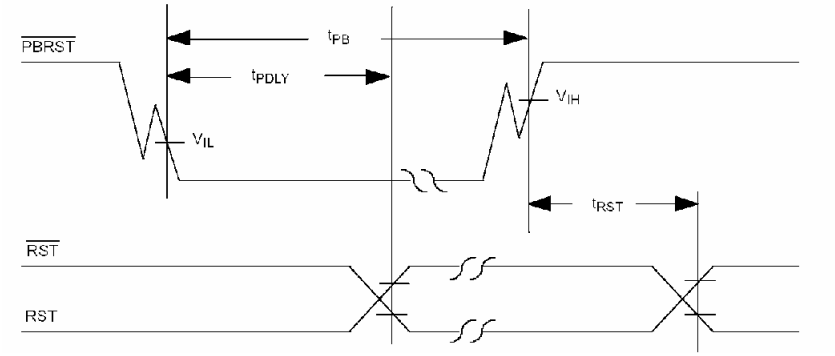
PUSHBUTTON RESET



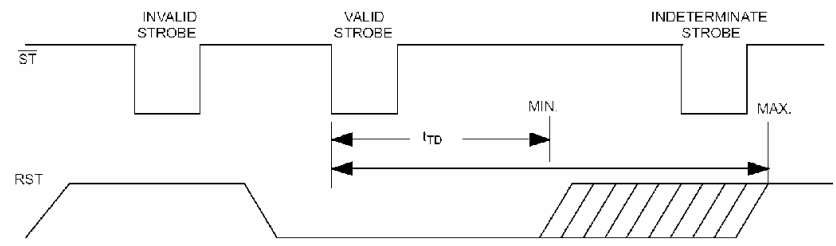
WATCHDOG TIMER



TIMING DIAGRAM: PUSHBUTTON RESET



TIMING DIAGRAM: STROBE INPUT

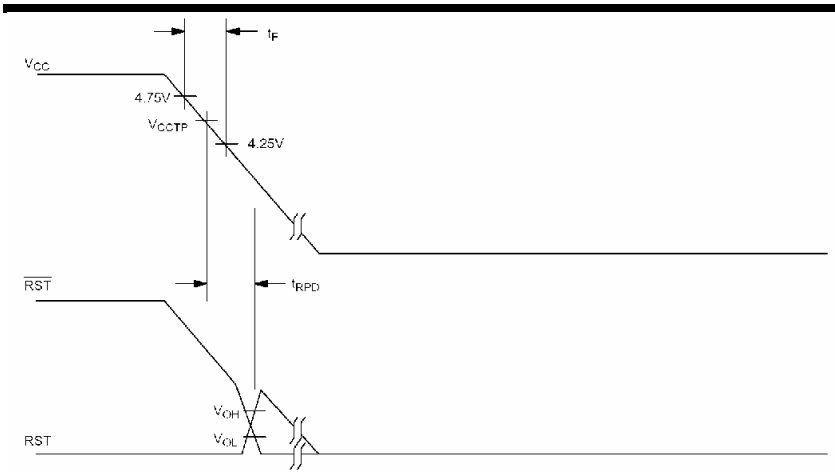


WATCHDOG TIMEOUTS

TD PIN	TIME–OUT		
	MIN	TYP	MAX
GND	62.5 ms	150 ms	250 ms
Float	250 ms	600 ms	1000 ms
V_{CC}	500 ms	1200 ms	2000 ms

TIMING DIAGRAM: POWER DOWN

INTEGRAL



TIMING DIAGRAM: POWER UP

