YAMAHA LSI

YMU762

MA-3
Mobile Audio 3

Outline

MA-3 is a synthesizer LSI for mobile phones that realize advanced game sounds.
This LSI has a built-in speaker amplifier, and thus, is an ideal device for outputting sounds that are used by mobile phones in addition to game sounds and ringing melodies that are replayed by a synthesizer.
The synthesizer section adopts “stereophonic hybrid synthesizer system” that are given advantages of both FM synthesizers and Wave Table synthesizers to allow simultaneous generation of up to thirty two FM voices and eight Wave Table voices.
Since FM synthesizer is able to present countless voices by specifying parameters with only several tens of bytes, memory capacity and communication band can be saved, and thus, the device exhibits the features in operating environment of mobile phones such as allowing distribution of arbitrary melodies with voices.
On the other hand, Wave Table synthesizer can pronounce the voice built in ROM and arbitrary ADPCM/PCM voices from sequencer by the download of the melody with voices etc..
MA-3 has a built-in hardware sequencer that helps to realize complex play without heavily loading the host CPU.
The device also has a built-in circuit for controlling vibrators and LEDs synchronizing with play of music.

Features

MA-3 has features as described below.

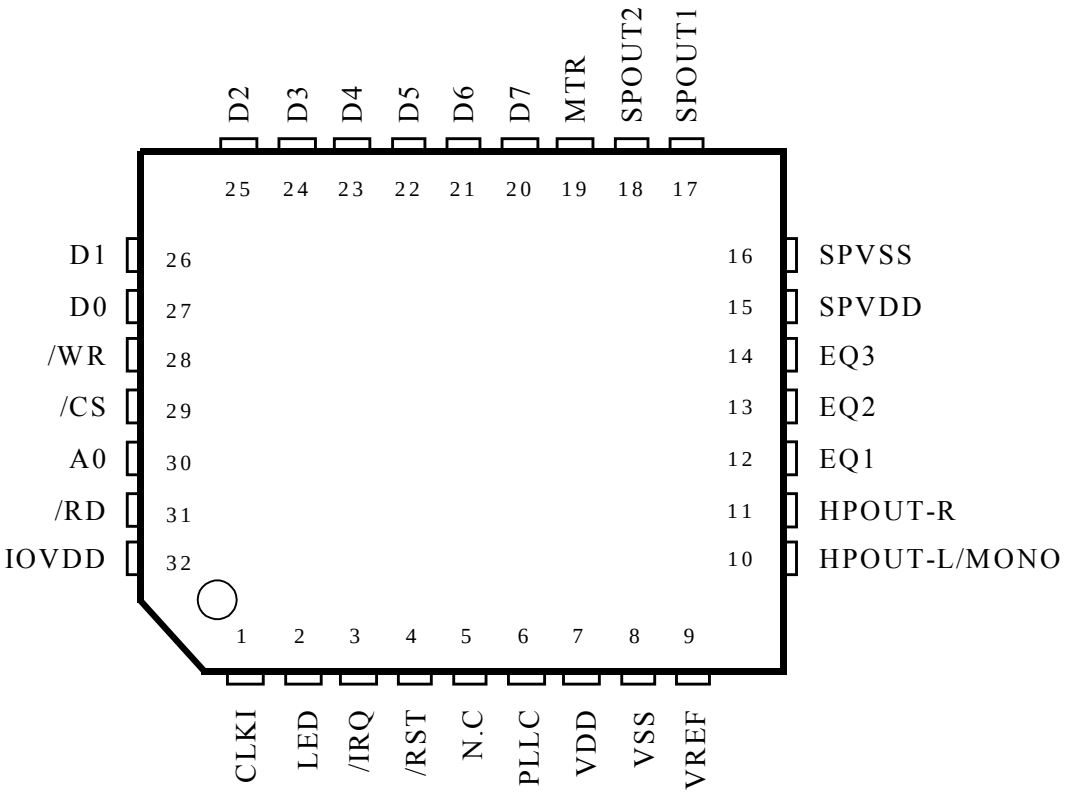
- Simultaneous generation of up to 40 tones: FM + Wave Table stereophonic hybrid synthesizer.
- Polyphonic synthesizer specification.
- Has built-in default voices for FM and Wave Table synthesizers in the ROM, and the voices can be downloaded to RAM.
- Fundamental waveforms for FM and algorithm are improved compared with YMU759 (MA-2), and voice parameters of detune etc. are added.
- Stream replay with ADPCM / PCM (shared use of Wave Table section).
- Software interrupt mechanism for external synchronization.
- Equipped with 8 bit parallel I/F for control from CPU.
- Equipped with speaker amplifier and equalizer circuit.
- Equipped with vibration control circuit, and LED lighting control circuit.
- Has built-in PLL to support inputting of master clock up to 20 MHz.
- Contains a 16-bit stereophonic D/A converter.
- Equipped with a stereophonic output terminal for headphone.
- Supports power down mode.
- Digital power supply: 2.7V to 3.3V (Typ 3.0V)
- Analog power supply: 2.7V to 4.5V (Typ 3.6V)
- 32-pin QFN plastic package

The contents of this booklet are target specifications and they are subject to change without a prior notice. Please check the finalized specifications before actually using this LSI.

YAMAHA CORPORATION

YMU762 CATALOG
CATALOG No.:LSI-4MU762A3
2002.9

Pin configuration



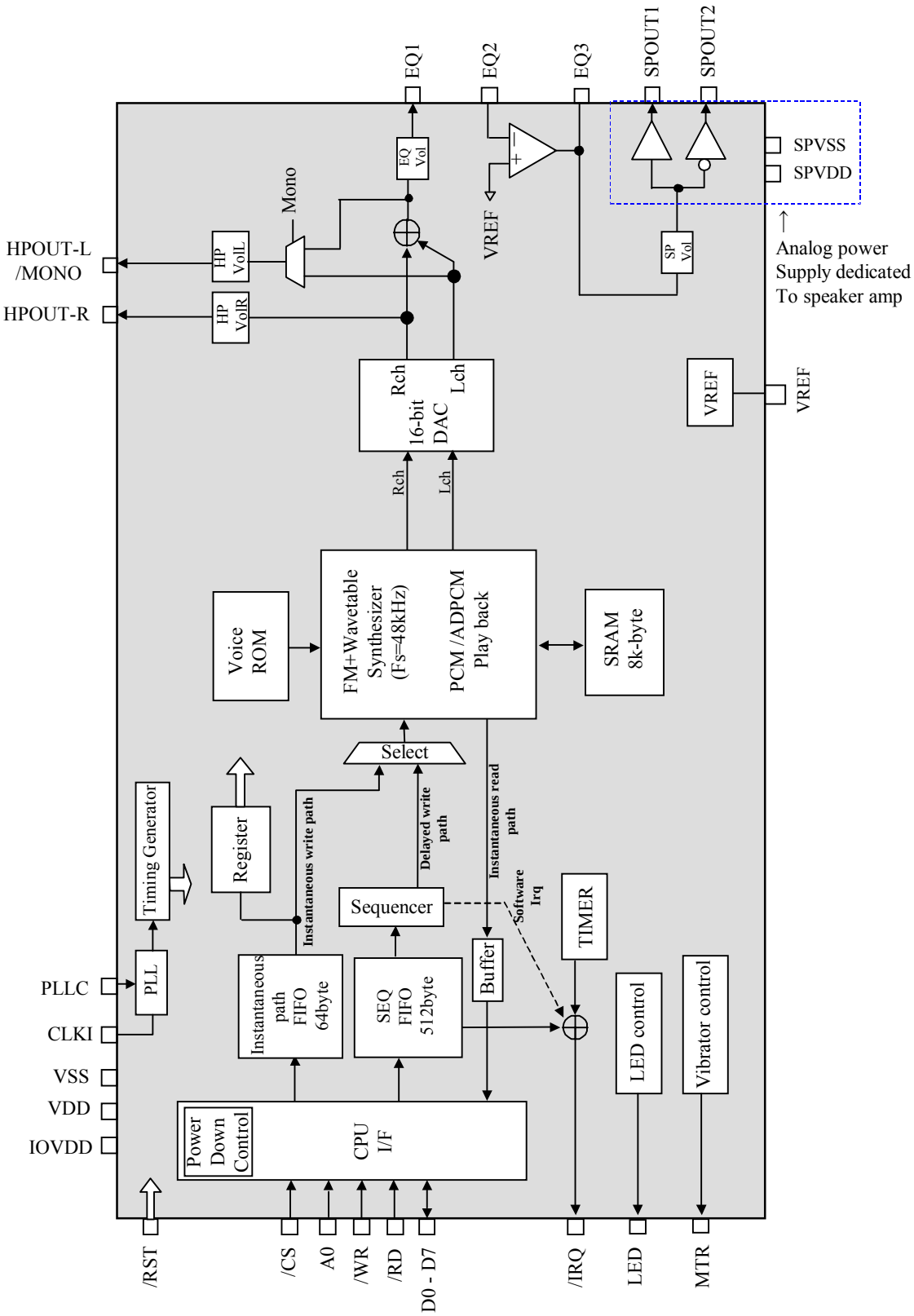
<32pin QFN Top View>

Functions of pins

No.	Pin name	I/O	Power supply	Function
1	CLKI	Ish	IOVDD	Clock input (2 MHz to 20 MHz)
2	LED	O	IOVDD	External LED control (Drive Capability = 4 mA)
3	/IRQ	O	IOVDD	Interrupt output (Drive Capability = 1 mA)
4	/RST	Ish	IOVDD	Hardware reset input
5	N.C	–	–	No Connection (during regular operations)
6	PLLC	A	VDD	Connection of capacitor for built-in PLL Connect a series connection of 1000 pF capacitor and 3.3 kΩ resistor between this pin and VSS(*). (*)Directly connect VSS used here and VSS of 8th pin.
7	VDD	–	–	Power supply (Typ +3.0V) Connect 0.1 µF and 4.7 µF capacitors between this pin and VSS.
8	VSS	–	–	Ground
9	VREF	A	VDD	Analog reference voltage Connect 0.1 µF capacitor between this pin and VSS.
10	HPOUT-L / MONO	A	VDD	Headphone output Lch (Can be used as MONO output)
11	HPOUT-R	A	VDD	Headphone output Rch
12	EQ1	A	VDD	Equalizer pin 1
13	EQ2	A	VDD	Equalizer pin 2
14	EQ3	A	VDD	Equalizer pin 3
15	SPVDD	–	–	Speaker amplifier analog power supply (Typ +3.6V) Connect 0.1 µF and 4.7 µF capacitors between this pin and SPVSS.
16	SPVSS	–	–	Speaker amplifier analog ground
17	SPOUT1	A	SPVDD	Speaker connection pin 1
18	SPOUT2	A	SPVDD	Speaker connection pin 2
19	MTR	O	IOVDD	External motor control pin (Drive Capability = 4 mA)
20	D7	I/O	IOVDD	CPU I/F data bus 7 (Drive Capability = 1 mA)
21	D6	I/O	IOVDD	CPU I/F data bus 6 (Drive Capability = 1 mA)
22	D5	I/O	IOVDD	CPU I/F data bus 5 (Drive Capability = 1 mA)
23	D4	I/O	IOVDD	CPU I/F data bus 4 (Drive Capability = 1 mA)
24	D3	I/O	IOVDD	CPU I/F data bus 3 (Drive Capability = 1 mA)
25	D2	I/O	IOVDD	CPU I/F data bus 2 (Drive Capability = 1 mA)
26	D1	I/O	IOVDD	CPU I/F data bus 1 (Drive Capability = 1 mA)
27	D0	I/O	IOVDD	CPU I/F data bus 0 (Drive Capability = 1 mA)
28	/WR	I	IOVDD	CPU I/F write enable
29	/CS	I	IOVDD	CPU I/F chip select
30	A0	I	IOVDD	CPU I/F address signal
31	/RD	I	IOVDD	CPU I/F read enable
32	IOVDD	–	–	Pin power supply (Typ +3.0V) Be sure to apply potential equivalent to 7th pin (directly connect on the board).

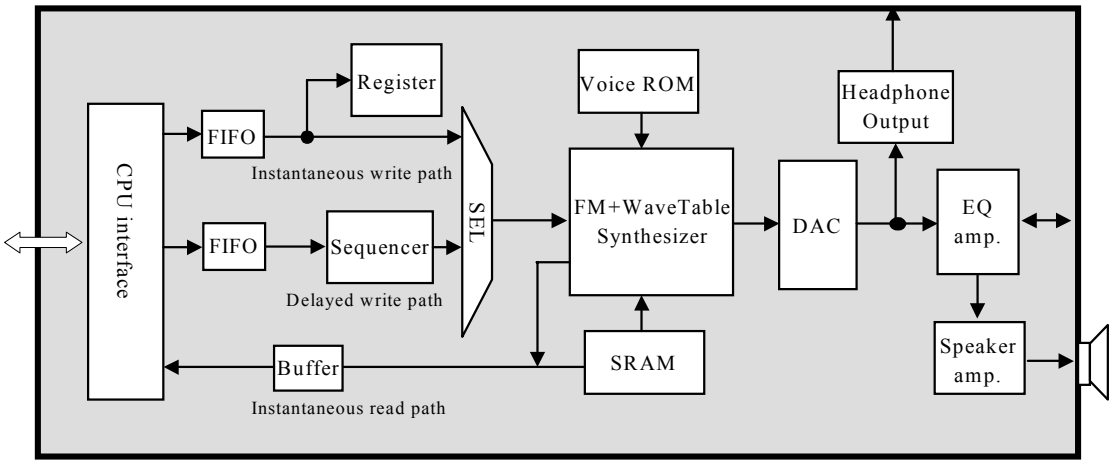
A : Analog pin Ish : Schmitt input

Block diagram



Outline of blocks

This section outlines functions of blocks contained in this device and flow of signals.



CPU interface

CPU interface is an 8-bit parallel type.

- ”Instantaneous write path” that enables Write command immediately (equipped with 64byte FIFO),
- ”Delayed write path” that enables Write command after elapse of specified time, and
- Instantaneous read path

are available.

Hardware sequencer and FIFO

The sequencer is a block that controls time and register access.

The structure of sequence data includes “time information data + MA-3 register control data”, for which 512 byte FIFO is provided. The sequence data is written into delayed write path.

FM+Wave Table synthesizer

This device contains a Polyphonic synthesizer that adopts FM +Wave Table stereophonic hybrid system that generates up to 40 tones.

The FM synthesizer has two operation modes; “16-Voice 4 operation mode” and “32-Voice 2 operation mode” which can be changed to each other freely (except during tone generation).

Since waveform for FM operation can be set arbitrarily, the device is able to create voices that are more complex than by conventional devices.

Wave Table synthesizers is able to generate eight voices simultaneously, and supports 8 bit PCM and 4 bit ADPCM data format. The sampling frequency is 48 kHz. Stream replaying is also available, realizing interchangeability with ADPCM replay capability of MA-2.

Voice ROM and SRAM

This device stores voice parameters (GM 128 voices + DRUM 40 voices) for FM and waveform data for Wave Table in the ROM. SRAM is used when downloading arbitrary FM voice parameter and waveform data for Wave Table. It is also used as waveform data buffer at stream replay with PCM/ADPCM.

DAC

Converts digital signal from a synthesizer into analog signal. The data length is 16 bit.

IRQ and TIMER

This device supports FIFO, two hardware TIMERs, and interrupt output with software interrupt.

Headphone output

This device supports stereophonic analog output for the headphone. Monaural output is available.

EQ amplifier

The filter response and gain of the amplifier can be changed by adjusting external parts such as resistors and/or capacitors.

Speaker amplifier

A speaker amplifier of which maximum out is 580 mW at SPVDD=3.6V is built in this device.
A control that adjusts the output level of the amplifier is provided in the previous stage of the amplifier.

LED and vibrator control block

LEDs and vibrator can be controlled synchronizing with a play. Control asynchronous with play is also possible.

Clock generating block

This devices supports clock input ranging from 2 MHz to 20 MHz. (Stop = 0 Hz is possible at power down.)
This block increases the frequency of inputted clock with various frequency by using PLL to create clocks with fixed frequency that are needed in the device.

Electrical Characteristics

Absolute maximum rating

Item	Symbol	Min.	Max.	Unit
SPVDD pin, power supply voltage (Speaker amplifier section)	SPVDD	-0.3	6.0	V
VDD pin, power supply voltage	VDD	-0.3	4.2	V
IOVDD pin, power supply voltage	IOVDD	-0.3	4.2	V
SPOUT1, SPOUT2 pin, applied voltage	V_{INSP}	-0.3	SPVDD+0.3	V
Analog input voltage	V_{INA}	-0.3	VDD+0.3	V
Digital input voltage	V_{IND}	-0.3	IOVDD+0.3	V
Permissible loss (*)	Pd		1197	mW
Storage temperature	T_{STG}	-50	125	°C

Note: VSS = SPVSS = 0V

(*) : Top= 25 °C, and glass epoxy PCB (30mm × 100mm × 1.0mm) is installed.

Operation with Top= 25 °C or higher degrees the permissible loss at the rate of 12mW per 1 °C.

Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
SPVDD operating voltage (Speaker amplifier section)	SPVDD	2.7	3.6	4.5	V
VDD operating voltage	VDD	2.7	3.0	3.3	V
IOVDD operating voltage	IOVDD	2.7	3.0	3.3	V
Operating ambient temperature	T_{OP}	-20	25	85	°C

Note: VSS = SPVSS = 0V

Make VDD and IOVDD into same electric potential (Connect them directly on the circuit board).

DC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage “H” level	V_{IH}		0.7 × IOVDD			V
Input voltage “L” level	V_{IL}				0.2 × IOVDD	V
Output voltage “H” level	V_{OH}	I_{OH} = (*)	0.8 × IOVDD			V
Output voltage “L” level	V_{OL}	I_{OL} = (*)			0.4	V
Schmitt width	Vsh			0.5		V
Input leakage current	IL		-10		10	µA
Input capacity	CI				10	pF

Note: T_{OP}=-20 to 85°C, VDD, IOVDD=3.0±0.3V, Capacitor load=50 pF

(*) : /IRQ, D0 ~ D7 are I_{OH}= –1 mA, I_{OL}= +1 mA

LED, MTR are I_{OH} = –4 mA, I_{OL}= +4 mA

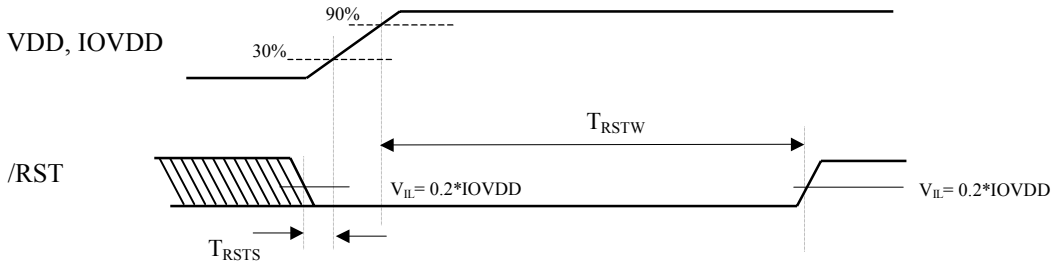
AC characteristics

/RST, CLKI

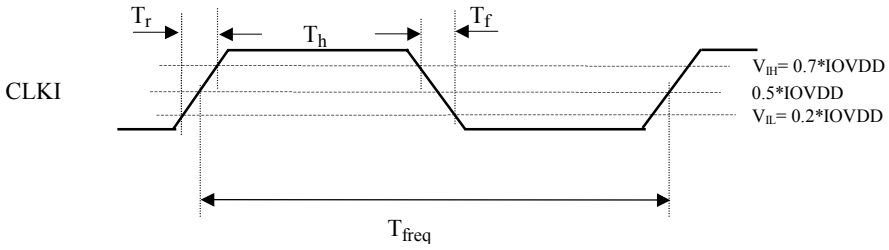
Item	Symbol	Min.	Typ.	Max.	Unit
/RST "L" pulse width	T_{RSTW}	100			µs
/RST (indefinite → L) setup time	T_{RSTS}	0			µs
CLKI frequency	1 / Tfreq	0		20	MHz
CLKI rise / fall time	Tr / Tf			30	ns
CLKI duty factor	Th / Tfreq	30	50	70	%

Note: T_{OP}=-20 to 85°C, VDD, IOVDD=3.0±0.3V, Capacitor load=50 pF

The input to Clock can be stopped (=0Hz) during reset period and power down state (DP0=1).
However, the input level is to be H or L, and input of intermediate level is prohibited.



The reset width is defined as the time from the moment VDD or IOVDD has risen to 90%.
/RST has to be settled at "L" level at the time VDD or IOVDD has risen to 30%.



Measurement point
V_{IH} = 0.7*IOVDD
V_{IL} = 0.2*IOVDD
V_{OH} = 0.8*IOVDD
V_{OL} = 0.2*IOVDD

CPU interface

(Write cycle)

Item	Symbol	Min	Max.	Unit
Address setup time	T_{ADS}	50		ns
Address hold time	T_{ADH}	0		ns
Chip select setup time	T_{CSS}	50		ns
Chip select hold time	T_{CSH}	0		ns
Write pulse width	T_{WW}	50		ns
Data setup time	T_{WDS}	30		ns
Data hold time	T_{WDH}	0		ns

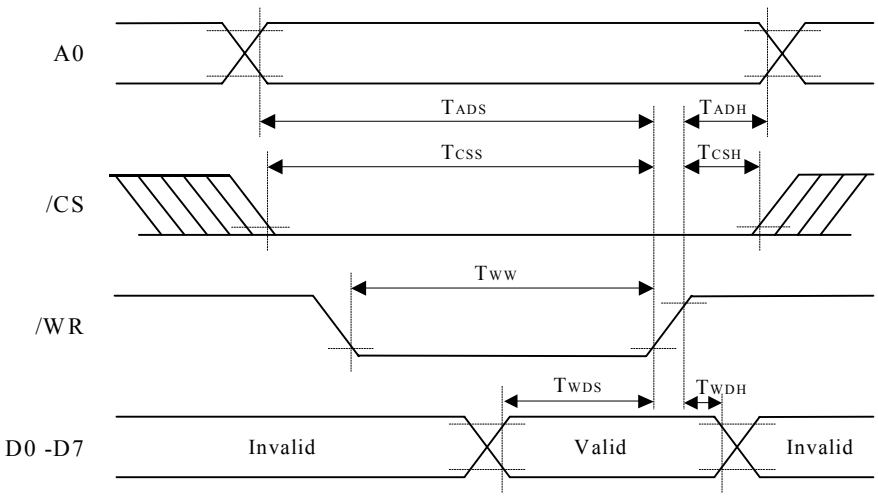
T_{OP}=-20 to 85°C, VDD,IOVDD=3.0±0.3V, Capacitor load=50 pF

(Read cycle)

Item	Symbol	Min	Max.	Unit
Address setup time	T_{ADS}	80		ns
Address hold time	T_{ADH}	0		ns
Chip select setup time	T_{CSS}	80		ns
Chip select hold time	T_{CSH}	0		ns
Read pulse width	T_{RW}	80		ns
Read data access time	T_{ACC}		70	ns
Data hold time	T_{RDH}	0	30	ns

T_{OP}=-20 to 85°C, VDD,IOVDD=3.0±0.3V, Capacitor load=50 pF

Write cycle

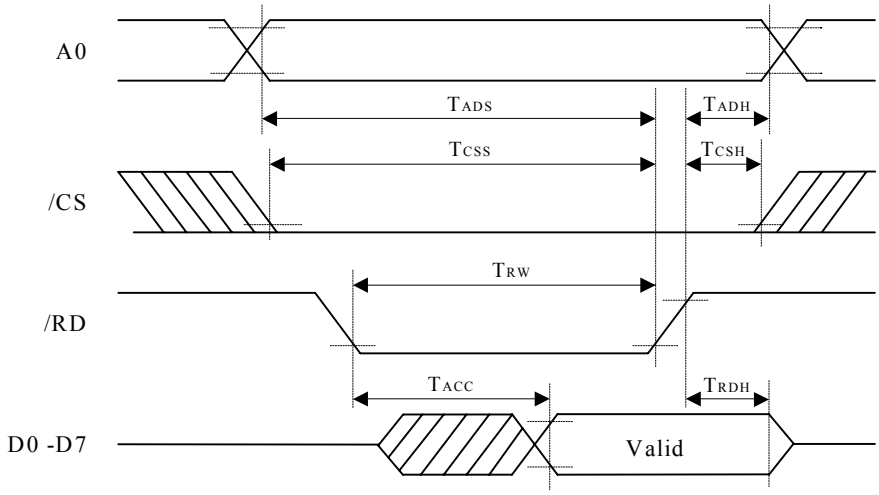


Note : Under the conditions of $T_{CSH} \geq 0$ns,

T_{ADH}, T_{WDH} : Defined with respect to the point where the rise of /WR has reached 0.7*IOVDD.

T_{ADS}, T_{WDS} : Defined with respect to the point where the rise of /WR has reached 0.2*IOVDD.

Read cycle



Note : Under the conditions of $T_{CSH} \geq 0$ns,

T_{ADH}, T_{RDH} : Defined with respect to the point where the rise of /RD has reached 0.7*IOVDD.

T_{ADS}, T_{CSS} : Defined with respect to the point where the rise of /RD has reached 0.2*IOVDD.

T_{ACC} : Defined with respect to the point where any of /CS , /RD and A0 has changed later.

T_{RDH} : Time to the point where D0-D7 pins become high impedance.

Power consumption

Item	Min.	Typical	Max.	Unit
Load current of VDD+ IOVDD (at regular operation)		25		mA
At SPVDD side no tone		4		mA
At SPVDD side 8ohm load 400mW output		210		mA
Power down mode (VDD + IOVDD+SPVDD) (*)		1	10	µA

Note: T_{OP}=-20 to 85°C, VDD, IOVDD=3.0±0.3V, SPVDD=3.6V

(*) : Measurement condition : /CS input pin is fixed to V_{IH}=VDD.

Analog characteristics

Conditions of T_{OP}=25°C, VDD, IOVDD=3.0V and SPVDD=3.6V apply to all items.

SP amplifier

Item	Min.	Typical	Max.	Unit
Gain setting (fixed)		±2		times
Min. load resistance (RL)		8		Ω
Max. output voltage amplitude (RL=8Ω)		6.0		Vp-p
Max. output power (RL=8Ω, THD+N≤1.0%)		580		mW
THD + N (RL=8Ω, f=1 kHz, output = 400mW)		0.025		%
Noise at no signal (A-filter: weighting filter)		-90		dBV
PSRR (f=1 kHz)		90		dB
Amplitude center potential (VSEL2, VSEL1 =0, 0)		0.6×VDD		V
(VSEL2, VSEL1 =0, 1)		0.5×VDD		V
(VSEL2, VSEL1 =1, 0)		0.67×VDD		V
Differential Output Voltage		10	50	mV

EQ amplifier

Item	Min.	Typical	Max.	Unit
Gain settable range			30	dB
Max. output voltage amplitude		2.7		Vp-p
THD + N (f=1 kHz)			0.05	%
Noise at no signal (A-filter)		-90		dBV
Input impedance	10			MΩ
Feedback resistance between EQ2 and EQ3	20			kΩ

SP Volume

Item	Min.	Typical	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
THD + N (f=1 kHz)			0.05	%

EQ Volume

Item	Min.	Typical	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise at no signal (A-filter)		-90		dBV
Max. output current	120			μA
Max. output voltage amplitude		1.5		Vp-p
Output impedance		300	600	Ω

HP Volume

Item	Min.	Typical	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise at no signal (A-filter)		-90		dBV
Max. output current	120			μA
Max. output volt. amplitude		1.5		Vp-p
Output impedance		300	600	Ω

VREF

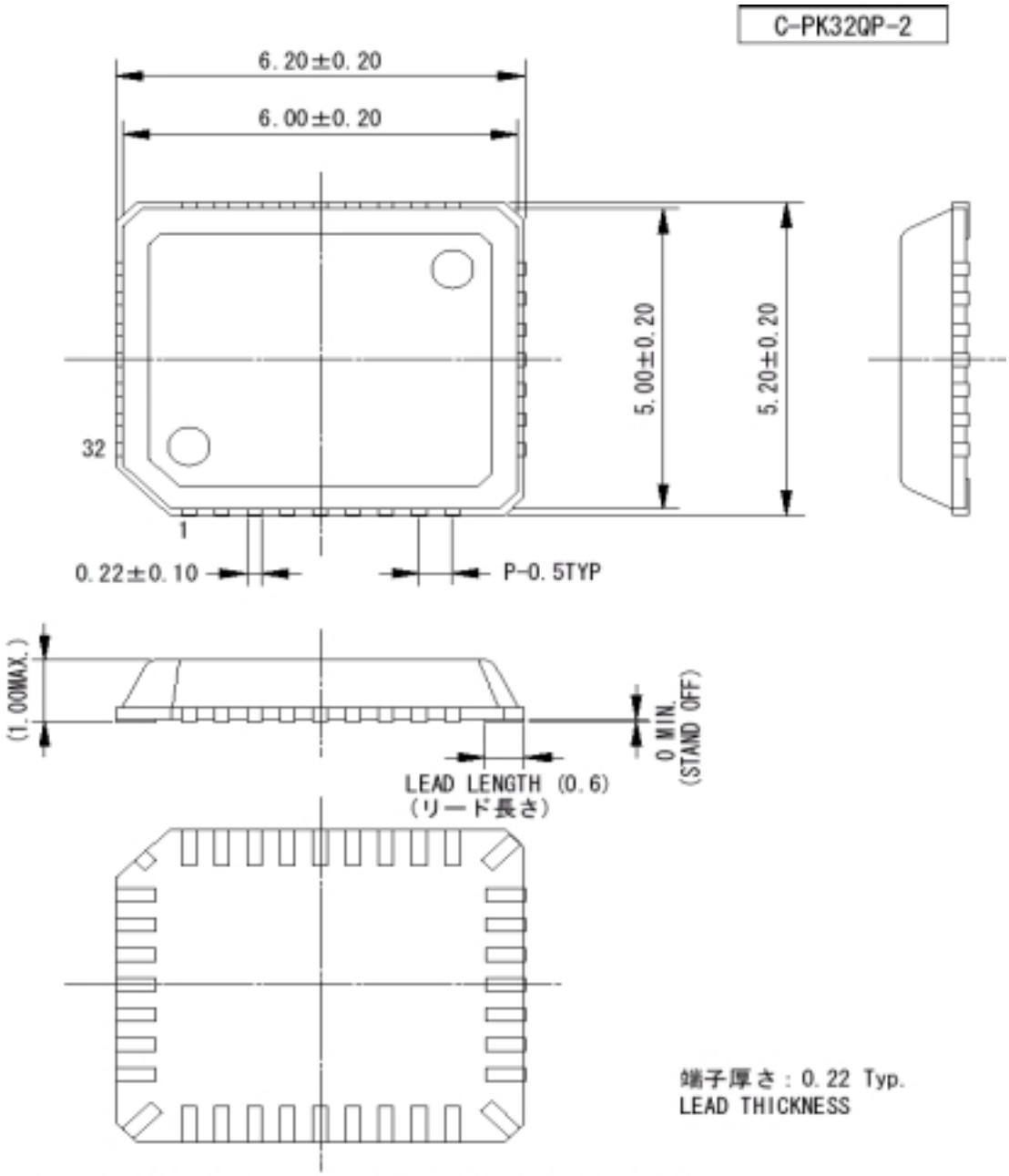
Item	Min.	Typical	Max.	Unit
VREF voltage		0.5×VDD		V

DAC

Item	Min.	Typical	Max.	Unit
Resolution		16		Bit
Full scale output volt.		1.5		Vp-p
THD+N (f= 1 kHz)			0.5	%
Noise at no signal (A-filter)		-85	-80	dBV
Frequency response (f=50Hz to 20 kHz)	-3.0 (*)		+0.5	dB

(*): Reduction of response in high frequency range caused by aperture effect

External dimensions of package



モールドコーナー形状は、この図面と若干異なるタイプのものもあります。
カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.
The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

注) 表面実装LSIは保管条件及び、半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせ下さい。
Note: The LSIs for surface mount need special consideration on storage and soldering conditions.
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