

**256K (32K x 8) Static RAM**

**Features**

- **Temperature Ranges**
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
  - Automotive-A: -40°C to 85°C
  - Automotive-E: -40°C to 125°C
- **Speed: 70 ns**
- **Low voltage range: 2.7V–3.6V**
- **Low active power and standby power**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in standard Pb-free and non Pb-free 28-lead (300-mil) narrow SOIC, 28-lead TSOP-I and 28-lead Reverse TSOP-I packages**

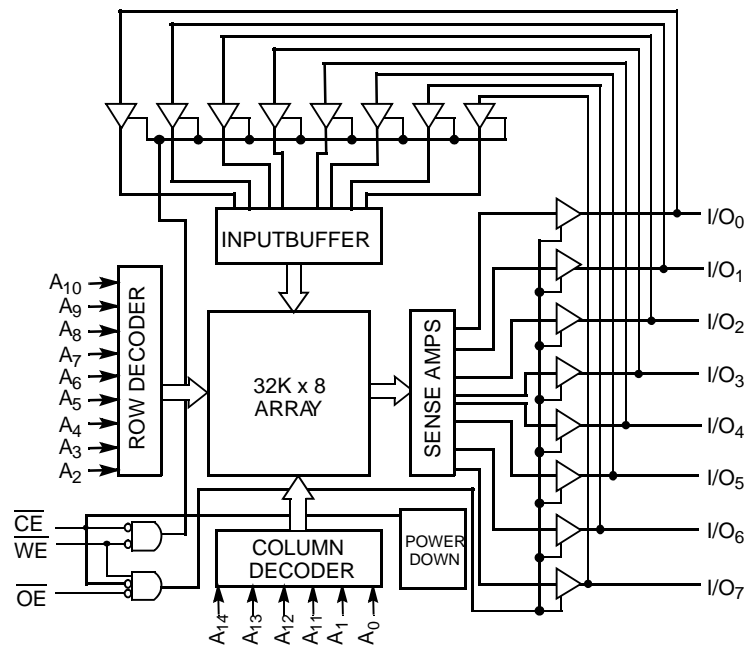
**Functional Description<sup>[1]</sup>**

The CY62256VN family is composed of two high-performance CMOS static RAM's organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and active LOW output enable ( $\overline{OE}$ ) and tri-state drivers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{14}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.

**Logic Block Diagram**

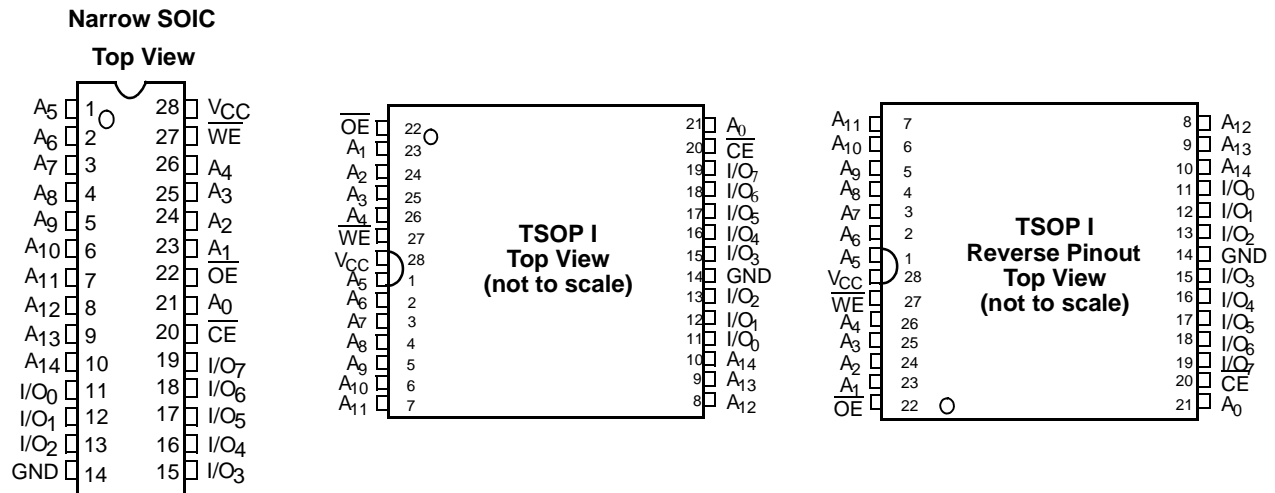


**Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Product Portfolio**

Product	Range	V <sub>CC</sub> Range (V)			Power Dissipation			
					Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (μA)	
		Min.	Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.
CY62256VNLL	Com'l	2.7	3.0	3.6	11	30	0.1	5
CY62256VNLL	Ind'l	2.7	3.0	3.6	11	30	0.1	10
CY62256VNLL	Automotive-A	2.7	3.0	3.6	11	30	0.1	10
CY62256VNLL	Automotive-E	2.7	3.0	3.6	11	30	0.1	130

**Pin Configurations**

**Pin Definitions**

Pin Number	Type	Description
1–10, 21, 23–26	Input	<b>A<sub>0</sub>–A<sub>14</sub></b> . Address Inputs
11–13, 15–19	Input/Output	<b>I/O<sub>0</sub>–I/O<sub>7</sub></b> . Data lines. Used as input or output lines depending on operation
27	Input/Control	<b>WE</b> . When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
20	Input/Control	<b>CE</b> . When LOW, selects the chip. When HIGH, deselects the chip
22	Input/Control	<b>OE</b> . Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
14	Ground	<b>GND</b> . Ground for the device
28	Power Supply	<b>V<sub>CC</sub></b> . Power supply for the device

**Note:**

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> Typ., T<sub>A</sub> = 25°C, and t<sub>AA</sub> = 70 ns.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to + 150°C  
 Ambient Temperature with Power Applied..... -55°C to + 125°C  
 Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... -0.5V to + 4.6V  
 DC Voltage Applied to Outputs in High-Z State<sup>[3]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 DC Input Voltage<sup>[3]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

**Operating Range**

Device	Range	Ambient Temperature (T <sub>A</sub> ) <sup>[4]</sup>	V <sub>CC</sub>
CY62256VN	Commercial	0°C to +70°C	2.7V to 3.6V
	Industrial	-40°C to +85°C	
	Automotive-A	-40°C to +85°C	
	Automotive-E	-40°C to +125°C	

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	-70			Unit	
			Min.	Typ. <sup>[2]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.7V		2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.7V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> + 0.3V		V
V <sub>IL</sub>	Input Leakage Voltage		-0.5		0.8		V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	Com'l/Ind'l/Auto-A	-1	+1		μA
			Auto-E	-10	+10		μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , Output Disabled	Com'l/Ind'l/Auto-A	-1	+1		μA
			Auto-E	-10	+10		μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = 3.6V, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	All Ranges		11	30	mA
I <sub>SB1</sub>	Automatic CE Power down Current - TTL Inputs	V <sub>CC</sub> = 3.6V, $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	All Ranges		100	300	μA
I <sub>SB2</sub>	Automatic CE Power-down Current - CMOS Inputs	V <sub>CC</sub> = 3.6V, $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l	0.1	5		μA
			Ind'l/Auto-A		10		
			Auto-E		130		

**Notes:**

3. V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.

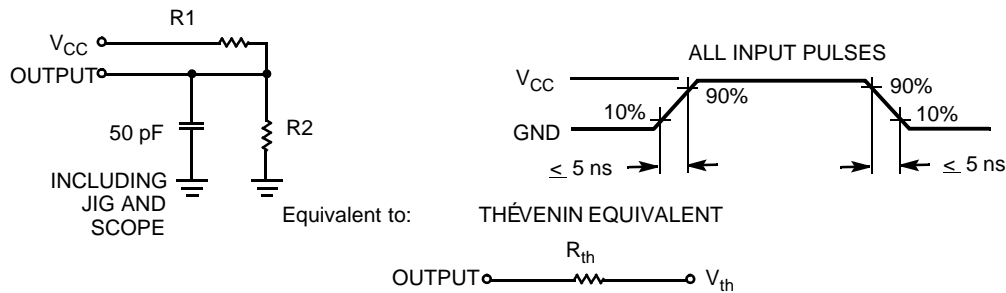
4. T<sub>A</sub> is the "Instant-On" case temperature

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.0V	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Thermal Resistance<sup>[5]</sup>**

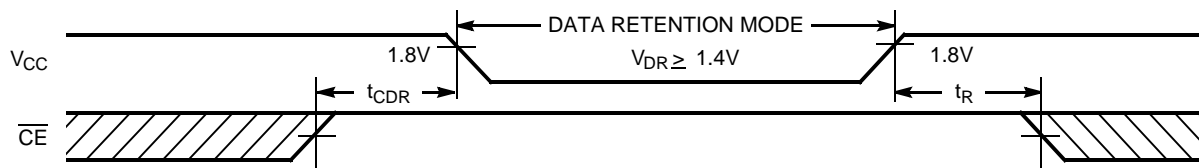
Parameter	Description	Test Conditions	SOIC	TSOPI	RTSOPI	Unit
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	68.45	87.62	87.62	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		26.94	23.73	23.73	°C/W

**AC Test Loads and Waveforms**


Parameter	Value	Units
R1	1100	Ohms
R2	1500	Ohms
R <sub>TH</sub>	645	Ohms
V <sub>TH</sub>	1.750	Volts

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions <sup>[6]</sup>	Min.	Typ. <sup>[2]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.4			V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.4V, CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V	Com'l	0.1	3	μA
			Ind'l/Auto-A		6	
			Auto-E		50	
t <sub>CDR</sub> <sup>[6]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[5]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Data Retention Waveform**

**Note:**

5. Tested initially and after any design or process changes that may affect these parameters.
6. No input may exceed V<sub>CC</sub> + 0.3V.

**Switching Characteristics** Over the Operating Range<sup>[7]</sup>

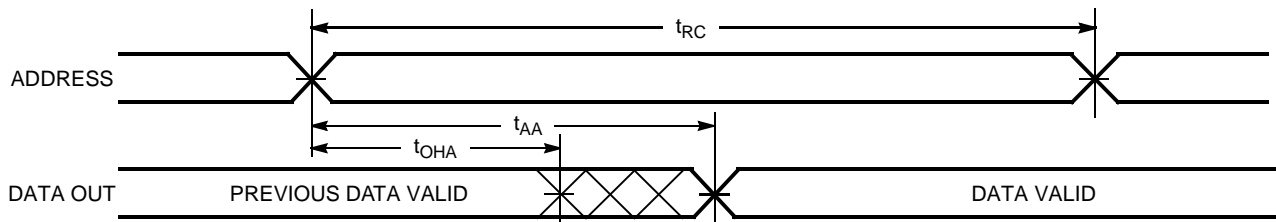
Parameter	Description	CY62256VN-70		Unit
		Min.	Max.	
<b>Read Cycle</b>				
t <sub>RC</sub>	Read Cycle Time	70		ns
t <sub>AA</sub>	Address to Data Valid		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z <sup>[8]</sup>	5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[8, 9]</sup>		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low-Z <sup>[8]</sup>	10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High-Z <sup>[8, 9]</sup>		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-up	0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-down		70	ns
<b>Write Cycle<sup>[10, 11]</sup></b>				
t <sub>WC</sub>	Write Cycle Time	70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	60		ns
t <sub>AW</sub>	Address Set-up to Write End	60		ns
t <sub>HA</sub>	Address Hold from Write End	0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	50		ns
t <sub>SD</sub>	Data Set-up to Write End	30		ns
t <sub>HD</sub>	Data Hold from Write End	0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[8, 9]</sup>		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[8]</sup>	10		ns

**Notes:**

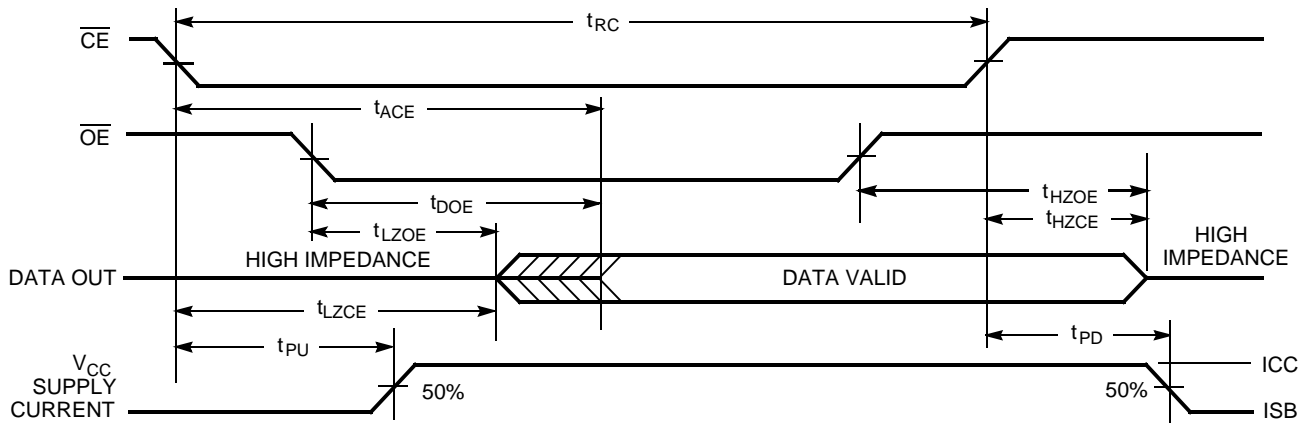
7. Test conditions assume signal transition time of 5 ns or less timing reference levels of  $V_{CC}/2$ , input pulse levels of 0 to  $V_{CC}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 100-pF load capacitance.
8. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
9. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

### Switching Waveforms

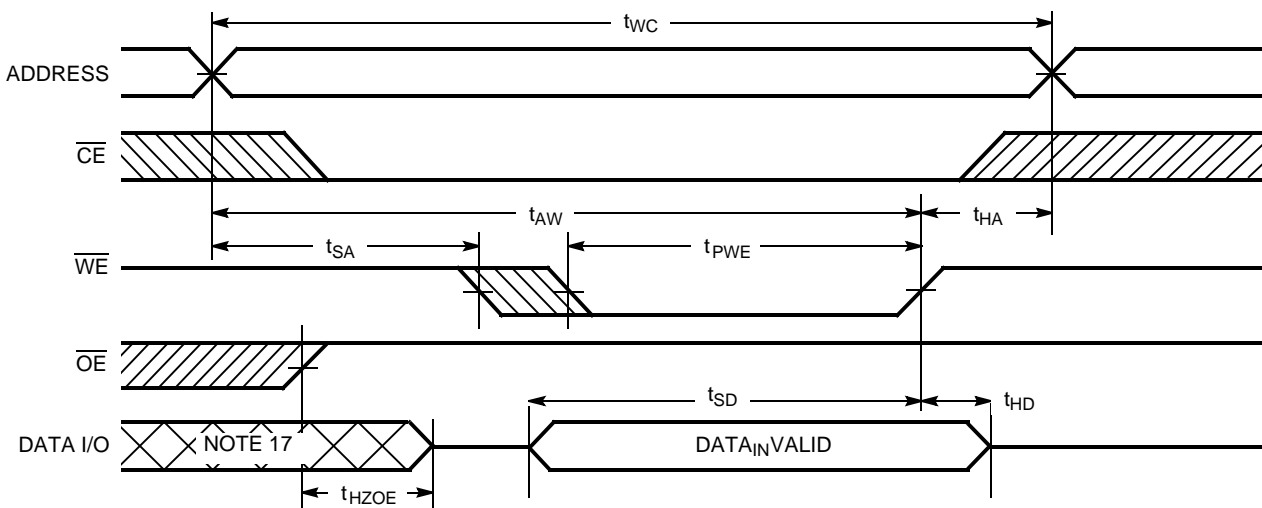
#### Read Cycle No. 1<sup>[12, 13]</sup>



#### Read Cycle No. 2<sup>[13, 14]</sup>



#### Write Cycle No. 1 ( $\overline{WE}$ Controlled)<sup>[10, 15, 16]</sup>

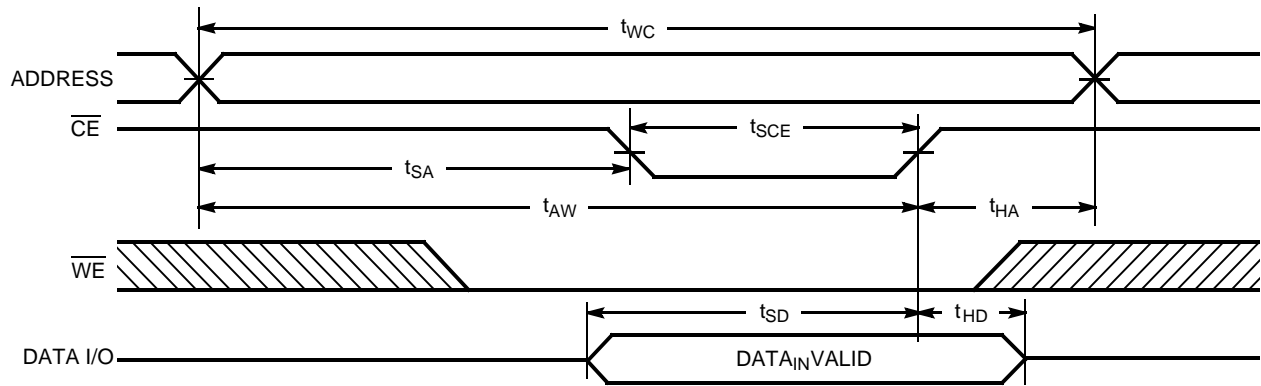


**Notes:**

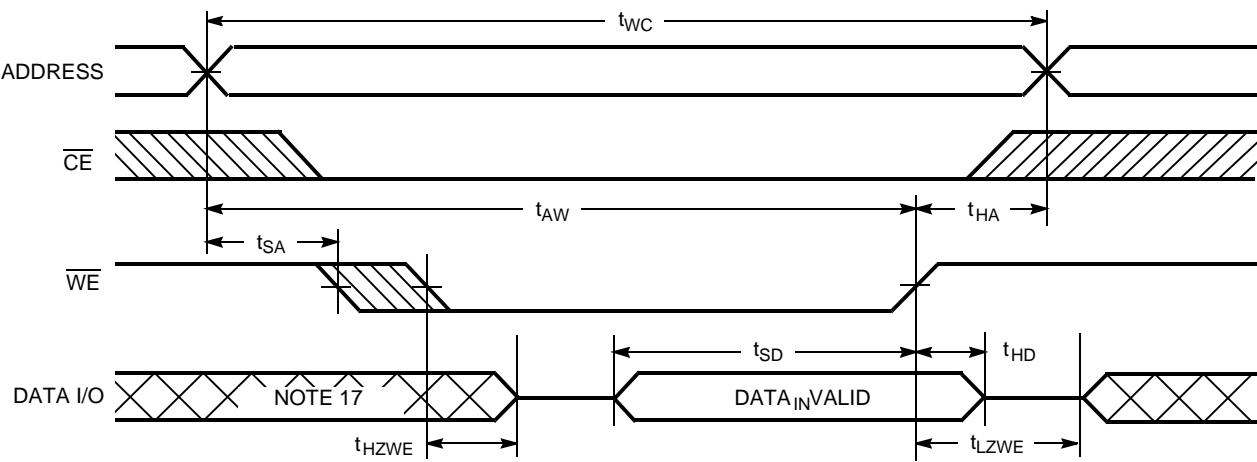
- 12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
- 13.  $\overline{WE}$  is HIGH for read cycle.
- 14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- 15. Data I/O is high impedance if  $\overline{OE} = V_{IL}$ .
- 16. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
- 17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

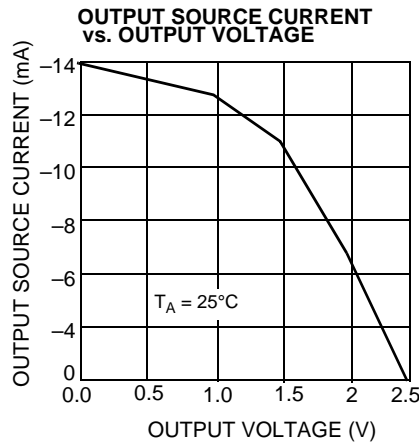
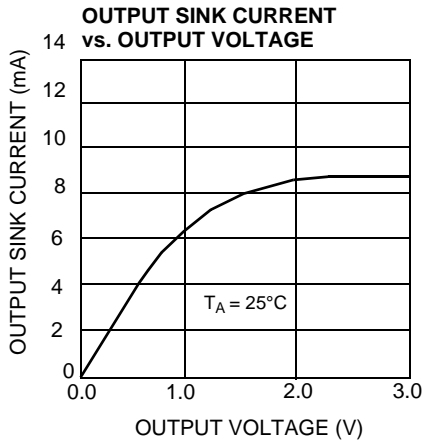
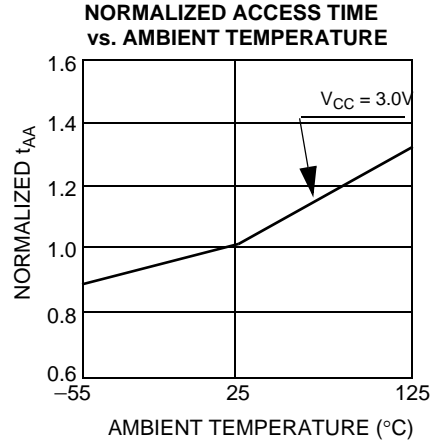
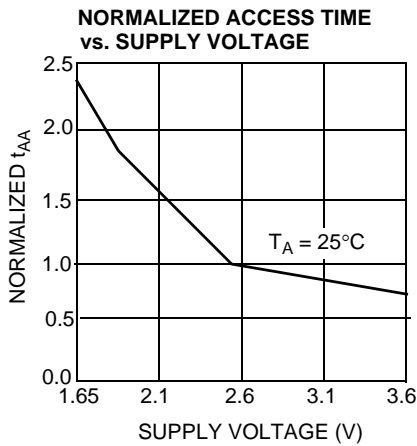
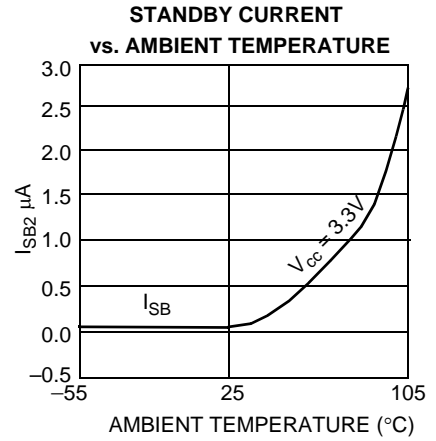
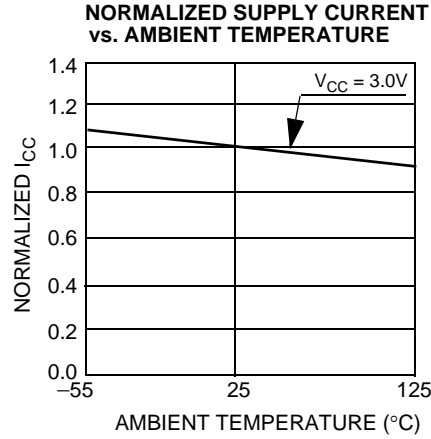
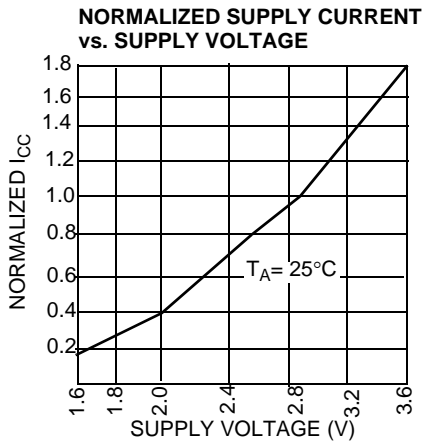
Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[10, 15, 16]</sup>



Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[11, 16]</sup>

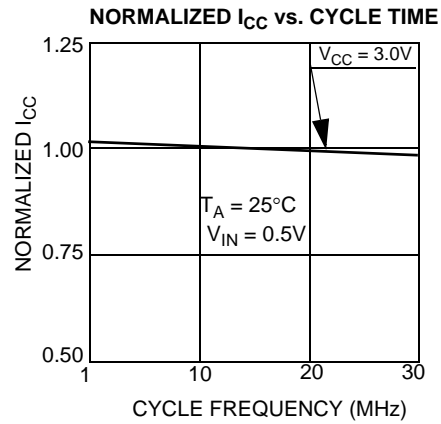
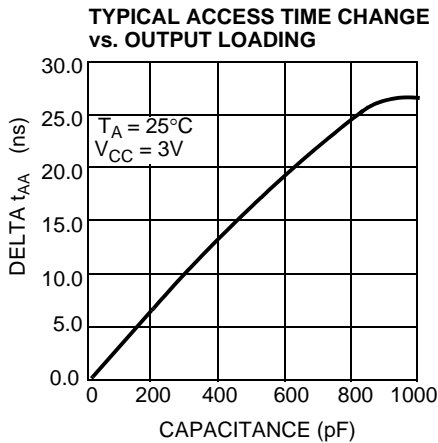


Typical DC and AC Characteristics





**Typical DC and AC Characteristics** (continued)



**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	High-Z	Deselect/Power-down	Standby ( $I_{\text{SB}}$ )
L	H	L	Data Out	Read	Active ( $I_{\text{CC}}$ )
L	L	X	Data In	Write	Active ( $I_{\text{CC}}$ )
L	H	H	High-Z	Deselect, Output Disabled	Active ( $I_{\text{CC}}$ )

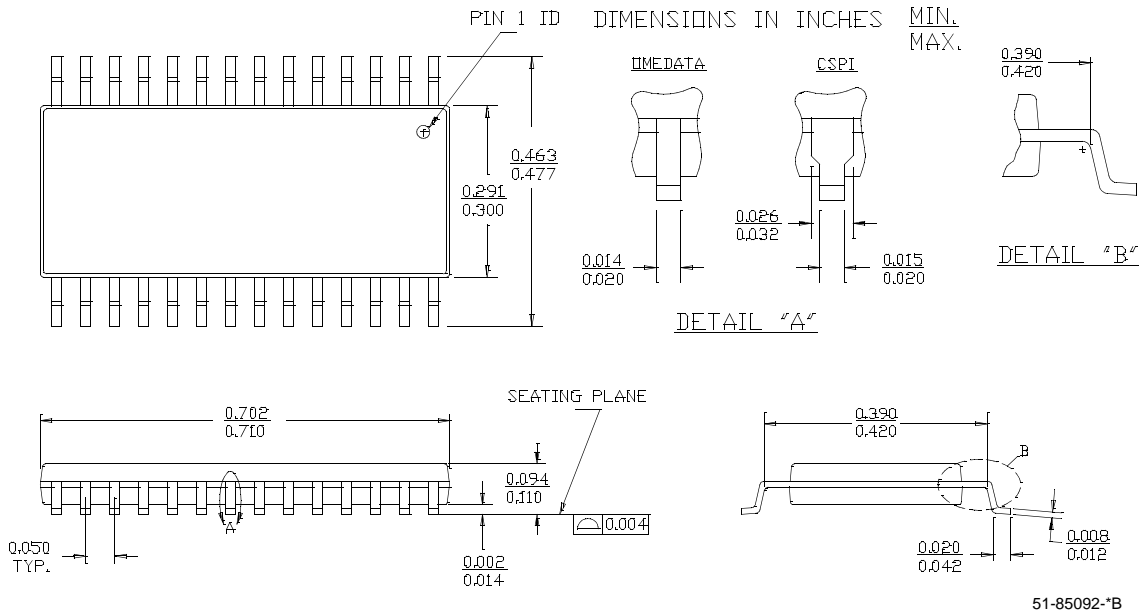
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62256VNLL-70SNC	51-85092	28-lead (300-mil) Narrow SOIC	Commercial
	CY62256VNLL-70SNXC		28-lead (300-mil) Narrow SOIC (Pb-Free)	
	CY62256VNLL-70ZC	51-85071	28-lead TSOP I	
	CY62256VNLL-70ZXC		28-lead TSOP I (Pb-Free)	
	CY62256VNLL-70SNXI	51-85092	28-lead (300-mil) Narrow SOIC (Pb-Free)	Industrial
	CY62256VNLL-70ZI	51-85071	28-lead TSOP I	
	CY62256VNLL-70ZXI		28-lead TSOP I (Pb-Free)	
	CY62256VNLL-70ZRI	51-85074	28-lead Reverse TSOP I	
	CY62256VNLL-70ZRXI		28-lead Reverse TSOP I (Pb-Free)	
	CY62256VNLL-70ZXA	51-85071	28-lead TSOP I (Pb-Free)	Automotive-A
	CY62256VNLL-70SNXE	51-85092	28-lead (300-mil) Narrow SOIC (Pb-Free)	Automotive-E
	CY62256VNLL-70ZXE	51-85071	28-lead TSOP I (Pb-Free)	
CY62256VNLL-70ZRXE	51-85074	28-lead Reverse TSOP I (Pb-Free)		

Please contact your local Cypress sales representative for availability of other parts

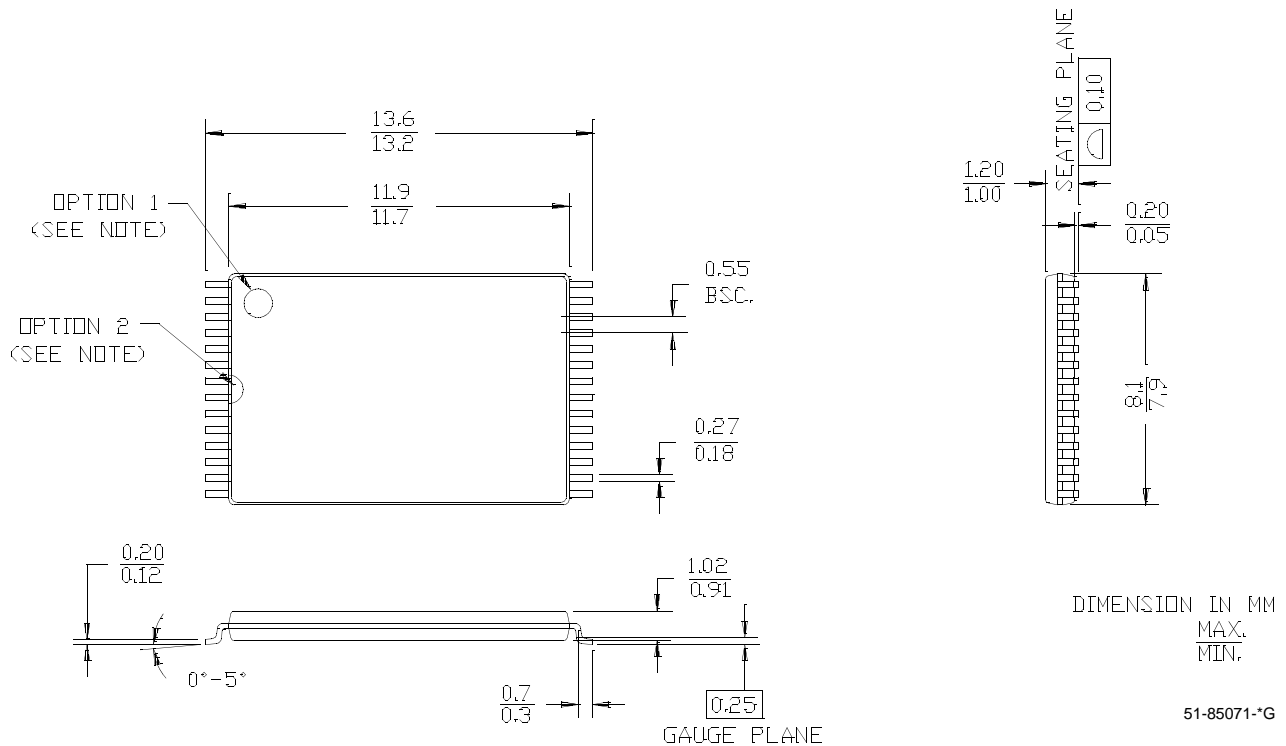
**Package Diagrams**

**28-lead (300-mil) SNC (Narrow Body) (51-85092)**



**28-lead TSOP 1 (8 x 13.4 mm) (51-85071)**

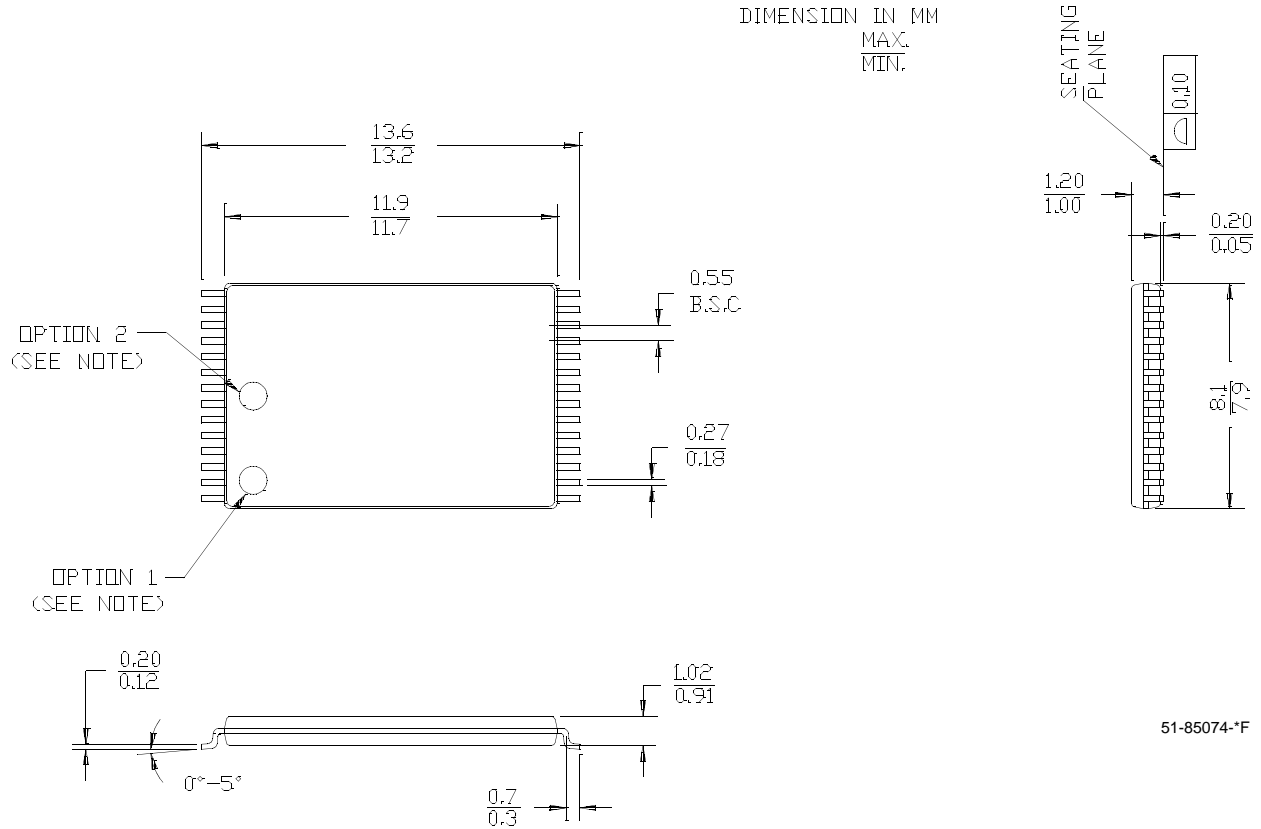
NOTE: ORIENTATION ID MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



Package Diagrams (continued)

28-lead Reverse TSOP 1 (8 x 13.4 mm) (51-85074)

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



51-85074-\*F

All product and company names mentioned in this document are the trademarks of their respective holders.

**Document History Page**

<b>Document Title: CY62256VN 256K (32K x 8) Static RAM</b> <b>Document Number: 001-06512</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	426504	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated ordering Information table