STOD03B

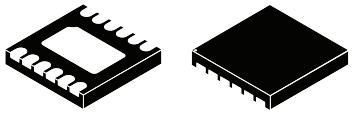
150 mA dual DC-DC converter with LDO for powering AMOLED displays

Features

- Step-up with LDO and inverter converters
- Operating input voltage range from 2.3 V to 4.8 V
- Synchronous rectification for both DC-DC converters
- Minimum 150 mA output current
- LDO post regulator for 4.6 V fixed positive output to provide line and load transient response with minimum output voltage ripple
- Programmable negative voltage by S_{WIRE} from - 2.4 V to -5.4 V at 100 mV steps
- Typical efficiency: 82%
- Pulse skipping mode in light load condition
- 1.5 MHz PWM mode control switching frequency
- Enable pin for shutdown mode
- Low quiescent current in shutdown mode
- Soft-start with inrush current protection
- Overtemperature protection
- Temperature range: -40 °C to 85 °C
- True-shutdown mode
- Package DFN (3 x 3) 12 leads 0.6 mm height

Applications

- Active matrix AMOLED power supply in portable devices
- Cellular phones
- Camcorders and digital still cameras
- Multimedia players



DFN12L (3 x 3 mm)

Description

The STOD03B is a dual DC-DC converter for AMOLED display panels. It integrates a step-up and an inverting DC-DC converter making it particularly suitable for battery operated products, in which the major concern is the overall system efficiency. It works in pulse skipping mode during low load conditions and PWM-MODE at 1.5 MHz frequency for medium/high load conditions. The high frequency allows the value and size of external components to be reduced. The 4.6 V output is provided by an LDO in cascade with the step-up converter. This allows a noise and ripple free positive output for the AMOLED panel to provide stable picture quality. The Enable pin allows the device to be turned off, therefore reducing the current consumption to less than 1 µA. The negative output voltage can be programmed by an MCU through a dedicated pin which implements single-wire protocol. Soft-start with controlled inrush current limit and thermal shutdown are integrated functions of the device.

Table 1. Device summary

Order code	Positive voltage	Negative voltage	Package	Packaging
STOD03BTPUR	4.6V	- 2.4V to - 5.4V	DFN12L (3 x 3mm)	3000 parts per reel

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1 Schematic

Figure 1. Application schematic

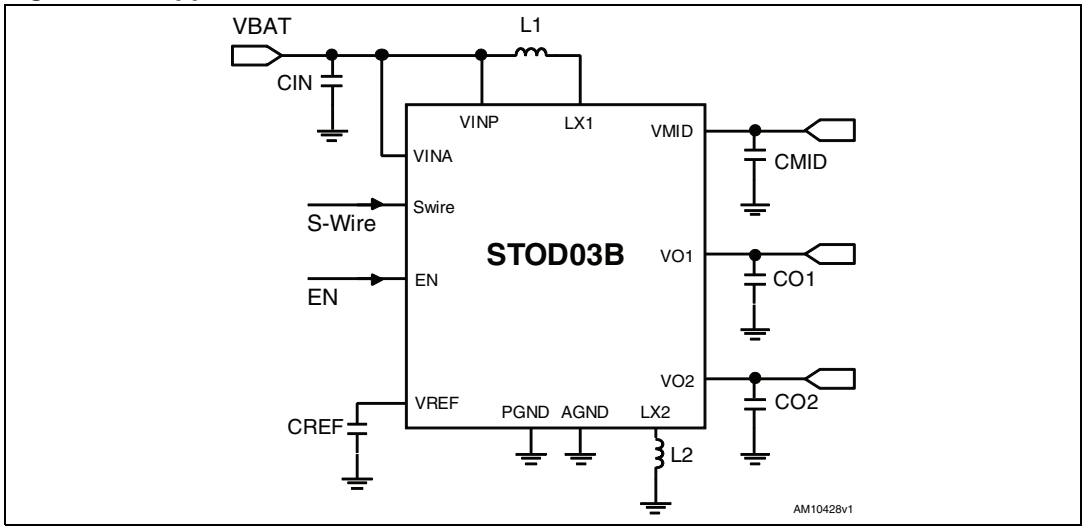


Table 2. Typical external components

Comp.	Manufacturer	Part number	Value	Size	Ratings
L_1 (1)	COILCRAFT MURATA SEMCO ABCO ABCO	LPS4012-472ML LQH3NPN4R7MJ0 CIG22B4R7MNE LPF2810T-4R7M LPF2807T-4R7M	4.7µH	4.0 x 4.0 x 1.2 3.0 x 3.0 x 1.1 2.5 x 2.0 x 1.0 2.8 x 2.8 x 1.0 2.8 x 2.8 x 0.7	±20%, curr. 1.7A, res. 0.175Ω ±20%, curr. 1.1A, res. 0.156Ω ±20%, curr. 1.1A, res. 0.300Ω ±20%, curr. 0.85A, res. 0.33Ω ±20%, curr. 0.70A, res. 0.44Ω
L_2 (2)	COILCRAFT MURATA TOKO ABCO	LPS4012-472ML LQH3NPN4R7MJ0 DFE252012C 1239AS-H-4R7N LPF2807T-4R7M	4.7µH	4.0 x 4.0 x 1.2 3.0 x 3.0 x 1.1 2.5 x 2.0 x 1.2 2.8 x 2.8 x 0.7	±20%, curr. 1.7A, res. 0.175Ω ±20%, curr. 1.1A, res. 0.156Ω ±30%, curr. 1.2A, res. 0.252Ω ±20%, curr. 0.70A, res. 0.44Ω
C_{IN}	MURATA TAIYO YUDEN	GRM219R61A106KE44 LMK212BJ106KD-T	10µF	0805 0805	±10%, X5R, 10V ±10%, X5R, 10V
C_{O1}	MURATA TAIYO YUDEN	GRM219R61A106KE44 LMK212BJ106KD-T	10µF	0805 0805	±10%, X5R, 10V ±10%, X5R, 10V
C_{O2}	MURATA TAIYO YUDEN	GRM219R61A106KE44 LMK212BJ106KD-T	10µF	0805 0805	±10%, X5R, 10V ±10%, X5R, 10V

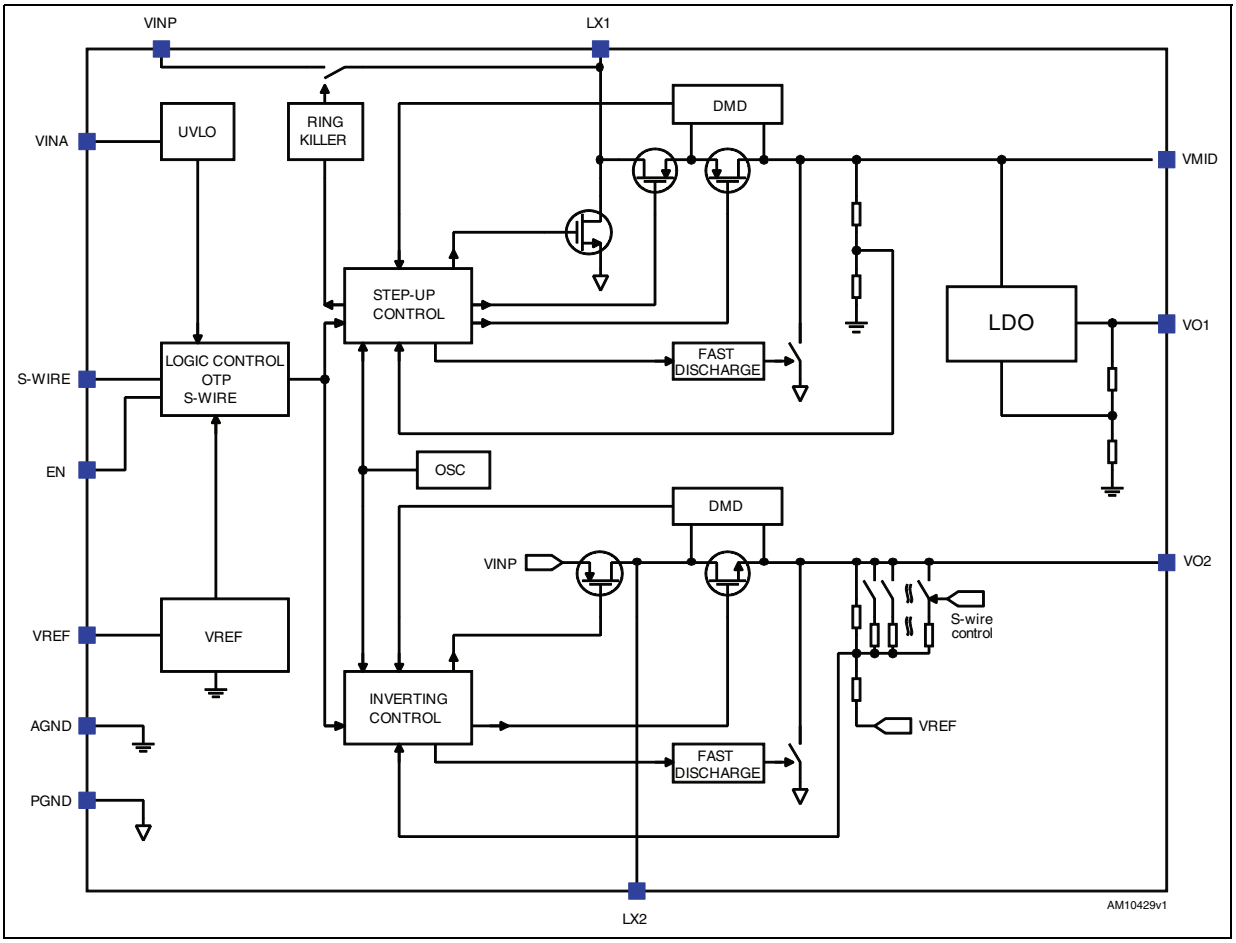
Table 2. Typical external components (continued)

Comp.	Manufacturer	Part number	Value	Size	Ratings
C_{MID}	MURATA TAIYO YUDEN	GRM219R61A106KE44 LMK212BJ106KD-T	10µF	0805 0805	±10%, X5R, 10V ±10%, X5R, 10V
C_{REF}	MURATA TAIYO YUDEN	GRM185R60J105KE26 JMK107BJ105KK-T	1µF	0805 0805	±10%, X5R, 10V ±10%, X5R, 10V

1. A 200 mA load can be provided with inductor saturation current as a minimum of 0.6 A.
2. For V_{O2} in a range between - 4.9 V to -5.4 V, a load current of 150 mA to 200 mA can be provided using inductors with a saturation current as a minimum of 1 A. See *Section 7.1.1*.

Note: All the above components refer to the typical application performance characteristics. Operation of the device is not limited to the choice of these external components. Inductor values ranging from 3.3 µH to 6.8 µH can be used together with STOD03B.

Figure 2. Block schematic



2 Pin configuration

Figure 3. Pin configuration (top view)

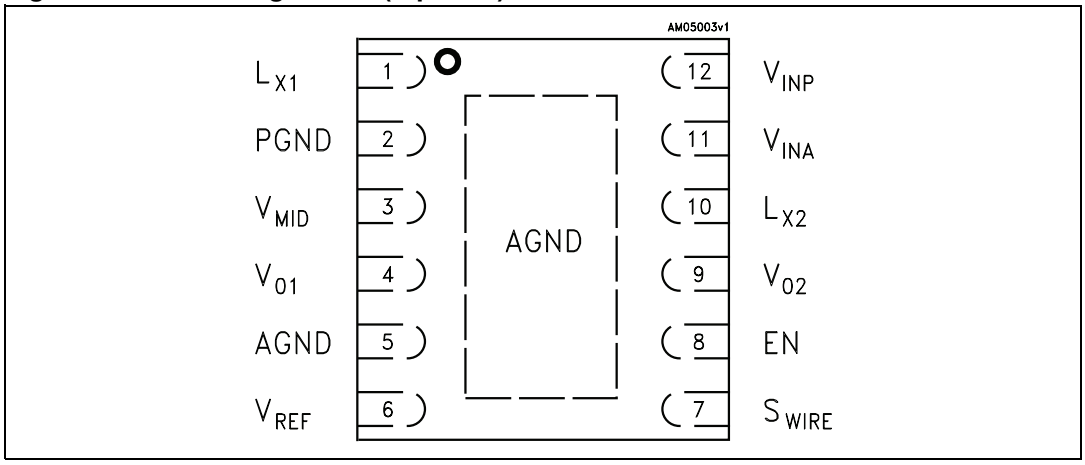


Table 3. Pin description

Pin name	Pin n°	Description
Lx_1	1	Boost converter switching node
PGND	2	Power ground pin
V_{MID}	3	Step-up converter output voltage (4.9V)
V_{O1}	4	4.6V fixed LDO output
AGND	5	Signal ground pin. This pin must be connected to the power ground layer
V_{REF}	6	Voltage reference output. 1µF bypass capacitor must be connected between this pin and AGND
S_{WIRE}	7	Negative voltage setting pin.
EN	8	Enable control pin. High 1 converter on; low or floating = converter in shutdown mode (1)
V_{O2}	9	Inverting converter output voltage
Lx_2	10	Inverting converter switching node
$V_{IN\ A}$	11	Analogic input supply voltage
$V_{iN\ P}$	12	Power input supply voltage
	Exposed pad	Internally connected to AGND. Exposed pad must be connected to ground layers in the PCB layout in order to guarantee proper operation of the device

1. No pull-up/pull-down resistors are needed.

3 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{INA}, V_{INP}	DC supply voltage	-0.3 to 6	V
EN, S_{WIRE}	Logic input pins	-0.3 to 4.6	V
IL_{X2}	Inverting converter switching current	Internally limited	A
L_{X2}	Inverting converter switching node voltage	-10 to V_{INP}+0.3	V
V_{O2}	Inverting converter output voltage	-10 to AGND+0.3	V
V_{O1}, V_{MID}	LDO and step-up converter output voltage	-0.3 to 6	V
L_{X1}	Step-up converter switching node voltage	-0.3 to V_{MID}+0.3	V
IL_{X1}	Step-up converter switching current	Internally limited	A
V_{REF}	Reference voltage	-0.3 to 3	V
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	°C
ESD	Human Body Model Protection	± 2	kV
	Machine Body Model Protection	± 200	kV

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 5. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	33	°C/W
R_{thJC}	Thermal resistance junction-case (FR-4 PCB) (1)	2.12	°C/W

1. The package is mounted on a 4-layer (2S2P) JEDEC board as per JESD51-7.

4 Electrical characteristics

T_J = 25 °C, V_{INA} = V_{INP} = 3.7 V, $I_{O1,2}$ = 30 mA, C_{IN} = 2 x10 µF, C_{MID} = 2 x10 µF, C_{O1} = 10 µF, C_{O2} = 2 x10 µF, C_{REF} = 1 µF, L1 = L2 = 4.7 µH, V_{EN} = 2 V, V_{MID} = 4.9 V, V_{O1} = 4.6 V, V_{O2} = -4.9 V unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{INA}, V_{INP}	Supply input voltage		2.3		4.8	V
UVLO_H	Undervoltage lockout HIGH	V_{INA} rising		2.22	2.25	V
UVLO_L	Undervoltage lockout LOW	V_{INA} falling	1.9	2.18		V
I_V_I	Input current	No load condition (sum of V_{INA} and V_{INP})		1.3	1.7	mA
I_{Q_SH}	Shutdown current	V_{EN}=GND (sum of V_{INA} and V_{INP}); T_J=-40°C to +85°C;			1	µA
V_{EN} H	Enable high threshold	V_{INA}=2.3V to 4.8V, T_J=-40°C to +85°C;	1.2			V
V_{EN} L	Enable low threshold				0.4	
I_{EN}	Enable input current	V_{EN}=V_{INA}=4.8V; T_J=-40°C to +85°C;			1	µA
f_S	Switching frequency	PWM mode	1.35	1.5	1.65	MHz
$D1_{MAX}$	Step-up maximum duty cycle	No load		87		%
$D2_{MAX}$	Inverting maximum duty cycle	No load		87		%
η	Total system efficiency	$I_{O1,O2}$=10 to 30mA, V_{O1}=4.6V, V_{O2}=-4.9V		75		%
		$I_{O1,O2}$=30 to 150mA, V_{O1}=4.6V, V_{O2}=-4.9V		82		%
V_{REF}	Voltage reference	I_{REF}=10µA	1.195	1.207	1.219	V
I_{REF}	Voltage reference current capability	At 98.5% of no load reference voltage	100			µA
OTP	Overtemperature protection			140		°C
OTP_{HYST}	Overtemperature protection hysteresis			15		°C
Positive output section						
V_{O1}	Positive voltage total variation	V_{INA}=V_{INP}=2.3V to 4.8V; T_J=-40°C to +85°C; I_{O1}=5mA to 150mA, I_{O2} no load	4.554	4.6	4.646	V
ΔV_{O1LT}	Line transient	$V_{INA,P}$=3.5V to 3.0V, I_{O1}=100mA; T_R=T_F=50µs		-12		mV
ΔV_{O1T}	Load transient regulation	I_{O1}=3 to 30mA and I_{O1}=30 to 3mA, T_R=T_F=150µs		±20		mV

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
TDMA Noise	TDMA noise immunity	I_{O1}=5 to 100mA; I_{O2} no load (1)		±20		mV
$I_{O1\ MAX}$	Max. output current	$V_{INA,P}$=2.9V to 4.8V	150			mA
V_{MID}	Positive voltage total variation	V_{INA}=V_{INP}=2.9V to 4.8V; I_{MID}=5mA to 150mA; I_{O2} no load; T_J=25°C	4.8	4.9	5.0	V
	Temperature accuracy	V_{INA}=V_{INP}=3.7V; I_{MID}=5mA; I_{O2} no load; T_J=-40 to +85°C;	-05		0.5	%
$I\text{-}L_{1MAX}$	Step-up inductor peak current	V_{MID} 10% below nominal value	1		1.1	A
$R_{DSON}P1$	P-channel Static Drain-source On resistance	V_{INA}=V_{INP}=3.7V, $I_{SW\text{-}P1}$=100mA		1.0	1.6	Ω
$R_{DSON}N1$	N-channel Static Drain-source On resistance	V_{INA}=V_{INP}=3.7V, $I_{SW\text{-}P1}$=100mA		0.4	0.7	Ω
Negative output						
V_{O2}	Negative output voltage range	31 different values set by the S_{WIRE} pin (see S_{WIRE})	-5.4		-2.4	V
	Negative output voltage total variation on default value	V_{INA}=V_{INP}=2.9V to 4.8V; T_J=25°C; I_{O2}=5mA to 150mA, I_{O1} no load	-4.97	-4.9	-4.83	V
	Temperature accuracy	V_{INA}=V_{INP}=3.7V; I_{O2}=5mA; I_{O2} no load; T_J=-40°C to +85°C	-0.5		0.5	%
ΔV_{O2LT}	Line transient	$V_{INA,P}$=3.5V to 3.0V, I_{O2}=100mA, T_R=T_F=50µs		+12		mV
ΔV_{O2T}	Load transient regulation	I_{O2}=3 to 30mA and I_{O2}=30 to 3mA, T_R=T_F=150µs		±20		mV
	Load transient regulation	I_{O2}=10 to 100mA and I_{O2}=100 to 10mA, T_R=T_F=150µs		±25		mV
TDMA Noise	TDMA noise immunity	I_{O2}=5 to 100mA; I_{O1} no load		±25		mV
$I_{O2\ MAX}$	Maximum output current	$V_{INA,P}$=2.9V to 4.8V	-150			mA
$I\text{-}L_{2MAX}$	Inverting peak current	V_{O2} below 10% of nominal value	-1.2		-0.9	A
$R_{DSON}P2$	P-channel Static Drain-source On resistance	V_{INA}=V_{INP}=3.7V; $I_{SW\text{-}P2}$=100mA		0.42	0.8	Ω
$R_{DSON}N2$	N-channel Static Drain-source On resistance	V_{INA}=V_{INP}=3.7V; $I_{SW\text{-}P2}$=100mA		0.43	0.8	Ω

1. $V_{INA,P}$ = 4.2 to 3.7 V, 3.7 to 3.2 V, 3.4 to 2.9 V, f = 200 Hz, t_{ON} = 3.65 ms, t_{OFF} = 1.25 ms, T_R = T_F = 50 µs, pulse signal.

5 Typical performance characteristics

V_{O2} = -4.9 V; T_J = 25 °C; See *Table 1*. for external components used in the tests below.

Figure 4. Max power output vs. V_{IN}

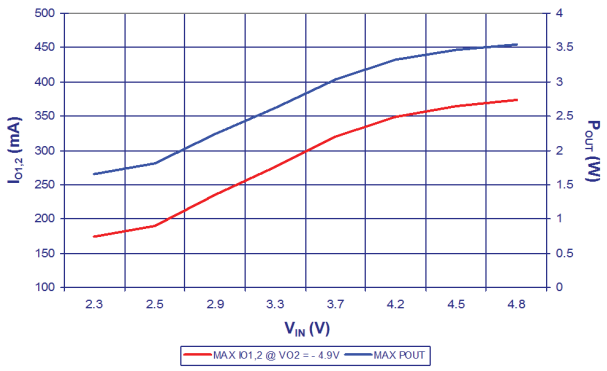


Figure 5. Efficiency vs. output current

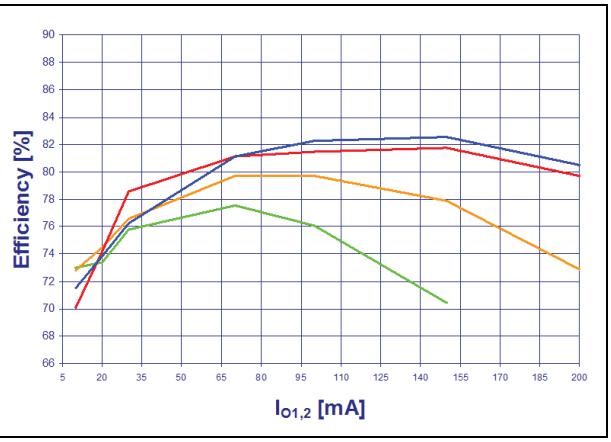
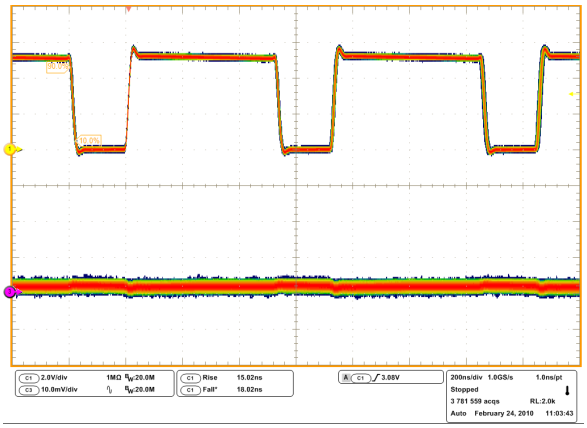
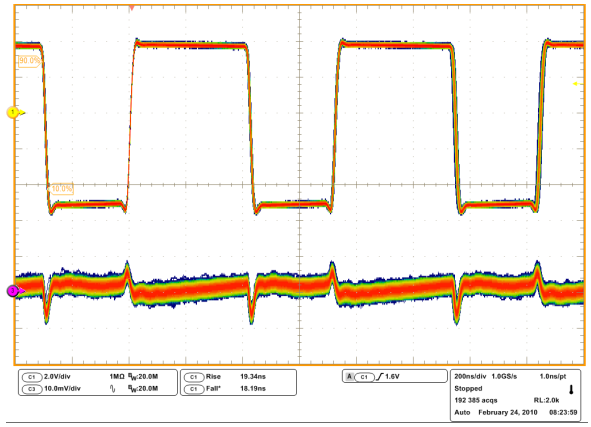


Figure 6. Positive output operation



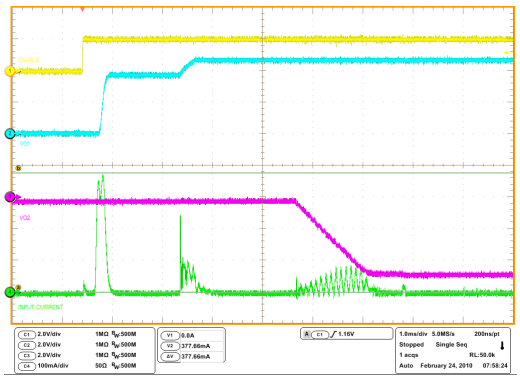
I_{O1} = 100 mA

Figure 7. Negative output operation



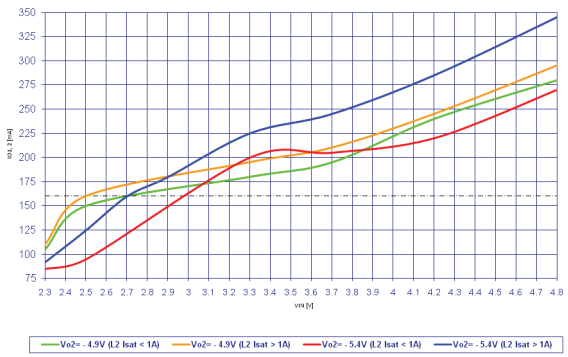
I_{O2} = 100 mA

Figure 8. Soft-start inrush current



I_O = 200 mA, V_{O2} = - 4.9 V

Figure 9. Output current vs. input voltage



V_{INA} = V_{INAP} = 2.3 to 4.8 V, V_{O1} = 4.6 V

6 Detailed description

6.1 S_{WIRE}

- Protocol: to digitally communicate over a single cable with single-wire components
- Single-wire's 3 components:

1. An external MCU
2. Wiring and associated connectors
3. STOD03B device with a dedicated single-wire pin.

6.1.1 S_{WIRE} features and benefits

- Fully digital signal
- No handshake needed
- Protection against glitches and spikes though an internal low pass filter acting on falling edge
- Uses a single wire (plus analog ground) to accomplish both communication and power control transmission
- Simplify design with an interface protocol that supplies control and signaling over a single-wire connection to set the output voltages.

6.1.2 S_{WIRE} protocol

- Single-wire protocol uses conventional CMOS/TTL logic levels (maximum 0.6 V for logic "zero" and a minimum 1.2 V for logic "one") with operation specified over a supply voltage range of 2.3 V to 4.8 V
- Both master (MCU) and slave (STOD03B) are configured to permit bit sequential data to flow only in one direction at a time; master initiates and controls the device
- Data is bit-sequential with a START bit and a STOP bit
- Signal is transferred in real time
- System clock is not required; each single-wire pulse is self-clocked by the oscillator integrated in the master and is asserted valid within a frequency range of 250 kHz (maximum).

6.1.3 S_{WIRE} basic operations

- The negative output voltage levels are selectable within a wide range (steps of 100 mV)
- The device can be enabled / disabled via S_{WIRE} in combination with the Enable pin.

6.2 Negative output voltage levels

Table 7. Default output voltage

Pulse	V_{O2}	Pulse	V_{O2}	Pulse	V_{O2}
1	-5.4	11	-4.4	21	-3.4
2	-5.3	12	-4.3	22	-3.3
3	-5.2	13	-4.2	23	-3.2
4	-5.1	14	-4.1	24	-3.1
5	-5.0	15	-4.0	25	-3.0
6 (1)	-4.9	16	-3.9	26	-2.9
7	-4.8	17	-3.8	27	-2.8
8	-4.7	18	-3.7	28	-2.7
9	-4.6	19	-3.6	29	-2.6
10	-4.5	20	-3.5	30	-2.5
				31	-2.4

1. Default value.

6.3 Enable and S_{WIRE}

Table 8. EN and S_{WIRE} operation table (1)

Enable	S_{WIRE}	Action
Low	Low	Device off
Low	High	Negative output voltage set by S_{WIRE}
High	Low	Default negative output voltage
High	High	Default negative output voltage

1. The Enable pin must be set to AGND while using the S_{WIRE} function.

7 Application information

7.1 External passive components

7.1.1 Inductor selection

Magnetic shielded low ESR power inductors must be chosen as the key passive components for switching converters.

For the step-up converter an inductance between 4.7 µH and 6.8 µH is recommended.

For the inverting stage the suggested inductance ranges from 3.3 µH to 4.7 µH.

It is very important to select the right inductor according to the maximum current the inductor can handle to avoid saturation. The step-up and the inverting peak current can be calculated as follows:

Equation 1

$$I_{PEAK-BOOST} = \frac{V_{MID} \times I_{OUT}}{\eta 1 \times VIN_{MIN}} + \frac{VIN_{MIN} \times (V_{MID} - VIN_{MIN})}{2 \times V_{MID} \times fs \times L1}$$

Equation 2

$$I_{PEAK-INVERTING} = \frac{(VIN_{MIN} - VO2_{MIN}) x I_{OUT}}{\eta 2 \times VIN_{MIN}} + \frac{VIN_{MIN} \times VO2_{MIN}}{2 \times (VO2_{MIN} - VIN_{MIN}) \times fs \times L2}$$

where

V_{MID}: step-up output voltage, fixed at 4.9 V;

V_{O2}: inverting output voltage including sign (minimum value is the absolute maximum value);

I_O: output current for both DC-DC converters;

V_{IN}: input voltage of STOD03B;

f_s: switching frequency. Use the minimum value of 1.35 MHz for the worst case;

$\eta 1$: efficiency of step-up converter. Typical value is 0.70;

$\eta 2$: efficiency of inverting converter. Typical value is 0.60.

The negative output voltage can be set via S_{WIRE} at -5.4 V. Accordingly, the inductor peak current, at the maximum load condition, increases. A proper inductor, with a saturation current as a minimum of 1 A, is preferred.

STOD03B is capable of supplying a load current from 150 mA to 200 mA. Inductors with a saturation current as a minimum of 1 A must be selected.

7.1.2 Input and output capacitor selection

It is recommended to use X5R or X7R low ESR ceramic capacitors as input and output capacitors in order to filter any disturbance present in the input line and to obtain stable operation for the two switching converters. A minimum real capacitance value of 6 µF must be guaranteed for C_{MID}, C_{O1} and C_{O2} in all conditions. Considering tolerance, temperature variation and DC polarization, 2 x 10 µF, 10 V ±10% as C_{MID}, a 10 µF 10V ±10% capacitor as C_{O1} and 2 x 10 µF 10 V ±10% as CO2 can be used to achieve the needed 6 µF.

7.2 Recommended PCB layout

The STOD03B is a high frequency power switching device and therefore requires a proper PCB layout in order to obtain the necessary stability and optimize line/load regulation and output voltage ripple.

Analog input (V_{INA}) and power input (V_{INP}) must be kept separated and connected together at the C_{IN} pad only. The input capacitor must be as close as possible to the IC.

In order to minimize ground noise, a common ground node for power ground and a different one for analog ground must be used. In the recommended layout, the AGND node is placed close to C_{REF} ground while the PGND node is centered at C_{IN} ground. They are connected by a separated layer routing on the bottom through vias.

The exposed pad is connected to AGND through vias.

Figure 10. Top layer and top silk-screen (top view, not to scale)

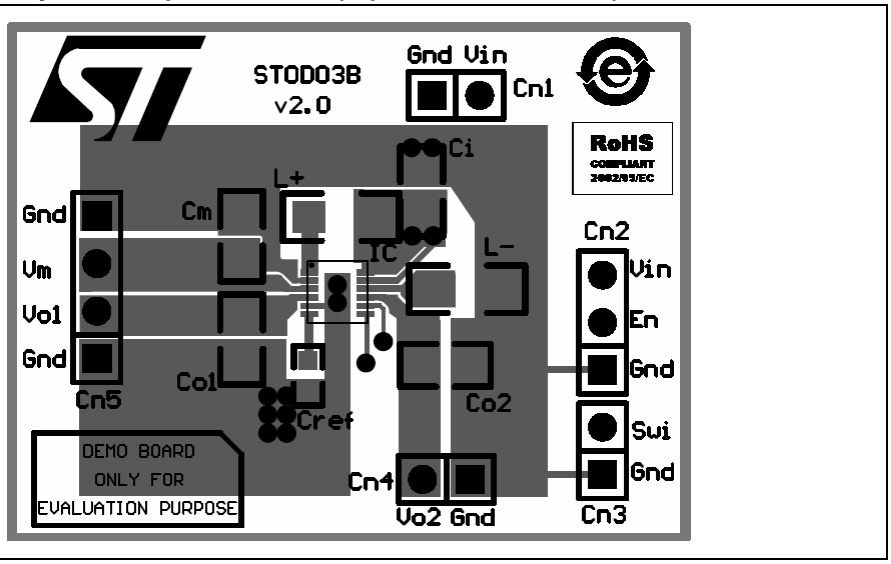
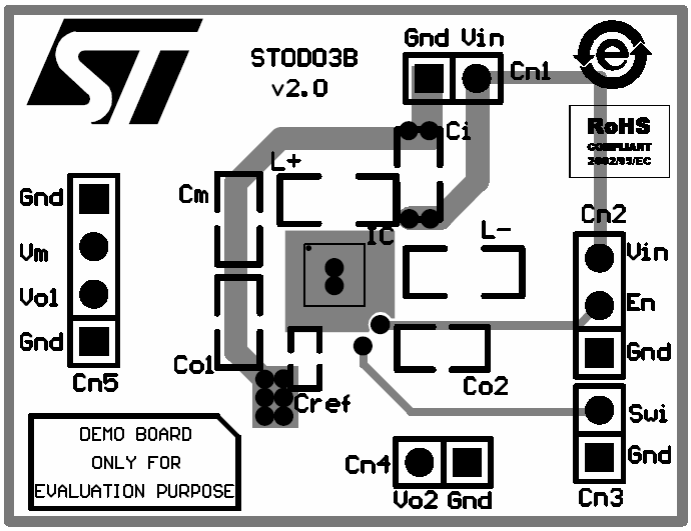


Figure 11. Bottom layer and silk-screen (top view, not to scale)



8 Detailed description

8.1 General description

The STOD03B is a high efficiency dual DC-DC converter which integrates a step-up with an LDO and inverting power stages suitable for supplying AMOLED panels. Thanks to the high level of integration it needs only 6 external components to operate and it achieves very high efficiency using a synchronous rectification technique for each of the two DC-DC converters. This topology of a boost followed by an LDO regulator offers an efficient ripple reduction solution for loads up to 200 mA. The controller uses an average current mode technique in order to obtain good stability and precise voltage regulation in all possible conditions of input voltage, output voltage, and output current. In addition, the peak inductor current is monitored in order to avoid saturation of the coils. The STOD03B implements a power saving technique in order to maintain high efficiency at very light load and it switches to PWM operation as the load increases, in order to guarantee the best dynamic performance and low noise operation. The STOD03B avoids battery leakage thanks to the true-shutdown feature and it is self protected by overtemperature. Undervoltage lockout and soft-start guarantee proper operation during startup.

8.1.1 Multiple operation modes

Both the step-up and the inverting stage of the STOD03B operate in three different modes: pulse skipping mode (PSM), discontinuous conduction mode (DCM), and continuous conduction mode (CCM). It switches automatically between the three modes according to input voltage, output current, and output voltage conditions.

Pulse skipping operation:

The STOD03B works in pulse skipping mode when the load current is below a few mA.

The load current level at which this way of operating occurs depends on input voltage only for the step-up converter and on input voltage and negative output voltage (V_{O2}) for the inverting converter.

Discontinuous conduction mode:

When the load increases above some tens of mA, the STOD03B enters DCM operation.

In order to obtain this type of operation the controller must avoid the inductor current going negative. The discontinuous mode detector (DMD) blocks sense the voltage across the synchronous rectifiers (P1B for the step-up and N2 for the inverting) and turn off the switches when the voltage crosses a defined threshold which, in turn, represents a certain current in the inductor. This current can vary according to the slope of the inductor current which depends on input voltage, inductance value, and output voltage.

Continuous conduction mode:

At medium/high output loads, the STOD03B enters full CCM at constant switching frequency mode for each of the two DC-DC converters.

8.1.2 Enable pin

The device operates when the EN pin is set high. If the EN pin is set low, the device stops switching, and all the internal blocks are turned off. In this condition the current drawn from V_{INP}/V_{INA} is below 1 µA in the whole temperature range. In addition, the internal switches are in an OFF state so the load is electrically disconnected from the input, this avoids unwanted current leakage from the input to the load.

8.1.3 Soft-start and inrush current limiting

After the EN pin is pulled high, or after a suitable voltage is applied to V_{INP}, V_{INA} and EN, the device initiates the startup phase. As a first step, the C_{MID} capacitor is charged and the P1B switch implements a current limiting technique in order to keep the charge current below 400 mA. This avoids the battery overloading during startup. After V_{MID} reaches the V_{INP} voltage level, the P1B switch is fully turned on and the soft-start procedure for the step-up is started.

After around 2 ms the soft-start for the inverting is started. The positive and negative voltages are under regulation by around 6 ms after the EN pin is asserted high.

8.1.4 Undervoltage lockout

The undervoltage lockout function avoids improper operation of the STOD03B when the input voltage is not high enough. When the input voltage is below the UVLO threshold the device is in shutdown mode. The hysteresis of 50 mV avoids unstable operation when the input voltage is close to the UVLO threshold.

8.1.5 Overtemperature protection

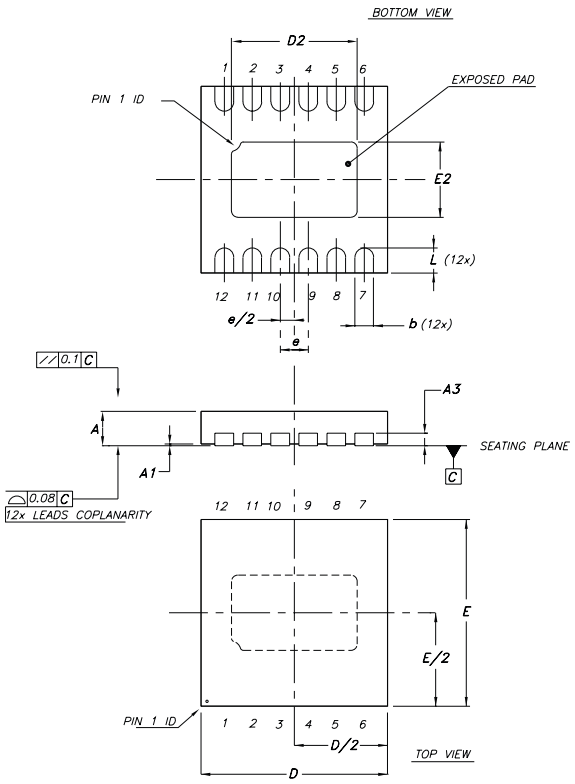
An internal temperature sensor continuously monitors the IC junction temperature. If the IC temperature exceeds 140 °C, typical, the device stops operating. As soon as the temperature falls below 125 °C, typical, normal operation is restored.

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

DFN12L (3 x 3 x 0.6 mm) mechanical data

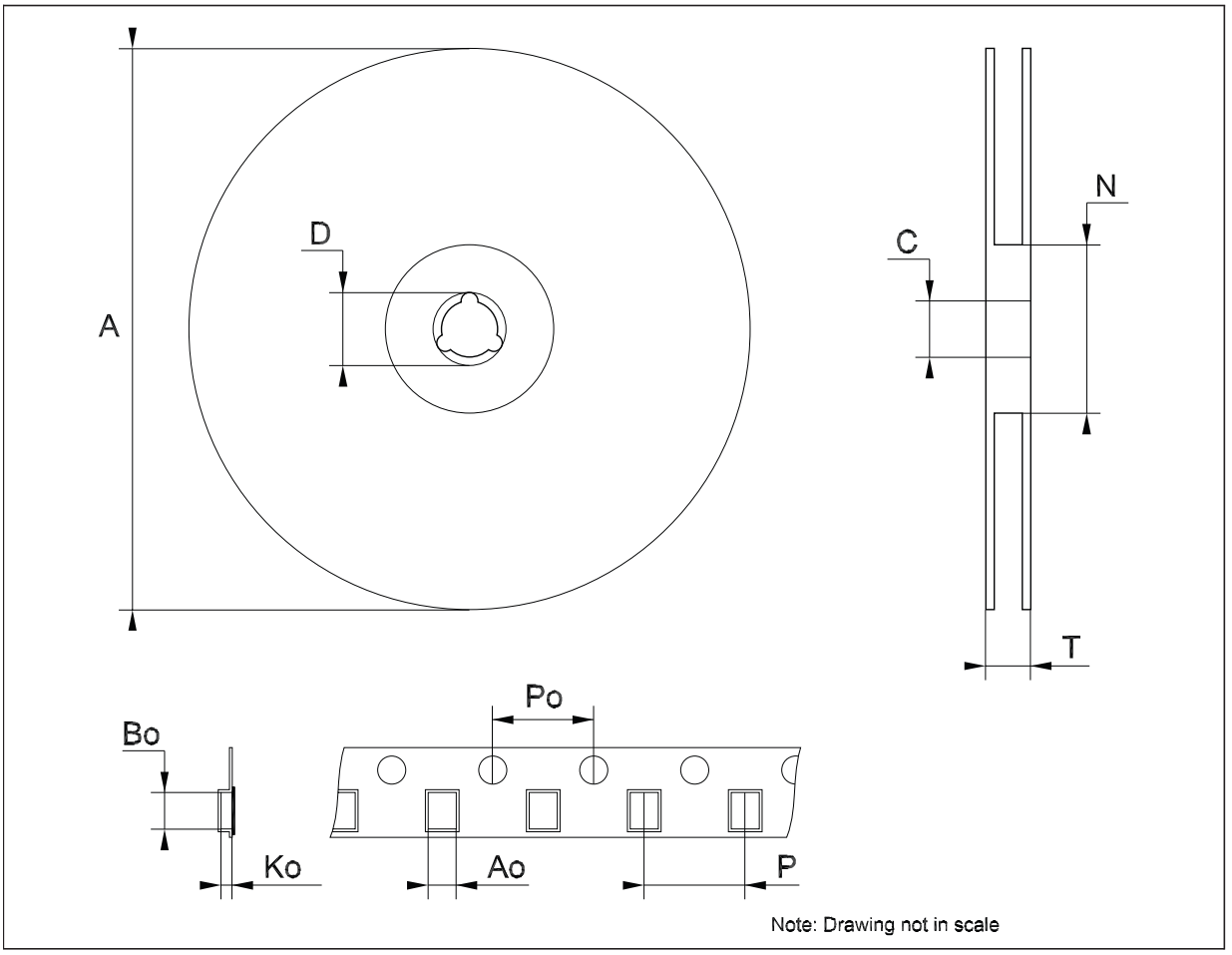
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	2.85	3	3.15	0.112	0.118	0.124
D2	1.87	2.02	2.12	0.074	0.080	0.083
E	2.85	3	3.15	0.112	0.118	0.124
E2	1.06	1.21	1.31	0.042	0.048	0.052
e		0.45			0.018	
L	0.30	0.40	0.50	0.012	0.016	0.020



8085116/A

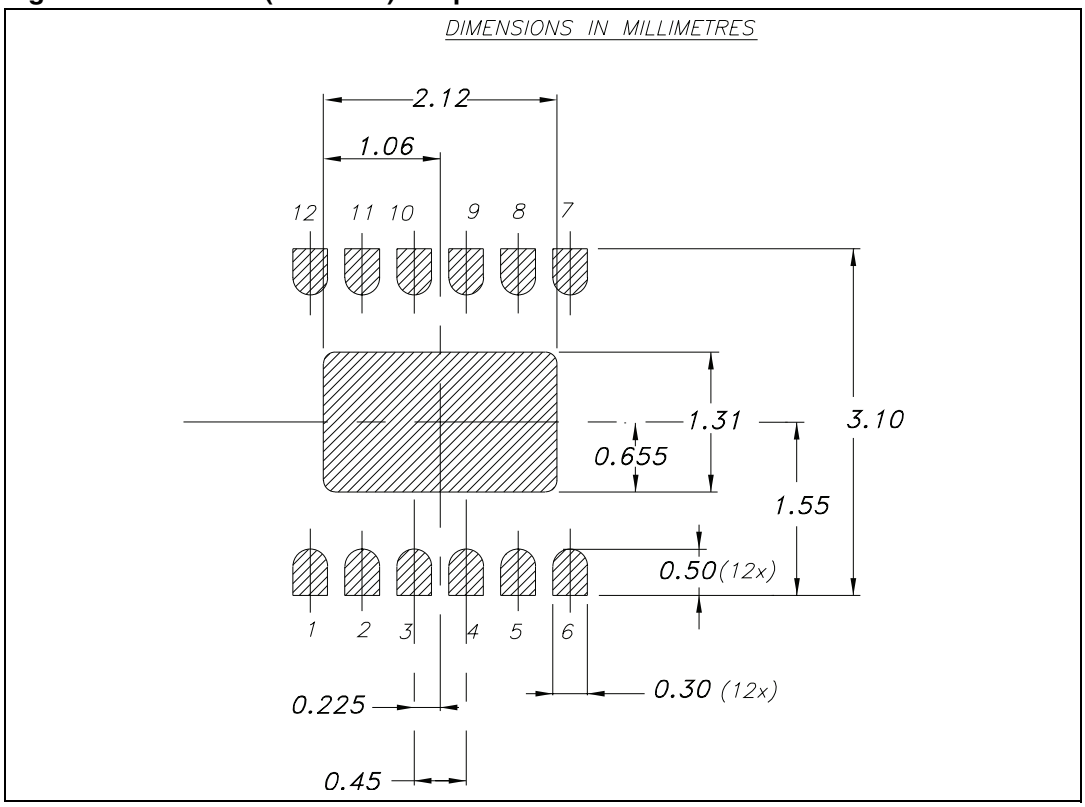
Tape & reel QFNxx/DFNxx (3x3) mechanical data

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

Figure 12. DFN12L (3 x 3 mm) footprint recommended data



10 Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Dec-2011	1	Initial release.

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