IF Diversity Receiver

AD6649

FEATURES

SNR = 73.0 dBFS in a 95 MHz bandwidth at 185 MHz A_{IN} and 245.76 MSPS
SFDR = 85 dBc at 185 MHz A_{IN} and 250 MSPS
Noise density = −151.2 dBFS/Hz input at 185 MHz, −1 dBFS A_{IN} and 250 MSPS
Total power consumption: 1 W with fixed-frequency NCO, 95 MHz FIR filter
1.8 V supply voltages
LVDS (ANSI-644 levels) outputs
Integer 1-to-8 input clock divider (625 MHz maximum input)
Integrated dual-channel ADC
- **Sample rates of up to 250 MSPS**
- **IF sampling frequencies to 400 MHz**
- **Internal ADC voltage reference**
- **Flexible input range**
  - **1.4 V p-p to 2.1 V p-p (1.75 V p-p nominal)**
- **ADC clock duty cycle stabilizer**
- **95 dB channel isolation/crosstalk**

Integrated wideband digital processor
- **32-bit complex numerically controlled oscillator (NCO)**
- **FIR filter with 2 modes**
- **Real output from an $f_S/4$ output NCO**

Amplitude detect bits for efficient AGC implementation
Energy saving power-down modes
Decimated, interleaved real LVDS data outputs

APPLICATIONS

Communications
Diversity radio systems
Multimode digital receivers (3G)
- **TD-SCDMA, WiMax, WCDMA, CDMA2000, GSM, EDGE, LTE**

General-purpose software radios
Broadband data applications

GENERAL DESCRIPTION

The AD6649 is a mixed-signal intermediate frequency (IF) receiver consisting of dual 14-bit, 250 MSPS ADCs and a wideband digital downconverter (DDC). The AD6649 is designed to support communications applications, where low cost, small size, wide bandwidth, and versatility are desired.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

FUNCTIONAL BLOCK DIAGRAM

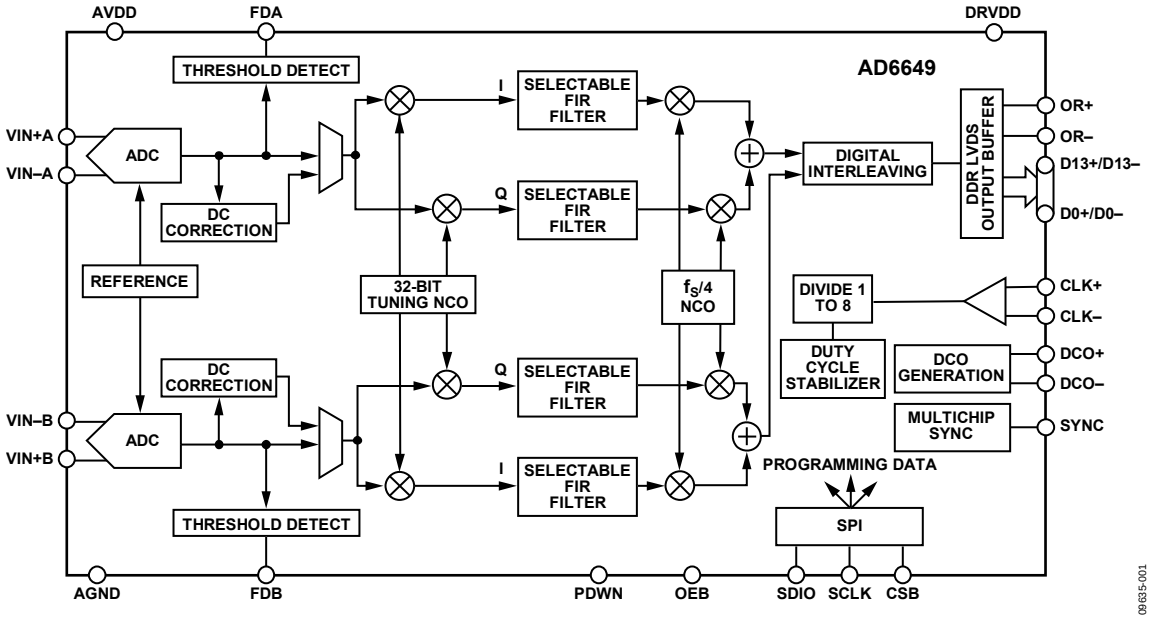

Figure 1.

Rev. 0

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REVISION HISTORY

4/11—Revision 0: Initial Version

ADC data outputs are internally connected directly to the digital downconverter (DDC) of the receiver. The digital receiver has two channels and provides processing flexibility. Each receive channel has four cascaded signal processing stages: a 32-bit frequency translator (numerically controlled oscillator (NCO)), an optional sample rate converter, a fixed FIR filter, and an $f_S/4$ fixed-frequency NCO.

In addition to the receiver DDC, the AD6649 has several functions that simplify the automatic gain control (AGC) function in the system receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

After digital processing, data is routed directly to the 14-bit output port. These outputs operate at ANSI or reduced swing LVDS signal levels.

The AD6649 receiver digitizes a wide spectrum of IF frequencies. Each receiver is designed for simultaneous reception of the main channel and the diversity channel. This IF sampling architecture greatly reduces component cost and complexity compared with traditional analog techniques or less integrated digital methods. In diversity applications, the output data format is real due to the final NCO, which shifts the output center frequency to $f_S/4$.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-pin SPI-compatible serial interface.

The AD6649 is available in a 64-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Integrated dual, 14-bit, 250 MSPS ADCs.
2. Integrated wideband filter and 32-bit complex NCO.
3. Fast overrange and threshold detect.
4. Proprietary differential input maintains excellent SNR performance for input frequencies of up to 400 MHz.
5. SYNC input allows synchronization of multiple devices.
6. 3-pin, 1.8 V SPI port for register programming and register readback.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input,[1] 1.75 V p-p full-scale input range, duty cycle stabilizer (DCS) enabled, NCO enabled, FIR filter enabled, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full			±10	mV
Gain Error	Full	−5.5		+2.5	%FSR
MATCHING CHARACTERISTIC					
Offset Error	Full			±13	mV
Gain Error	Full			±2.5	%FSR
TEMPERATURE DRIFT					
Offset Error	Full		±15		ppm/°C
Gain Error	Full		±50		ppm/°C
INPUT REFERRED NOISE					
VREF = 1.0 V	25°C		1.32		LSB rms
ANALOG INPUT					
Input Span	Full		1.75		V p-p
Input Capacitance[2]	Full		2.5		pF
Input Resistance[3]	Full		20		kΩ
Input Common-Mode Voltage	Full		0.9		V
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
Supply Current					
I_{AVDD}[4]	Full		271	275	mA
I_{DRVDD}[4] (Fixed-Frequency NCO, 95 MHz FIR Filter)	Full		283	300	mA
I_{DRVDD}[4] (Tunable-Frequency NCO, 100 MHz FIR Filter)	Full		375		mA
POWER CONSUMPTION					
Sine Wave Input (Fixed-Frequency NCO, 95 MHz FIR Filter)	Full		997	1035	mW
Sine Wave Input (Tunable-Frequency NCO, 100 MHz FIR Filter)	Full		1163		mW
Standby Power[5]	Full		104		mW
Power-Down Power	Full		10		mW

[1] A −1.0 dBFS input level at the analog inputs corresponds to an output level of −2.5 dBFS when using the fixed-frequency NCO and 95 MHz FIR filter. When using the tunable-frequency NCO and 100 MHz FIR filter, the output level is −1.3 dBFS. These respective output level reductions are due to FIR filter losses. See the FIR Filters section for more details.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Input resistance refers to the effective resistance between one differential input pin and its complement.
[4] Measured with a 185 MHz, full-scale sine wave input on both channels and an NCO frequency of 62.5 MHz ($f_S/4$).
[5] Standby power is measured with a dc input and the CLK pin inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input,[1] 1.75 V p-p full-scale input range, DCS enabled, NCO enabled, FIR filter enabled, unless otherwise noted.

Table 2.

Parameter[2]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)[3]					
f_{IN} = 30 MHz	25°C		74.5		dBFS
f_{IN} = 90 MHz	25°C		74.2		dBFS
f_{IN} = 140 MHz	25°C		73.9		dBFS
f_{IN} = 185 MHz	25°C		73.4		dBFS
	Full	70.9			dBFS
f_{IN} = 220 MHz	25°C		72.9		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)					
f_{IN} = 30 MHz	25°C		73.4		dBFS
f_{IN} = 90 MHz	25°C		73.0		dBFS
f_{IN} = 140 MHz	25°C		72.3		dBFS
f_{IN} = 185 MHz	25°C		71.7		dBFS
	Full	68.7			dBFS
f_{IN} = 220 MHz	25°C		71.0		dBFS
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 30 MHz	25°C		−92		dBc
f_{IN} = 90 MHz	25°C		−88		dBc
f_{IN} = 140 MHz	25°C		−85		dBc
f_{IN} = 185 MHz	25°C		−85		dBc
	Full			−80	dBc
f_{IN} = 220 MHz	25°C		−89		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 30 MHz	25°C		92		dBc
f_{IN} = 90 MHz	25°C		88		dBc
f_{IN} = 140 MHz	25°C		85		dBc
f_{IN} = 185 MHz	25°C		85		dBc
	Full	80			
f_{IN} = 220 MHz	25°C		84		dBc
WORST OTHER HARMONIC OR SPUR					
f_{IN} = 30 MHz	25°C		−95		dBc
f_{IN} = 90 MHz	25°C		−94		dBc
f_{IN} = 140 MHz	25°C		−93		dBc
f_{IN} = 185 MHz	25°C		−93		dBc
	Full			−80	dBc
f_{IN} = 220 MHz	25°C		−84		dBc
TWO-TONE SFDR					
f_{IN} = 184.12 MHz, 187.12 MHz (−7 dBFS)	25°C		88		dBc
CROSSTALK[4]	Full		95		dB
ANALOG INPUT BANDWIDTH	25°C		1000		MHz

[1] A −1.0 dBFS input level at the analog inputs corresponds to an output level of −2.5 dBFS when using the fixed-frequency NCO and 95 MHz FIR filter. When using the tunable-frequency NCO and 100 MHz FIR filter, the output level is −1.3 dBFS. These respective output level reductions are due to FIR filter losses. See the FIR Filters section for more details.
[2] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[3] SNR specifications are for filtered 95 MHz bandwidth.
[4] Crosstalk is measured at 100 MHz with −1 dBFS on one channel and with no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input,[1] 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	+10		+22	µA
Low Level Input Current	Full	−22		−10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS/LVDS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−5		+5	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
LOGIC INPUT (CSB)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−80		−45	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK)[3]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUTS (OEB, PDWN)[3]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA

Parameter	Temperature	Min	Typ	Max	Unit
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
FDA and FDB					
High Level Output Voltage					
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V
LVDS Data and OR Outputs					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	250	350	450	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	150	200	280	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] A −1.0 dBFS input level at the analog inputs corresponds to an output level of −2.5 dBFS when using the fixed-frequency NCO and 95 MHz FIR filter. When using the tunable-frequency NCO and 100 MHz FIR filter, the output level is −1.3 dBFS. These respective output level reductions are due to FIR filter losses. See the FIR Filters section for more details.
[2] Pull-up.
[3] Pull-down.

SWITCHING SPECIFICATIONS

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS					
Input Clock Rate	Full			625	MHz
Conversion Rate[1]	Full	40		250	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	4.0			ns
CLK Pulse Width High (t_{CH})					
Divide-by-1 Mode, DCS Enabled	Full	1.8	2.0	2.2	ns
Divide-by-1 Mode, DCS Disabled	Full	1.9	2.0	2.1	ns
Divide-by-3 Through Divide-by-8 Modes, DCS Enabled	Full	0.8			ns
DATA OUTPUT PARAMETERS (DATA, OR)					
Data Propagation Delay (t_{PD})	Full		4.8		ns
DCO Propagation Delay (t_{DCO})	Full		5.5		ns
DCO-to-Data Skew (t_{SKEW})	Full	0.1	0.7	1.3	ns
Pipeline Delay—Fixed-Frequency NCO, 95 MHz FIR Filter (Latency)	Full		23		Cycles
Pipeline Delay—Tunable-Frequency NCO, 100 MHz FIR Filter (Latency)	Full		43		Cycles
Aperture Delay (t_A)	Full		1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1		ps rms
Wake-Up Time (from Standby)	Full		10		µs
Wake-Up Time (from Power-Down)	Full		250		µs
OUT-OF-RANGE RECOVERY TIME	Full		3		Cycles

[1] Conversion rate is the clock rate after the divider.

TIMING SPECIFICATIONS

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to the rising edge of CLK setup time		0.3		ns
t_{HSYNC}	SYNC to the rising edge of CLK hold time		0.4		ns
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

Timing Diagrams

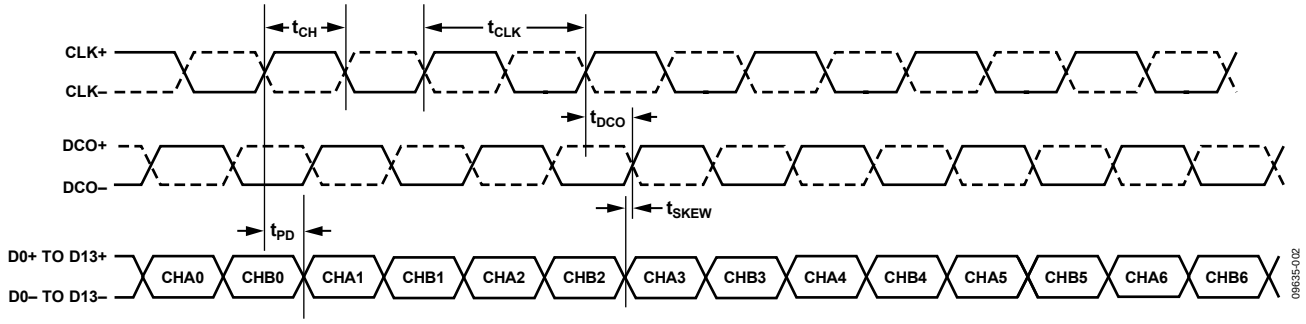


Figure 2. Interleaved LVDS Mode Data Output Timing

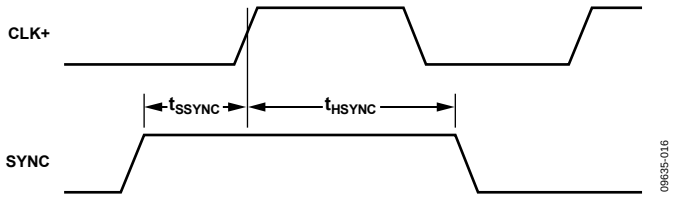


Figure 3. SYNC Timing Inputs

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.3 V
SCLK to AGND	−0.3 V to DRVDD + 0.3 V
SDIO to AGND	−0.3 V to DRVDD + 0.3 V
OEB to AGND	−0.3 V to DRVDD + 0.3 V
PDWN to AGND	−0.3 V to DRVDD + 0.3 V
D0−/D0+ through D13−/D13+ to AGND	−0.3 V to DRVDD + 0.3 V
FDA/FDB to AGND	−0.3 V to DRVDD + 0.3 V
OR+/OR− to AGND	−0.3 V to DRVDD + 0.3 V
DCO+/DCO− to AGND	−0.3 V to DRVDD + 0.3 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Unit
64-Lead LFCSP 9 mm × 9 mm (CP-64-4)	0	26.8	1.14	10.4	°C/W
	1.0	21.6			°C/W
	2.0	20.2			°C/W

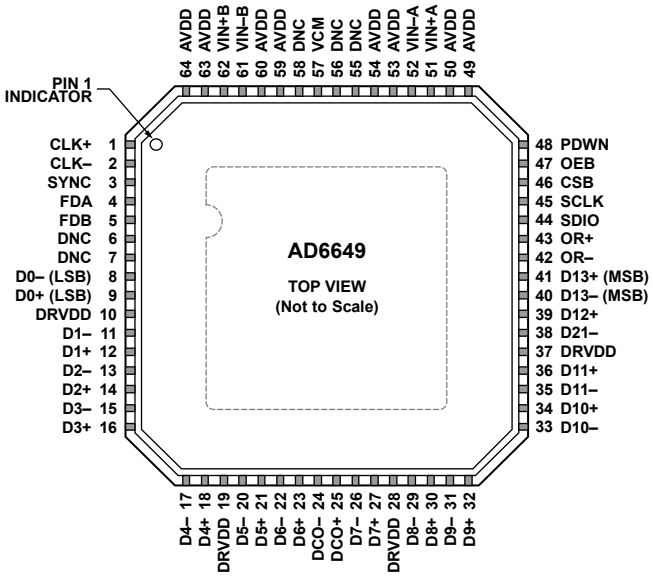
[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with solid ground plane. As shown in Table 7, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED THERMAL PADDLE ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PADDLE MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Figure 4. LFCSP Interleaved Parallel LVDS Pin Configuration (Top View)

Table 8. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
6, 7, 55, 56, 58	DNC		Do Not Connect. Do not connect to this pin.
0	AGND, Exposed Paddle	Ground	Analog Ground. The exposed thermal paddle on the bottom of the package provides the analog ground for the part. This exposed paddle must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. This pin should be decoupled to ground using a 0.1 µF capacitor.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
ADC Fast Detect Outputs			
4	FDA	Output	Channel A Fast Detect Indicator (CMOS Levels).
5	FDB	Output	Channel B Fast Detect Indicator (CMOS Levels).
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
9	D0+ (LSB)	Output	Channel A/Channel B LVDS Output Data 0—True.
8	D0− (LSB)	Output	Channel A/Channel B LVDS Output Data 0—Complement.
12	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
11	D1−	Output	Channel A/Channel B LVDS Output Data 1—Complement.
14	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
13	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
16	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.

Pin No.	Mnemonic	Type	Description
15	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
18	D4+	Output	Channel A/Channel B LVDS Output Data 4—True.
17	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
21	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
20	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
23	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
22	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
27	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
26	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
30	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
29	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
32	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
31	D9−	Output	Channel A/Channel B LVDS Output Data 9—Complement.
34	D10+	Output	Channel A/Channel B LVDS Output Data 10—True.
33	D10−	Output	Channel A/Channel B LVDS Output Data 10—Complement.
36	D11+	Output	Channel A/Channel B LVDS Output Data 11—True.
35	D11−	Output	Channel A/Channel B LVDS Output Data 11—Complement.
39	D12+	Output	Channel A/Channel B LVDS Output Data 12—True.
38	D12−	Output	Channel A/Channel B LVDS Output Data 12—Complement.
41	D13+ (MSB)	Output	Channel A/Channel B LVDS Output Data 13—True.
40	D13− (MSB)	Output	Channel A/Channel B LVDS Output Data 13—Complement.
43	OR+	Output	Channel A/Channel B LVDS Overrange—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK	Input	SPI Serial Clock.
44	SDIO	Input/Output	SPI Serial Data Input/Output.
46	CSB	Input	SPI Chip Select (Active Low).
Output Enable and Power-Down			
47	OEB	Input/Output	Output Enable Input (Active Low).
48	PDWN	Input/Output	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby (see Table 14).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, sample rate = 250 MSPS, DCS enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, 32k sample, T_A = 25°C, fixed-frequency NCO, 95 MHz BW FIR filter, unless otherwise noted. In the FFT plots that follow, the location of the second and third harmonics is noted when they fall in the pass band of the filter. A −1.0 dBFS input level at the analog inputs corresponds to an output level of −2.5 dBFS when using the fixed-frequency NCO and 95 MHz FIR filter. When using the tunable-frequency NCO and 100 MHz FIR filter, the output level is −1.3 dBFS. These respective output level reductions are due to FIR filter losses. See the FIR Filters section for more details.

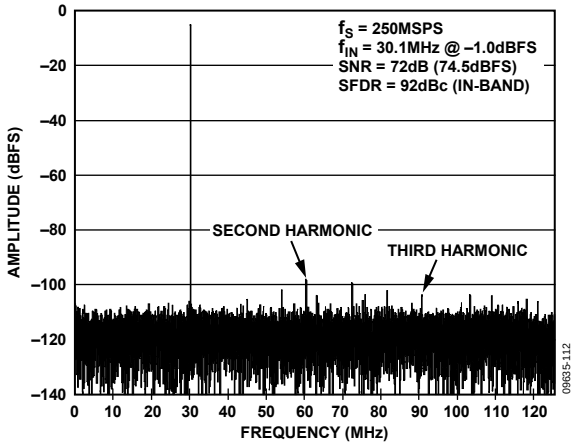


Figure 5. AD6649 Single-Tone FFT with f_{IN} = 30.1 MHz

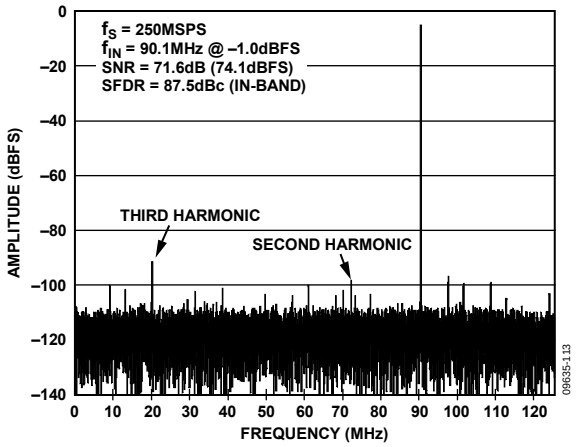


Figure 6. AD6649 Single-Tone FFT with f_{IN} = 90.1 MHz

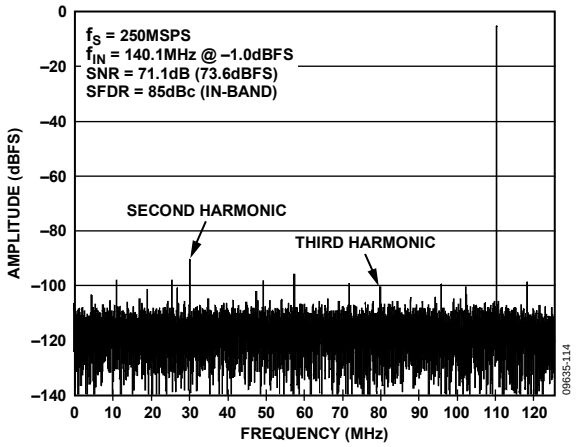


Figure 7. AD6649 Single-Tone FFT with f_{IN} = 140.1 MHz

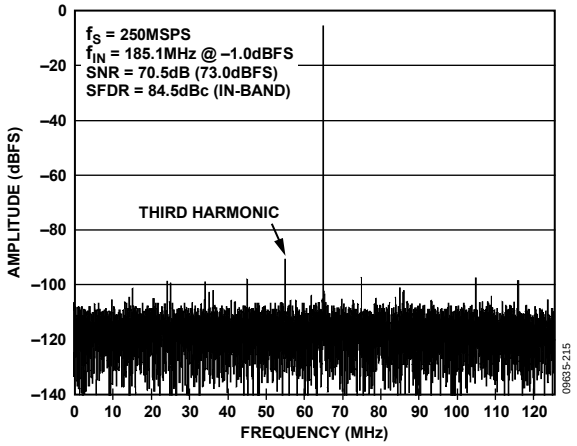


Figure 8. AD6649 Single-Tone FFT with f_{IN} = 185.1 MHz

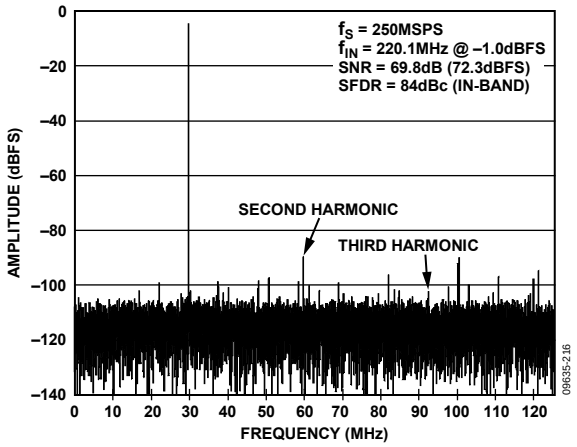


Figure 9. AD6649 Single-Tone FFT with f_{IN} = 220.1 MHz

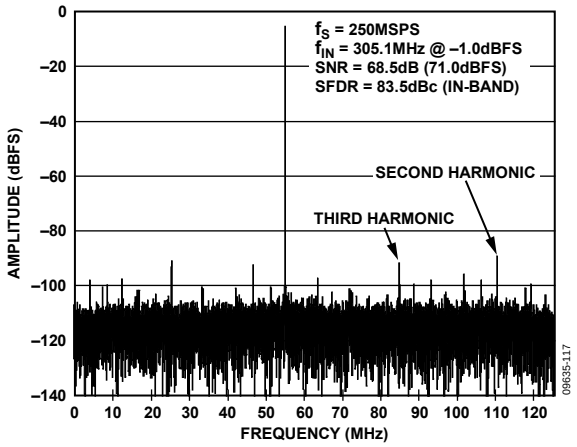


Figure 10. AD6649 Single-Tone FFT with f_{IN} = 305.1 MHz

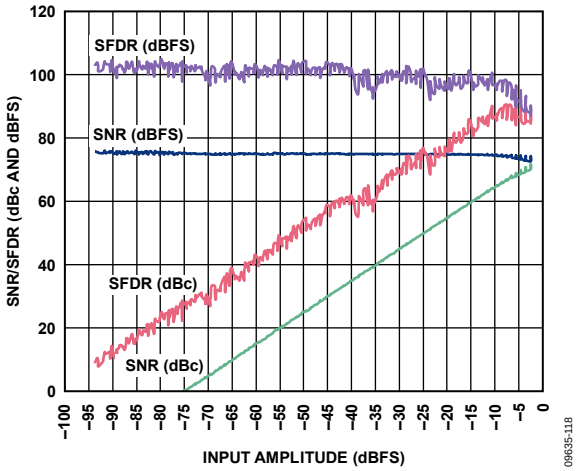


Figure 11. AD6649 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz

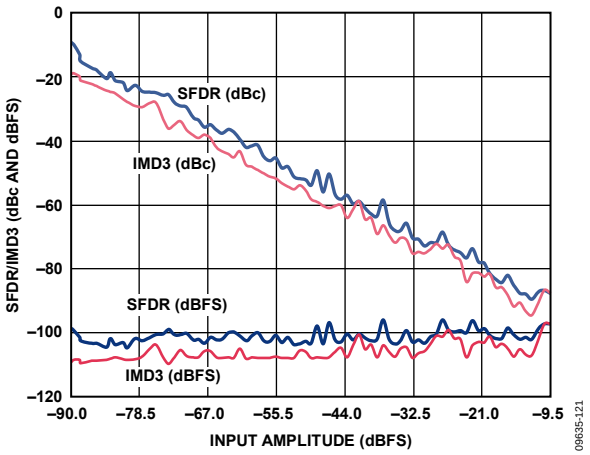


Figure 14. AD6649 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

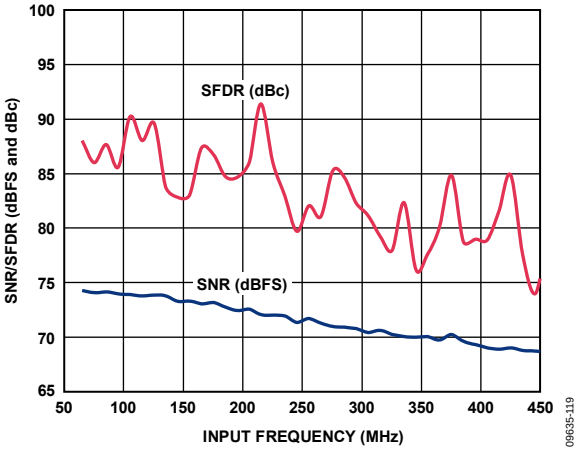


Figure 12. AD6649 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

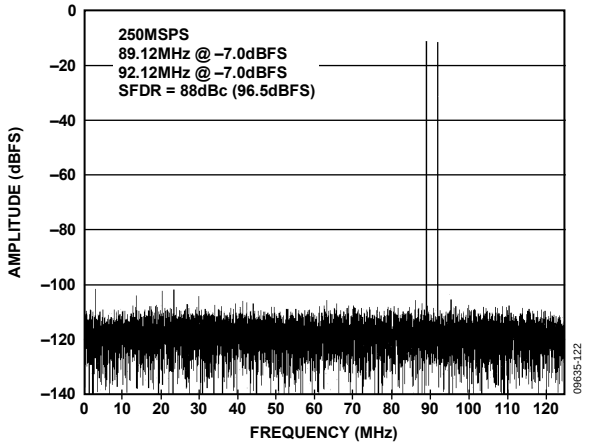


Figure 15. AD6649 Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

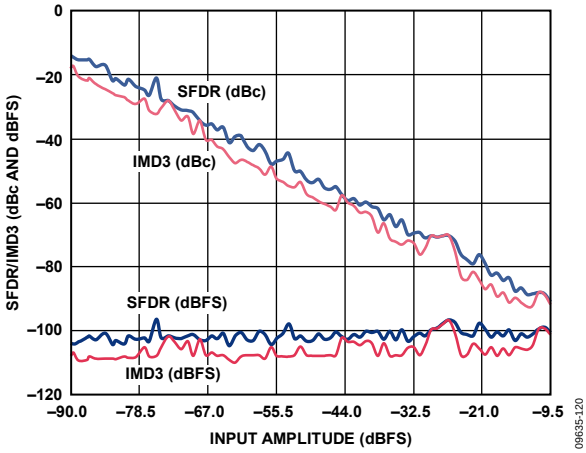


Figure 13. AD6649 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

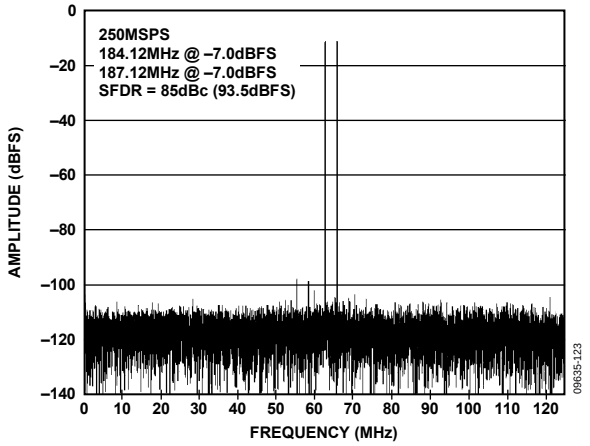


Figure 16. AD6649 Two-Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

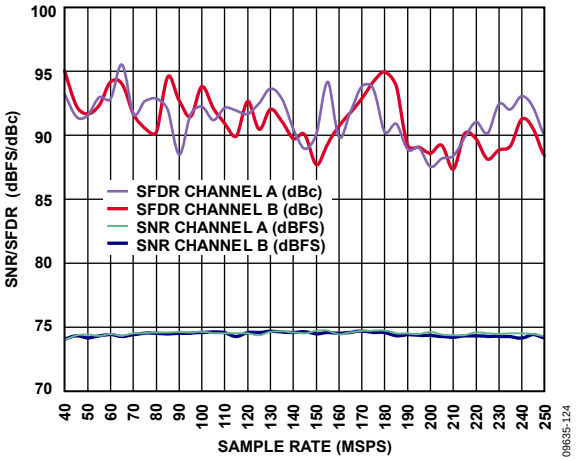


Figure 17. AD6649 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

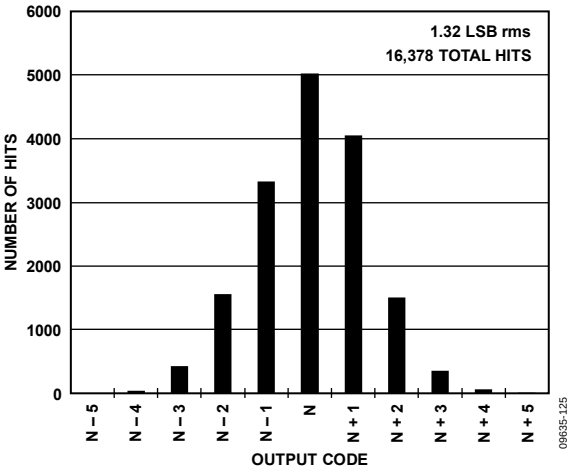


Figure 18. AD6649 Grounded Input Histogram

EQUIVALENT CIRCUITS

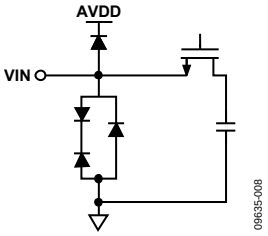


Figure 19. Equivalent Analog Input Circuit

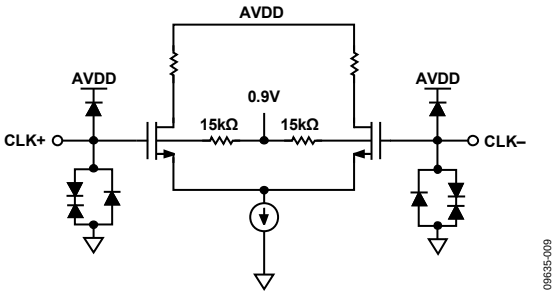


Figure 20. Equivalent Clock Input Circuit

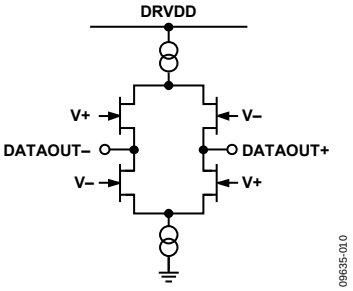


Figure 21. Equivalent LVDS Output Circuit

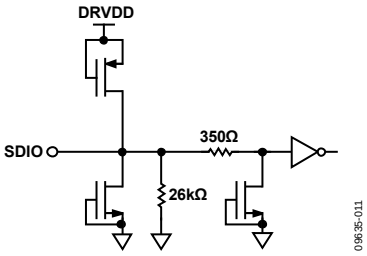


Figure 22. Equivalent SDIO Circuit

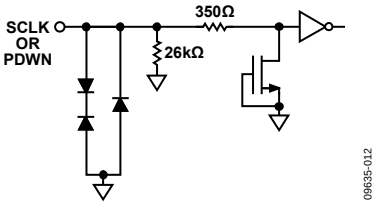


Figure 23. Equivalent SCLK or PDWN Input Circuit

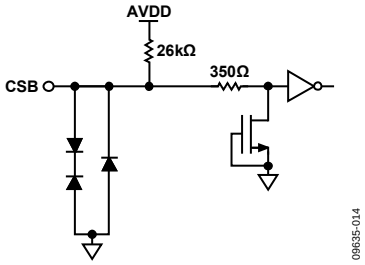


Figure 24. Equivalent CSB Input Circuit

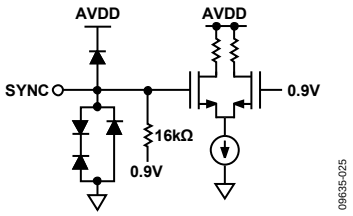


Figure 25. Equivalent SYNC Input Circuit

THEORY OF OPERATION

The AD6649 has two analog input channels, two filter channels, and two digital output channels. The intermediate frequency (IF) input signal passes through several stages before appearing at the output port(s) as a filtered and optionally decimated digital signal.

The dual ADC design can be used for diversity reception of signals, where the ADCs operate identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample frequencies from dc to 300 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 400 MHz analog input is permitted but occurs at the expense of increased ADC noise and distortion.

Synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD6649 are accomplished using a 3-pin SPI-compatible serial interface.

ADC ARCHITECTURE

The AD6649 architecture consists of a dual front-end sample-and-hold circuit, followed by a pipelined switched-capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6649 is a differential switched-capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see the configuration shown in Figure 26). When the input is switched into sample mode, the signal source must be capable of charging the sampling capacitors and settling within 1/2 clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, the shunt capacitors should be reduced. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject.

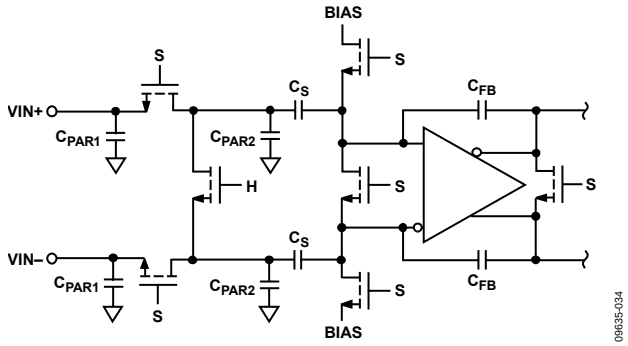


Figure 26. Switched-Capacitor Input

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched, and the inputs should be differentially balanced.

Input Common Mode

The analog inputs of the AD6649 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCM pin. Using the VCM output to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCM pin voltage (typically 0.5 × AVDD). The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section. This decoupling capacitor should be placed close to the pin to minimize the series resistance and inductance between the part and this capacitor.

Differential Input Configurations

Optimum performance is achieved while driving the AD6649 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, ADA4938-2, and ADA4930-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4930-2 is easily set with the VCM pin of the AD6649 (see Figure 27), and the driver can be configured in a Sallen-Key filter topology to provide band-limiting of the input signal.

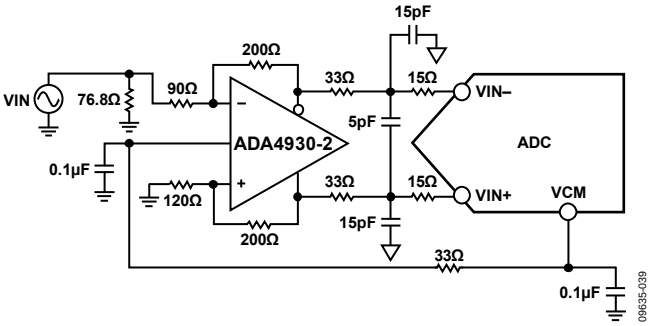


Figure 27. Differential Input Configuration Using the ADA4930-2

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 28. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

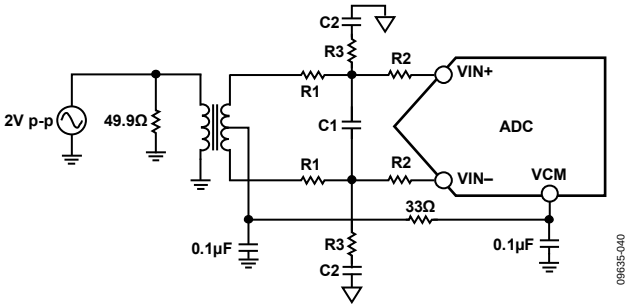


Figure 28. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz. Excessive signal power can also cause core saturation, which leads to distortion.

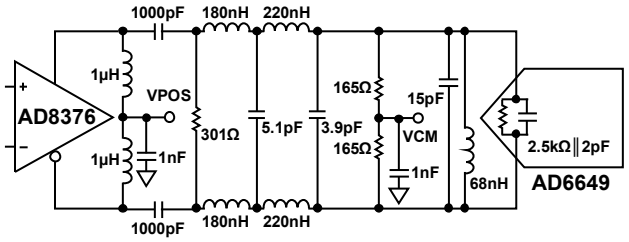
At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD6649. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 30). In this configuration, the input is ac-coupled and the CML is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 9 displays recommended values to set the RC network for different input frequency ranges. However, these values are dependent on the input signal and bandwidth and should be used only as a starting guide. Note that the values given in Table 9 are for each R1, R2, C2, and R3 component shown in Figure 28 and Figure 30.

Table 9. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	8.2	0	15	49.9
100 to 250	15	3.9	0	8.2	49.9

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use an amplifier with variable gain. The AD8375 or AD8376 digital variable gain amplifier (DVGAs) provides good performance for driving the AD6649. Figure 29 shows an example of the AD8376 driving the AD6649 through a band-pass antialiasing filter.



NOTES
1. ALL INDUCTORS ARE COILCRAFT® 0603CS COMPONENTS WITH THE EXCEPTION OF THE 1µH CHOKE INDUCTORS (COILCRAFT 0603LS).
2. FILTER VALUES SHOWN ARE FOR A 20MHz BANDWIDTH FILTER CENTERED AT 140MHz.

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Figure 29. Differential Input Configuration Using the AD8376

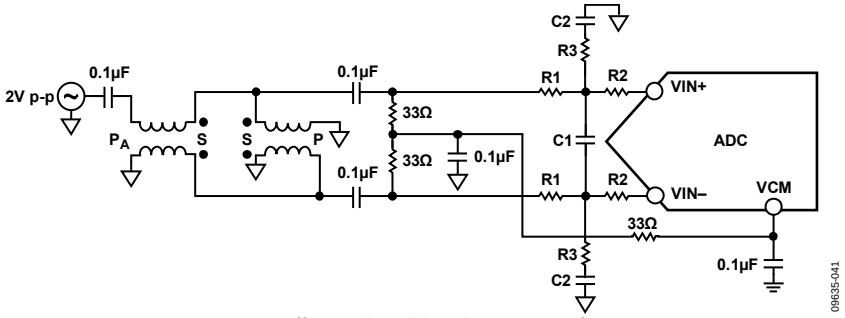


Figure 30. Differential Double Balun Input Configuration

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD6649. The full-scale input range can be adjusted by varying the reference voltage via SPI. The input span of the ADC tracks reference voltage changes linearly.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD6649 sample clock inputs, CLK+ and CLK−, should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or via capacitors. These pins are biased internally (see Figure 31) and require no external bias. If the inputs are floated, the CLK− pin is pulled low to prevent spurious clocking.

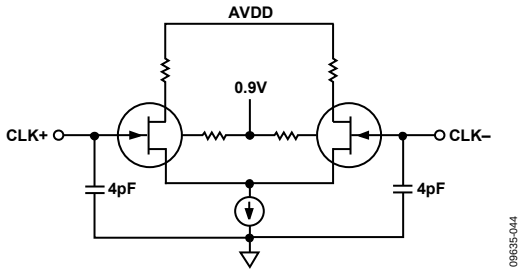


Figure 31. Simplified Equivalent Clock Input Circuit

Clock Input Options

The AD6649 has a very flexible clock input structure. Clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 32 and Figure 33 show two preferable methods for clocking the AD6649 (at clock rates of up to 625 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using an RF balun or RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD6649 to approximately 0.8 V p-p differential. This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD6649 while preserving the fast rise and fall times of the signal, which are critical to low jitter performance.

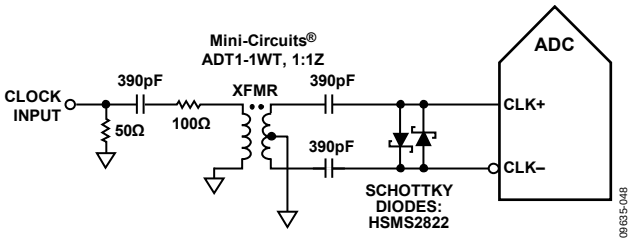


Figure 32. Transformer-Coupled Differential Clock (Up to 200 MHz)

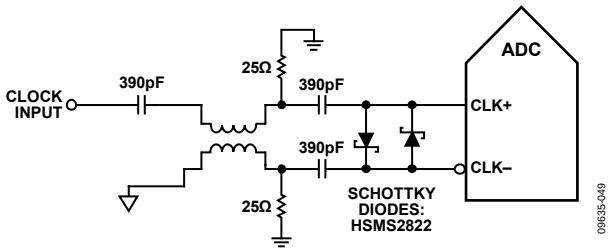


Figure 33. Balun-Coupled Differential Clock (Up to 625 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins as shown in Figure 34. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, AD9524, and ADCLK905/ADCLK907/ADCLK925 clock drivers offer excellent jitter performance.

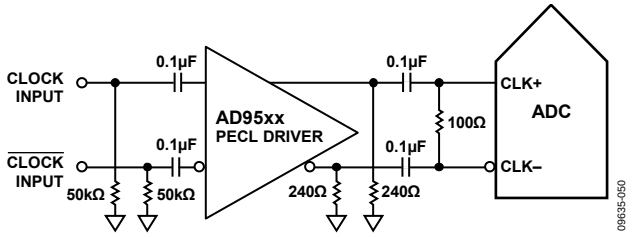


Figure 34. Differential PECL Sample Clock (Up to 625 MHz)

A third option is to ac-couple a differential LVDS signal to the sample clock input pins, as shown in Figure 35. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, and AD9524 clock drivers offer excellent jitter performance.

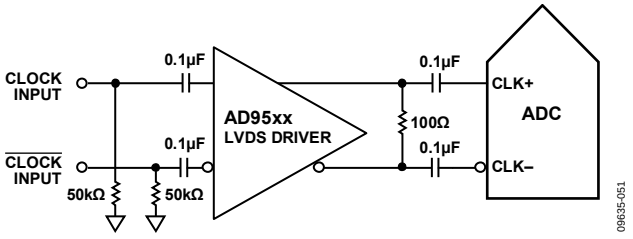


Figure 35. Differential LVDS Sample Clock (Up to 625 MHz)

Input Clock Divider

The AD6649 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. The duty cycle stabilizer (DCS) is enabled by default on power-up.

The AD6649 clock divider can be synchronized using the external SYNC input. Bit 1 and Bit 2 of Register 0x3A allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD6649 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD6649.

Jitter on the rising edge of the input clock is still of paramount concern and is not reduced by the duty cycle stabilizer. The duty cycle control loop does not function for clock rates less than 40 MHz nominally. The loop has a time constant associated with it that must be considered when the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time period that the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{IN}) due to jitter (t_J) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the root-mean-square of all jitter sources, which include the clock input, the analog input signal, and the ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as shown in Figure 36.

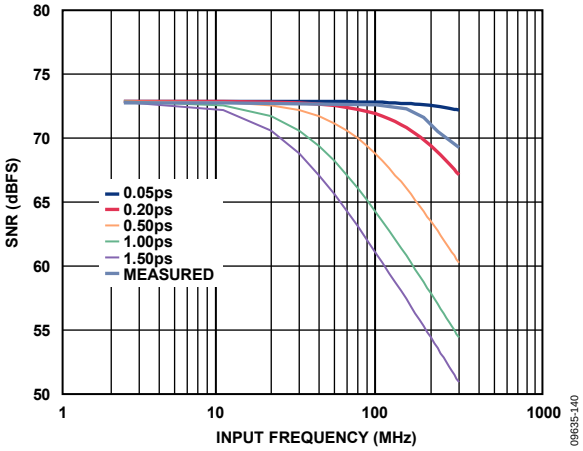


Figure 36. SNR (95 MHz BW) vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD6649. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 37, the power dissipated by the AD6649 is proportional to its sample rate. The data in Figure 37 was taken using the same operating conditions as those used for the Typical Performance Characteristics.

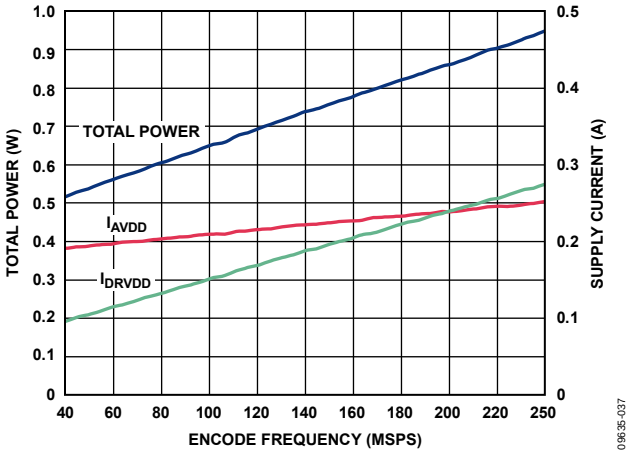


Figure 37. AD6649 Power and Current vs. Sample Rate

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD6649 is placed in power-down mode. In this state, the ADC typically dissipates 10 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD6649 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map Register Description section and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional details.

DIGITAL OUTPUTS

The AD6649 output drivers can be configured for either ANSI LVDS or reduced drive LVDS using a 1.8 V DRVDD supply.

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

Digital Output Enable Function (OEB)

The AD6649 has a flexible three-state ability for the digital output pins. The three-state mode is enabled using the OEB pin or through the SPI interface. If the OEB pin is low, the output data drivers are enabled. If the OEB pin is high, the output data drivers are placed in a high impedance state. This OEB function is not intended for rapid access to the data bus. Note that OEB is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

When using the SPI interface, the data and fast detect outputs of each channel can be independently three-stated by using the output enable bar bit (Bit 4) in Register 0x14. Because the output data is interleaved, if only one of the two channels is disabled, the data of the remaining channel is repeated in both the rising and falling output clock cycles.

Timing

The AD6649 provides latched data with a pipeline delay of 23 or 43 input sample clock cycles, depending on the mode of operation. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD6649. These transients can degrade converter dynamic performance.

The lowest typical conversion rate of the AD6649 is 40 MSPS. At clock rates below 40 MSPS, dynamic performance may degrade.

Data Clock Output (DCO)

The AD6649 also provides data clock output (DCO) intended for capturing the data in an external register. Figure 2 shows a graphical timing diagram of the AD6649 output modes.

Table 10. Output Data Format

Input (V)	VIN+ – VIN–, Input Span = 1.75 V p-p (V)	Offset Binary Output Mode	Twos Complement Mode (Default)	OR
VIN+ – VIN–	<–0.875	00 0000 0000 0000	10 0000 0000 0000	1
VIN+ – VIN–	–0.875	00 0000 0000 0000	10 0000 0000 0000	0
VIN+ – VIN–	0	10 0000 0000 0000	00 0000 0000 0000	0
VIN+ – VIN–	+0.875	11 1111 1111 1111	01 1111 1111 1111	0
VIN+ – VIN–	>+0.875	11 1111 1111 1111	01 1111 1111 1111	1

DIGITAL PROCESSING

The AD6649 includes a digital processing section that provides filtering. This digital processing section includes a numerically controlled oscillator (NCO), a selectable FIR filter (high performance or low latency), and a second coarse NCO ($f_S/4$ fixed value) for output frequency translation (complex to real). These blocks can be configured in several modes to implement a signal processing function. Refer to Figure 1 for the functional block diagram of the AD6649.

NUMERICALLY CONTROLLED OSCILLATOR (NCO)

Frequency translation is accomplished with an NCO shared between the two channels. Amplitude and phase dither can be enabled on chip to improve the noise and spurious performance of the NCO.

Because the filtering prevents usage of part of the Nyquist spectrum, a means is needed to translate the sampled input spectrum into the usable range of the decimation filter. To achieve this, a 32-bit, tuning, complex NCO is provided. This NCO/mixer allows the input spectrum to be tuned to dc, where it can be effectively filtered by the subsequent filter blocks to prevent aliasing.

When using the low latency FIR, the NCO must be tuned to $f_S/4$ (0x40000000). This prevents unwanted aliases from falling back into the band of interest.

NCO AND FIR FILTER MODES

The NCO and FIR blocks can be used in two modes depending on the bandwidth and latency requirement of the application. The two modes of operation of these blocks are summarized in Table 11.

Table 11. Signal Path Modes

Mode	FIR	Output Bandwidth at 245.76 MSPS
Fixed-Frequency NCO, 95 MHz FIR Filter	Low latency (default)	95 MHz
Tunable-Frequency NCO, 100 MHz FIR Filter	High performance	99.5 MHz

Two fixed-coefficient FIR filters provide filtering capability. A low latency FIR or a high performance FIR can be selected. It removes the negative frequency images to avoid aliasing negative frequencies for real outputs. Figure 38, Figure 39, and Figure 40 show the progression of a 95 MHz bandwidth signal through the filter stages when using the fixed-frequency NCO and 95 MHz FIR filter with a sample rate of 245.76 MSPS. The tunable-frequency NCO can be used instead and operates in a similar fashion. In these modes, the output is centered at 61.44 MHz, assuming a 245.76 MSPS sample rate.

$f_S/4$ FIXED-FREQUENCY NCO

A fixed-frequency $f_S/4$ NCO is provided to translate the filtered, decimated signal from dc to $f_S/4$ to allow a real output. The $f_S/4$ NCO is required in all operation modes because complex output from the part is not supported.

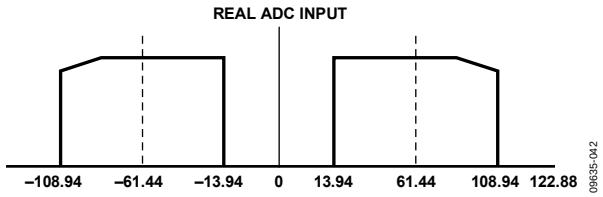


Figure 38. Example AD6649 Real 95 MHz Bandwidth Input Signal Centered at 61.44 MHz (f_{ADC} = 245.76 MHz)

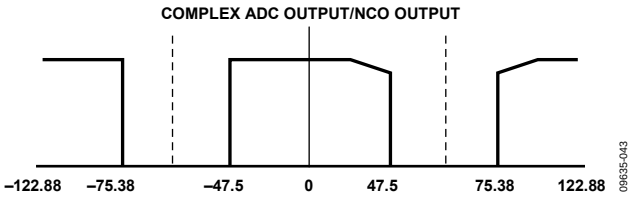


Figure 39. Example AD6649 95 MHz Bandwidth Input Signal Tuned to DC Using the NCO (NCO Frequency = 61.44 MHz)

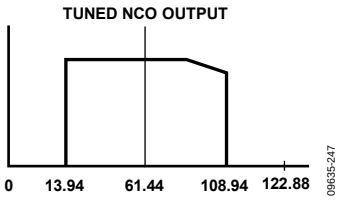


Figure 40. Example AD6649 95 MHz Bandwidth Output Signal Tuned to $f_S/4$ (NCO Frequency = 61.44 MHz)

NUMERICALLY CONTROLLED OSCILLATOR (NCO)

FREQUENCY TRANSLATION

This processing stage comprises a digital tuner consisting of a 32-bit complex numerically controlled oscillator (NCO). The NCO is always enabled. This NCO block accepts a real input from the ADC stage and outputs a frequency translated complex (I and Q) output.

The NCO frequency is programmed in Register 0x52 through Register 0x55. These four 8-bit registers make up a 32-bit unsigned frequency programming word. Frequencies between −CLK/2 and +CLK/2 are represented using the following frequency words:

- 0x80000000 represents a frequency given by −CLK/2.
- 0x00000000 represents dc (frequency = 0 Hz).
- 0x7FFFFFFF represents CLK/2 − CLK/2^{32}.

Use the following equation to calculate the NCO frequency:

$$NCO_FREQ = 2^{32} \times \frac{Mod(f, f_{CLK})}{f_{CLK}}$$

where:
NCO_FREQ is a 32-bit twos complement number representing the NCO frequency register.
f is the desired carrier frequency in hertz.
f_{CLK} is the AD6649 ADC clock rate in hertz.

NCO SYNCHRONIZATION

The AD6649 NCOs within a single part or across multiple parts can be synchronized using the external SYNC input. Bit 0 and Bit 1 of Register 0x58 allow the NCO to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the NCO to restart at the programmed phase offset value.

NCO AMPLITUDE AND PHASE DITHER

The NCO block contains amplitude and phase dither to improve the spurious performance. Amplitude dither improves performance by randomizing the amplitude quantization errors within the angular-to-Cartesian conversion of the NCO. This option reduces spurs at the expense of a slightly raised noise floor. With amplitude dither enabled, the NCO has an SNR of greater than 93 dB and an SFDR of greater than 115 dB. With amplitude dither disabled, the SNR is increased to greater than 96 dB at the cost of SFDR performance, which is reduced to 100 dB. The NCO amplitude and phase dither are recommended and can be enabled by setting Bit 1 and Bit 2 in Register 0x51.

FIR FILTERS

The two FIR filters that can be used are either a 47-tap, high performance, fixed-coefficient FIR filter or a 21-tap, low latency, fixed-coefficient FIR filter. These filters are useful in providing alias protection at the device output. The high performance FIR is a simple sum-of-products FIR filter with 47 filter taps and 21-bit fixed coefficients. Note that this filter does not decimate. The normalized coefficients used in the implementation and the decimal equivalent value of the coefficients are listed in Table 12.

Table 12. High Performance FIR Filter Coefficients

Coefficient Number	Normalized Coefficient	Decimal Coefficient (21-Bit)
C0, C46	−0.0001335	−140
C1, C45	−0.0009689	−1016
C2, C44	−0.0024185	−2536
C3, C43	−0.0019341	−2028
C4, C42	0.0023584	2473
C5, C41	0.0051260	5375
C6, C40	−0.0009680	−1015
C7, C39	−0.0086231	−9042
C8, C38	−0.0011368	−1192
C9, C37	0.0142097	14900
C10, C36	0.0064697	6784
C11, C35	−0.0207596	−21768
C12, C34	−0.0161047	−16887
C13, C33	0.0274601	28794
C14, C32	0.0310631	32572
C15, C31	−0.0348339	−36526
C16, C30	−0.0557785	−58488
C17, C29	0.0415993	43620
C18, C28	0.0986786	103472
C19, C27	−0.0463982	−48652
C20, C26	−0.1893501	−198548
C21, C25	0.0505829	53040
C22, C24	0.6113434	641040
C23	0.9171314	961682

FIR SYNCHRONIZATION

The AD6649 filters within a single part or across multiple parts can be synchronized using the external SYNC input. The filters can be configured to be resynchronized on every SYNC signal or only on the first SYNC signal after the SPI control register is written. A valid SYNC causes the FIR filter to restart at the programmed decimation phase value. Bit 4 and Bit 5 of Register 0x58 allow the FIR to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written.

FILTER PERFORMANCE

When using the fixed-frequency NCO and a 95 MHz FIR filter, the output rate is equal to the sample clock rate. The composite response of this mode is shown in Figure 41. The detailed pass-band response for this mode is shown in Figure 42. To place the part in this mode, set SPI Register 0x50 to 0xB0. When operating in this mode, the NCO must be placed at $f_S/4$, and the low latency NCO select bit (Bit 0) in Register 0x5A must be set. It is important to note that a −1.0 dBFS input level at the analog inputs corresponds to an output level of −2.5 dBFS when using the low latency FIR filter. This output level reduction is a result of the −1.5 dB pass-band attenuation in the FIR filter in this mode and does not result in loss in the dynamic range of the converter.

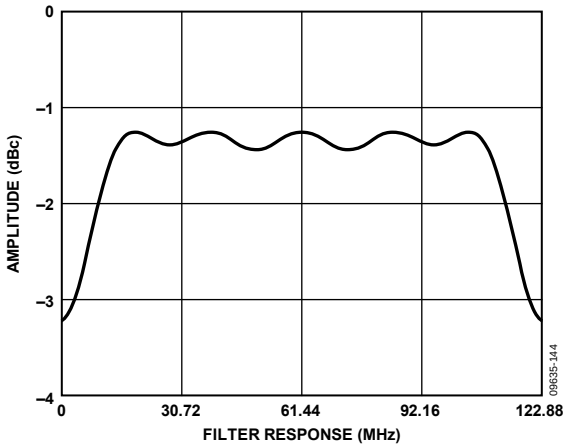


Figure 41. Low Latency FIR Filter Composite Response at 245.76 MSPS (Fixed-Frequency NCO, 95 MHz FIR Filter Mode)

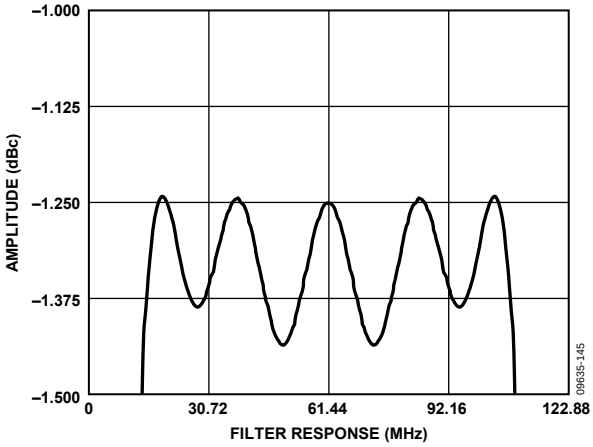


Figure 42. Low Latency FIR Filter Pass-Band Response at 245.76 MSPS (Fixed-Frequency NCO, 95 MHz FIR Filter Mode)

When using the tunable-frequency NCO and 100 MHz FIR filter, the output rate is equal to the sample clock rate. The response of the high performance FIR filter is shown in Figure 43. The detailed pass-band response for this mode is shown in Figure 44. To place the part into this mode, set SPI Register 0x50 to 0xA0. When using the high performance FIR filter, the output level is −1.3 dBFS for a corresponding input level of −1.0 dBFS at the analog inputs. This is a result of the −0.3 dB pass-band attenuation of the FIR filter in this mode and does not result in loss in the dynamic range of the converter.

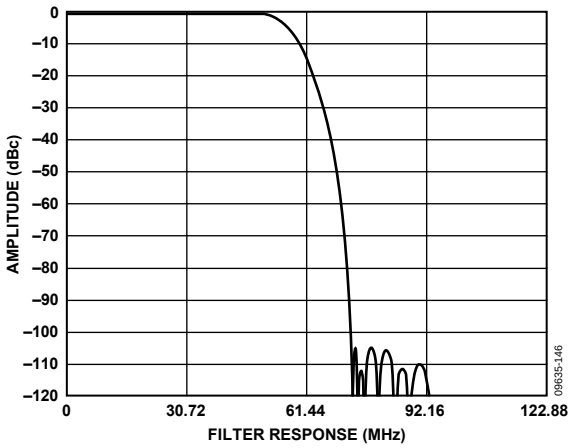


Figure 43. High Performance FIR Filter Pass-Band Response at 245.76 MSPS (Tunable-Frequency NCO, 100 MHz FIR Filter)

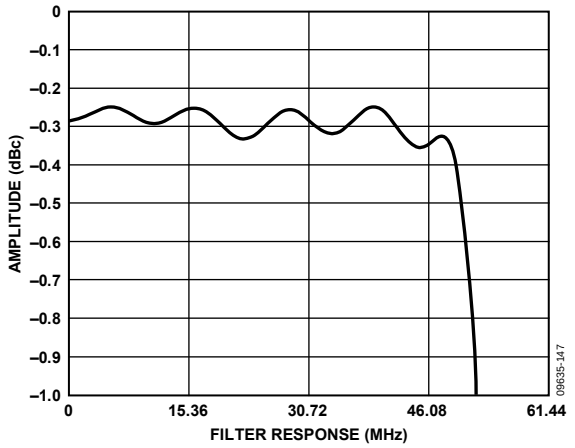


Figure 44. High Performance FIR Filter Pass-Band Response at 245.76 MSPS (Tunable-Frequency NCO, 100 MHz FIR Filter)

OUTPUT NCO

The output of the 32-bit fine-tuning NCO is complex and typically centered in frequency around dc. This complex output is carried through the stages of either the 95 MHz or 100 MHz FIR filter to provide proper antialiasing filtering. The final NCO provides a means to move this complex output signal away from dc so that a real output can be provided from the AD6649. The output NCO translates the output from dc to a frequency equal to the output frequency divided by 4 ($f_S/4$). This provides the user with an output signal centered at $f_S/4$ in frequency.

The AD6649 output NCOs within a single part or across multiple parts can be synchronized using the external SYNC input. Bit 7 and Bit 6 of Register 0x58 allow the output NCO to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written.

ADC OVERRANGE AND GAIN CONTROL

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overflow indicator provides delayed information on the state of the analog input that is of limited value in preventing clipping. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip occurs. In addition, because input signals can have significant slew rates, latency of this function is of concern.

Using the SPI port, the user can provide a threshold above which the FD output is active. Bit 0 of SPI Register 0x45 allows the user to select the threshold level. As long as the signal is below the selected threshold, the FD output remains low. In this mode, the magnitude of the data is considered in the calculation of the condition, but the sign of the data is not considered. The threshold detection responds identically to positive and negative signals outside the desired range (magnitude).

ADC OVERRANGE (OR)

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange condition is determined at the output of the ADC pipeline and, therefore, is subject to a latency of 7 ADC clock cycles. An overrange at the input is indicated by this bit 7 clock cycles after it occurs.

GAIN SWITCHING

The AD6649 includes circuitry that is useful in applications either where large dynamic ranges exist or where gain ranging amplifiers are employed. This circuitry allows digital thresholds to be set such that an upper threshold and a lower threshold can be programmed.

One such use is to detect when an ADC is about to reach full scale with a particular input condition. The result is to provide an indicator that can be used to quickly insert an attenuator that prevents ADC overdrive.

Fast Threshold Detection (FDA and FDB)

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold register, located in Register 0x47 and Register 0x48. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 4 clock cycles. The upper threshold magnitude is defined by the following equation:

$$\textit{Upper Threshold Magnitude}\ (\text{dBFS}) = 20\log(\textit{Threshold Magnitude}/2^{13})$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold register, located at Register 0x49 and Register 0x4A. The fast detect lower threshold register is a 15-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency but is accurate in terms of converter resolution. The lower threshold magnitude is defined by the following equation:

$$\textit{Lower Threshold Magnitude}\ (\text{dBFS}) = 20\log(\textit{Threshold Magnitude}/2^{13})$$

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time register, located in Register 0x4B and Register 0x4C.

The operation of the upper threshold and lower threshold registers, along with the dwell time, is shown in Figure 45.

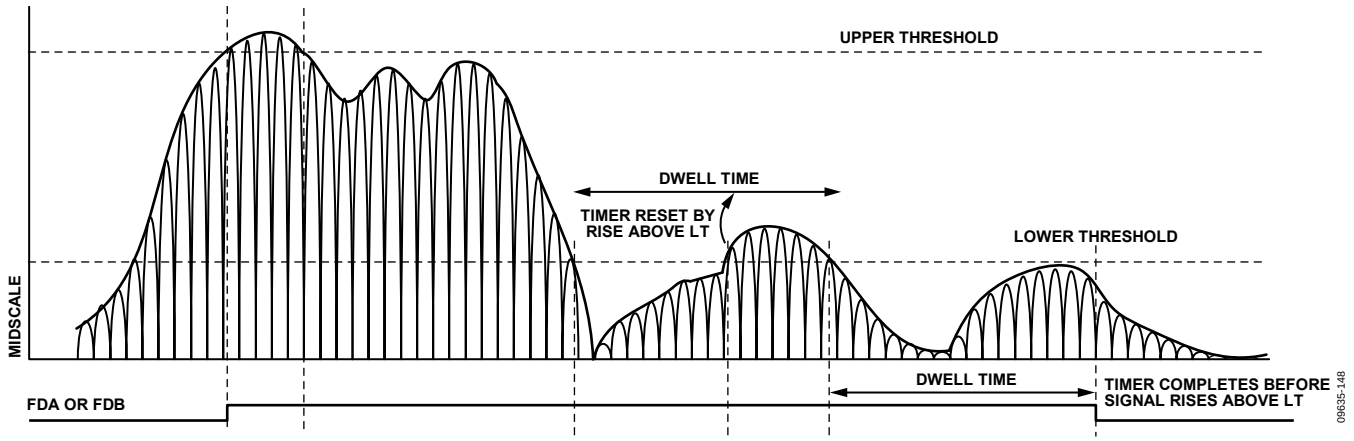


Figure 45. Threshold Settings for FDA and FDB Signals

DC CORRECTION

Because the dc offset of the ADC may be significantly larger than the signal being measured, a dc correction circuit is included to null the dc offset before measuring the power. The dc correction circuit can also be switched into the main signal path, but this may not be appropriate if the ADC is digitizing a time-varying signal with significant dc content, such as GSM.

DC Correction Bandwidth

The dc correction circuit is a high-pass filter with a programmable bandwidth (ranging between 0.29 Hz and 2.387 kHz at 245.76 MSPS). The bandwidth is controlled by writing the 4-bit dc correction bandwidth select register, located at Register 0x40, Bits[5:2]. The following equation can be used to compute the bandwidth value for the dc correction circuit:

$$DC_Corr_BW = 2^{-k-14} \times \frac{f_{CLK}}{2 \times \pi}$$

where:
k is the 4-bit value programmed in Bits[5:2] of Register 0x40 (values between 0 and 13 are valid for k; programming 14 or 15 provides the same result as programming 13).
f_{CLK} is the AD6649 ADC sample rate in hertz.

DC Correction Readback

The current dc correction value can be read back in Register 0x41 and Register 0x42 for each channel. The dc correction value is a 16-bit value that can span the entire input range of the ADC.

DC Correction Freeze

Setting Bit 6 of Register 0x40 freezes the DC correction at its current state and continues to use the last updated value as the dc correction value. Clearing this bit restarts dc correction and adds the currently calculated value to the data.

DC Correction Enable Bits

Setting Bit 1 of Register 0x40 enables dc correction for use in the output data signal path.

CHANNEL/CHIP SYNCHRONIZATION

The AD6649 has a SYNC input that allows the user flexible synchronization options for synchronizing the internal blocks. The SYNC feature is useful for guaranteeing synchronized operation across multiple ADCs. The input clock divider, NCO, FIR filters, and the output $f_S/4$ NCO can be synchronized using the SYNC input. Each of these blocks can be enabled to synchronize on a single occurrence of the SYNC signal or on every occurrence by setting the appropriate bits in Register 0x58.

The SYNC input is internally synchronized to the sample clock. However, to ensure that there is no timing uncertainty between multiple parts, the SYNC input signal should be synchronized to the input clock signal. The SYNC input should be driven using a single-ended CMOS type signal.

If Bit 1 in Register 0x59 is used, the SYNC input can be set to either level or edge sensitive mode. If the SYNC input is set to edge sensitive mode, Bit 0 of Register 0x59 can be used to determine whether the rising or falling edge is used.

SERIAL PORT INTERFACE (SPI)

The AD6649 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 13). The SCLK (serial clock) pin is used to synchronize the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 13. Serial Port Interface Pins

Pin	Function
SCLK	Serial Clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO	Serial Data Input/Output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip Select Bar. An active low control that gates the read and write cycles.

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 46 and Table 5.

Other modes involving the CSB are available. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 13 comprise the physical interface between the user programming device and the serial port of the AD6649. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD6649 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 14 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD6649 part-specific features are described in the Memory Map Register Description section.

Table 14. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS via the SPI
Offset	Allows the user to digitally adjust the converter offset
Test I/O	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set up outputs
Output Phase	Allows the user to set the output clock polarity
Output Delay	Allows the user to vary the DCO delay
VREF	Allows the user to set the reference voltage
Digital Processing	Allows the user to enable the NCOs, FIR filters, and synchronization features

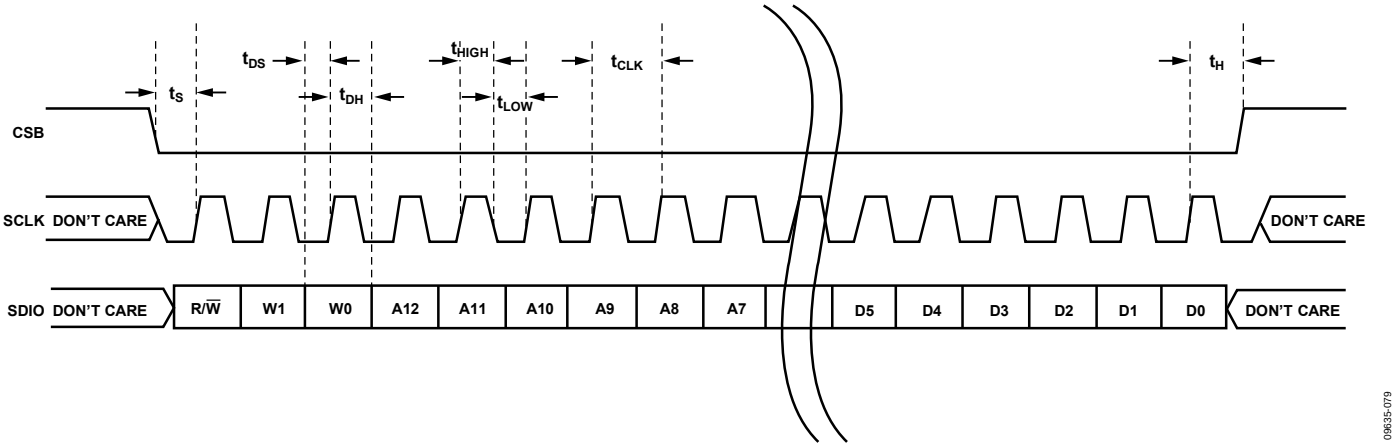


Figure 46. Serial Port Interface Timing Diagram

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into four sections: the chip configuration registers (Address 0x00 to Address 0x02); the channel index and transfer registers (Address 0x05 and Address 0xFF); the ADC functions registers, including setup, control, and test (Address 0x08 to Address 0x3A); and the digital feature control registers (Address 0x40 to Address 0x5A).

The memory map register table (see Table 15) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x14, the output mode register, has a hexadecimal default value of 0x05. This means that Bit 0 = 1 and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This document details the functions controlled by Register 0x00 to Register 0x25. The remaining registers, from Register 0x3A to Register 0x5A, are documented in the Memory Map Register Description section.

Open and Reserved Locations

All address and bit locations that are not included in Table 15 are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open (for example, Address 0x13), this address location should not be written.

Default Values

After the AD6649 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 15.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Address 0x08 to Address 0x20, Address 0x3A, Address 0x40 to Address 0x42, Address 0x45 to 0x4C, and Address 0x50 to Address 0x5A are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and then the bit autoclears.

Channel-Specific Registers

Some channel setup functions, such as the signal monitor thresholds, can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 15 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x05. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, only Channel A or Channel B should be set to read one of the two registers. If both bits are set during an SPI read cycle, the part returns the value for Channel A. Registers and bits designated as global in Table 15 affect the entire part and the channel features for which independent settings are not allowed between channels. The settings in Register 0x05 do not affect the global registers and bits.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 15 are not currently supported for this device.

Table 15. Memory Map Registers

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
0x00	SPI port configuration (global)[1]	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	The nibbles are mirrored so that LSB first mode or MSB first mode registers correctly, regardless of shift mode.
0x01	Chip ID (global)	8-bit chip ID[7:0] (AD6649 = 0xA1) (default)								0xA1	Read only.
0x02	Chip grade (global)	Open	Open	Speed grade ID 00 = 250 MSPS		Open	Open	Open	Open		Speed grade ID used to differentiate devices; read only.
Channel Index and Transfer Registers											
0x05	Channel index (global)	Open	Open	Open	Open	Open	Open	ADC B (default)	ADC A (default)	0x03	Bits are set to determine which device on the chip receives the next write command; applies to local registers only.
0xFF	Transfer (global)	Open	Open	Open	Open	Open	Open	Open	Transfer	0x00	Synchronously transfers data from the master shift register to the slave.
ADC Functions											
0x08	Power modes (local)	Open	Open	External power-down pin function (local) 0 = power-down 1 = standby	Open	Open	Open	Internal power-down mode (local) 00 = normal operation 01 = full power-down 10 = standby 11 = reserved		0x00	Determines various generic modes of chip operation.
0x09	Global clock (global)	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilizer (default)	0x01	
0x0B	Clock divide (global)	Open	Open	Input clock divider phase adjust 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles 011 = 3 input clock cycles 100 = 4 input clock cycles 101 = 5 input clock cycles 110 = 6 input clock cycles 111 = 7 input clock cycles			Clock divide ratio 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	Clock divide values other than 000 automatically cause the duty cycle stabilizer to become active.

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x0D	Test mode (local)	User test mode control 0 = continuous/ repeat pattern 1 = single pattern, then 0s	Open	Reset PN long gen	Reset PN short gen	Output test mode 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN long sequence 0110 = PN short sequence 0111 = one/zero word toggle 1000 = user test mode 1001 to 1110 = unused 1111 = ramp output				0x00	When this register is set, the test data is placed on the output pins in place of normal data.
0x0E	BIST enable (local)	Open	Open	Open	Open	Open	Reset BIST sequence	Open	BIST enable	0x00	
0x10	Offset adjust (local)	Open	Open	Offset adjust in LSBs from +31 to −32 (twos complement format)						0x00	
0x14	Output mode	Open	Open	Open	Output enable bar (local)	Open	Output invert (local) 1 = normal (default) 0 = inverted	Output format 00 = offset binary 01 = twos complement (default) 10 = gray code 11 = reserved (local)		0x05	Configures the outputs and the format of the data.
0x15	Output adjust (global)	Open	Open	Open	Open	LVDS output drive current adjust 0000 = 3.72 mA output drive current 0001 = 3.5 mA output drive current (default) 0010 = 3.30 mA output drive current 0011 = 2.96 mA output drive current 0100 = 2.82 mA output drive current 0101 = 2.57 mA output drive current 0110 = 2.27 mA output drive current 0111 = 2.0 mA output drive current (reduced range) 1000 to 1111 = reserved				0x01	
0x16	Clock phase control (global)	Invert DCO clock	Open	Open	Open	Open	Open	Open	Open	0x00	
0x17	DCO output delay (global)	Enable DCO clock delay	Open	Open	DCO clock delay [delay = (3100 ps × register value/31 +100)] 00000 = 100 ps 00001 = 200 ps 00010 = 300 ps … 11110 = 3100 ps 11111 = 3200 ps					0x00	
0x18	Input span select (global)	Open	Open	Open	Full-scale input voltage selection 01111 = 2.087 V p-p … 00001 = 1.772 V p-p 00000 = 1.75 V p-p (default) 11111 = 1.727 V p-p … 10000 = 1.383 V p-p					0x00	Full-scale input adjustment in 0.022 V steps.
0x19	User Test Pattern 1 LSB (global)	User Test Pattern 1[7:0]								0x00	
0x1A	User Test Pattern 1 MSB (global)	User Test Pattern 1[15:8]								0x00	
0x1B	User Test Pattern 2 LSB (global)	User Test Pattern 2[7:0]								0x00	
0x1C	User Test Pattern 2 MSB (global)	User Test Pattern 2[15:8]								0x00	
0x1D	User Test Pattern 3 LSB (global)	User Test Pattern 3[7:0]								0x00	
0x1E	User Test Pattern 3 MSB (global)	User Test Pattern 3[15:8]								0x00	

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x1F	User Test Pattern 4 LSB (global)	User Test Pattern 4[7:0]								0x00	
0x20	User Test Pattern 4 MSB (global)	User Test Pattern 4[15:8]								0x00	
0x24	BIST signature LSB (local)	BIST signature[7:0]								0x00	Read only.
0x25	BIST signature MSB (local)	BIST signature[15:8]								0x00	Read only.
0x3A	Sync control (global)	Open	Open	Open	Open	Open	Clock divider next sync only	Clock divider sync enable	Master sync buffer enable	0x00	
Digital Feature Control Registers											
0x40	DC correction control (local)	Open	DC correction freeze	DC correction bandwidth select 0000 = 2387.32 Hz 0001 = 1193.66 Hz 0010 = 596.83 Hz 0011 = 298.42 Hz 0100 = 149.21 Hz 0101 = 74.60 Hz 0110 = 37.30 Hz 0111 = 18.65 Hz 1000 = 9.33 Hz 1001 = 4.66 Hz 1010 = 2.33 Hz 1011 = 1.17 Hz 1100 = 0.58 Hz 1101 = 0.29 Hz 1110 = reserved 1111 = reserved			DC correction enable	Open	0x00	
0x41	DC Correction Value 0 (local)	DC correction value[7:0]									Read only.
0x42	DC Correction Value 1 (local)	DC correction value[15:8]									Read only.
0x45	Fast detect control (local)	Open	Open	Open	Open	Force FD output enable	Force FD output value	Reserved	Enable fast detect output	0x00	
0x47	Fast Detect Upper Threshold 0 (local)	Fast detect upper threshold[7:0]								0x00	
0x48	Fast Detect Upper Threshold 1 (local)	Open	Open	Open	Fast detect upper threshold[12:8]					0x00	
0x49	Fast Detect Lower Threshold 0 (local)	Fast detect lower threshold[7:0]								0x00	
0x4A	Fast Detect Lower Threshold 1 (local)	Open	Open	Open	Fast detect lower threshold[12:8]					0x00	
0x4B	Fast Detect Dwell Time 0 (local)	Fast detect dwell time[7:0]								0x00	
0x4C	Fast Detect Dwell Time 1 (local)	Fast detect dwell time[15:8]								0x00	
0x50	Filter control (local)	1	Reserved	1	FIR mode 0 = high perfor-mance 1 = low latency	Output gain 0 = 0 dB 1 = −6 dB	9-bit output mode enable	Datapath gain 00 = 0 dB 01 = −6 dB 10 = −12 dB 11 = −18 dB		0xB0	

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x51	NCO control (local)	Reserved	NCO32 to $f_S/4$ NCO sync enable	Spectral reversal	1	Reserved	NCO32 amplitude dither enable	NCO32 phase dither enable	1	0x51	
0x52	NCO Frequency 3 (local)	NCO frequency value[31:24]								0x40	
0x53	NCO Frequency 2 (local)	NCO frequency value[23:16]								0x00	
0x54	NCO Frequency 1 (local)	NCO frequency value[15:8]								0x00	
0x55	NCO Frequency 0 (local)	NCO frequency value[7:0]								0x00	
0x56	NCO Phase Offset 1 (local)	NCO phase value[15:8]								0x00	
0x57	NCO Phase Offset 0 (local)	NCO phase value[7:0]								0x00	
0x58	Sync control (local)	$f_S/4$ NCO next sync only	$f_S/4$ NCO sync enable	FIR next sync only	FIR Sync Enable	Reserved	Reserved	NCO32 next sync only	NCO32 sync enable	0x00	
0x59	Sync pin control (local)	Open	Open	Open	Open	Open	Open	SYNC pin sensitivity 0 = sync on high level 1 = sync on edge	SYNC pin edge sensitivity 0 = sync on falling edge 1 = sync on rising edge	0x00	
0x5A	NCO Control 2 (local)	Open	Open	Open	Open	Open	Open	Open	Low latency NCO select	0x01	

[1] The channel index register at Address 0x05 should be set to 0x03 (default) when writing to Address 0x00.

MEMORY MAP REGISTER DESCRIPTION

For more information on functions controlled in Register 0x00 to Register 0x25, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Sync Control (Register 0x3A)

Bits[7:3]—Reserved

Bit 2—Clock Divider Next Sync Only

If the master sync buffer enable bit (Address 0x3A, Bit 0) and the clock divider sync enable bit (Address 0x3A, Bit 1) are high, Bit 2 allows the clock divider to sync to the first sync pulse that it receives and to ignore the rest. The clock divider sync enable bit (Address 0x3A, Bit 1) resets after it syncs.

Bit 1—Clock Divider Sync Enable

Bit 1 gates the sync pulse to the clock divider. The sync signal is enabled when Bit 1 is high and Bit 0 is high. This is continuous sync mode.

Bit 0—Master Sync Buffer Enable

Bit 0 must be set high to enable any of the sync functions. If the sync capability is not used, this bit should remain low to conserve power.

DC Correction Control (Register 0x40)

Bit 7—Reserved

Bit 6—DC Correction Freeze

When Bit 6 is set high, the dc correction is no longer updated to the signal monitor block, which holds the last dc value calculated.

Bits[5:2]—DC Correction Bandwidth Select

Bits[5:2] set the averaging time of the signal monitor dc correction function. This 4-bit word sets the bandwidth of the correction block, according to the following equation:

$$DC_Corr_BW = 2^{-k-14} \times \frac{f_{CLK}}{2 \times \pi}$$

where:
k is the 4-bit value programmed in Bits[5:2] of Register 0x40 (values between 0 and 13 are valid for k; programming 14 or 15 provides the same result as programming 13).
f_{CLK} is the AD6649 ADC sample rate in hertz.

Bit 1—DC Correction Enable

Setting this bit high causes the output of the dc measurement block to be summed with the data in the signal path to remove the dc offset from the signal path.

Bit 0—Reserved

Fast Detect Control (Register 0x45)

Bits[7:4]—Reserved

Bit 3—Force FD Output Enable

Setting this bit high forces the FD output pin to the value written to Bit 2 of this register (Register 0x45). This enables the user to force a known value on the FD pin for debugging.

Bit 2—Force FD Output Value

The value written to Bit 2 is forced on the FD output pin when Bit 3 is written high.

Bit 1—Reserved

Bit 0—Enable Fast Detect Output

Setting this bit high enables the output of the upper threshold FD comparator to drive the FD output pin.

Fast Detect Upper Threshold (Register 0x47 and Register 0x48)

Register 0x48, Bits[7:5]—Reserved

Register 0x48, Bits[4:0]—Fast Detect Upper Threshold[12:8]

Register 0x47, Bits[7:0]—Fast Detect Upper Threshold[7:0]

These registers provide an upper limit threshold. The 13-bit value is compared with the output magnitude from the ADC block. If the ADC magnitude exceeds this threshold value, the FD output pin is set if Bit 0 in Register 0x45 is set.

Fast Detect Lower Threshold (Register 0x49 and Register 0x4A)

Register 0x4A, Bits[7:5]—Reserved

Register 0x4A, Bits[4:0]—Fast Detect Lower Threshold[12:8]

Register 0x49, Bits[7:0]—Fast Detect Lower Threshold[7:0]

These registers provide a lower limit threshold. The 13-bit value is compared with the output magnitude from the ADC block. If the ADC magnitude is less than this threshold value for the number of cycles programmed in the dwell time register, the FD output bit is cleared.

Fast Detect Dwell Time (Register 0x4B and Register 0x4C)

Register 0x4C, Bits[7:0]—Fast Detect Dwell Time[15:8]

Register 0x4B, Bits[7:0]—Fast Detect Dwell Time[7:0]

These register values set the minimum time in ADC sample clock cycles (after clock divider) that a signal needs to stay below the lower threshold limit before the FD output bits are cleared.

Filter Control (Register 0x50)

Bit 7—Reserved (Reads Back as 1)

Bit 6—Reserved

Bit 5—Reserved (Reads Back as 1)

Bit 4—FIR Mode

Setting this bit low enables the high performance FIR filter. Setting this bit high enables the low latency FIR.

Bit 3—Output Gain

Setting this bit high sets the output gain to −6 dB. A 0 value on this bit sets the gain at 0 dB.

Bit 2—9-bit Output Mode Enable

If this bit is set, the NCOs and filters are bypassed and the part outputs nine bits of data. These nine bits are presented on the nine MSBs of the output bus (that is, Bit D13 through Bit D5).

Bits[1:0]—Datapath Gain

These bits set the datapath gain as follows:

00 = 0 dB gain

01 = −6 dB gain

10 = −12 dB gain

11 = −18 dB gain

NCO Control (Register 0x51)

Bit 7—Reserved

Bit 6—NCO32 to $f_S/4$ NCO Sync Enable

This bit should be set high when NCO32 is set to $f_S/4$ using the fixed-frequency NCO and the 95 MHz FIR filter. It should be disabled when using the tunable-frequency NCO and 100 MHz FIR filter.

Bit 5—Spectral Reversal

This bit should be set high to reverse the output frequency spectrum.

Bit 4—Reserved (Reads Back as 1)

Bit 3—Reserved

Bit 2—NCO32 Amplitude Dither Enable

When Bit 2 is set, amplitude dither in the NCO is enabled. When Bit 2 is cleared, amplitude dither is disabled.

Bit 1—NCO32 Phase Dither Enable

When Bit 2 is set, phase dither in the NCO is enabled. When Bit 2 is cleared, phase dither is disabled.

Bit 0—Reserved (Reads Back as 1)

NCO Frequency (Register 0x52 to Register 0x55)

Register 0x52, Bits[7:0]—NCO Frequency Value[31:24]

Register 0x53, Bits[7:0]—NCO Frequency Value[23:16]

Register 0x54, Bits[7:0]—NCO Frequency Value[15:8]

Register 0x55, Bits[7:0]—NCO Frequency Value[7:0]

This 32-bit value is used to program the NCO tuning frequency. The frequency value to be programmed is given by the following equation:

$$NCO_FREQ = 2^{32} \times \frac{Mod(f, f_{CLK})}{f_{CLK}}$$

where:
NCO_FREQ is a 32-bit twos complement number representing the NCO frequency register.
f is the desired carrier frequency in hertz.
f_{CLK} is the AD6649 ADC clock rate in hertz.

NCO Phase Offset (Register 0x56 and Register 0x57)

Register 0x56, Bits[7:0]—NCO Phase Value[15:8]

Register 0x57, Bits[7:0]—NCO Phase Value[7:0]

The 16-bit value programmed into the NCO phase value register is loaded into the NCO block each time the NCO is started or when an NCO SYNC signal is received. This process allows the NCO to be started with a known nonzero phase.

Use the following equation to calculate the NCO phase offset value:

$$NCO_PHASE = 2^{16} \times PHASE/360$$

where *NCO_PHASE* is a decimal number equal to the 16-bit binary number to be programmed at Register 0x56 and Register 0x57, and *PHASE* is the desired NCO phase in degrees.

SYNC Control (Register 0x58)

Bit 7—$f_S/4$ NCO Next Sync Only

If the master sync buffer enable bit (Register 0x3A, Bit 0) and the $f_S/4$ NCO sync enable bit (Register 0x58, Bit 6) are high, Bit 7 allows the $f_S/4$ NCO to synchronize following the first sync pulse that it receives and ignore the rest. If Bit 7 is set, Bit 6 of Register 0x58 resets after this sync occurs.

Bit 6—$f_S/4$ NCO Sync Enable

Bit 6 gates the sync pulse to the $f_S/4$ NCO. When Bit 6 is set high, the sync signal causes the $f_S/4$ NCO to synchronize. This sync is active only when the master sync buffer enable bit (Register 0x3A, Bit 0) is high. This is continuous sync mode.

Bit 5—FIR Next Sync Only

If the master sync buffer enable bit (Register 0x3A, Bit 0) and the FIR sync enable bit (Register 0x58, Bit 4) are high, Bit 5 allows the FIR to synchronize following the first sync pulse that it receives and to ignore the rest. If Bit 5 is set, Bit 4 of Register 0x3A resets after this sync occurs.

Bit 4—FIR Sync Enable

Bit 4 gates the sync pulse to the FIR filter. When Bit 4 is set high, the sync signal causes the half-band to resynchronize. This sync is active only when the master sync buffer enable bit (Register 0x3A, Bit 0) is high. This is continuous sync mode.

Bits[3:2]—Reserved

Bit 1—NCO32 Next Sync Only

If the master sync buffer enable bit (Register 0x3A, Bit 0) and the NCO32 sync enable bit (Register 0x58, Bit 0) are high, Bit 1 allows the NCO32 to synchronize following the first sync pulse that it receives and to ignore the rest. Bit 0 of Register 0x58 resets after a sync occurs if Bit 1 is set.

Bit 0—NCO32 Sync Enable

Bit 0 gates the sync pulse to the 32-bit NCO. When this bit is set high, the sync signal causes the NCO to resynchronize, starting at the NCO phase offset value. This sync is active only when the master sync buffer enable bit (Register 0x3A, Bit 0) is high. This is continuous sync mode.

SYNC Pin Control (Register 0x59)

Bits[7:2]—Reserved

Bit 1—SYNC Pin Sensitivity

If Bit 1 is set to a 0, the SYNC input responds to a level. If this bit is set low, the SYNC input responds to the edge (rising or falling) set in Bit 0 of Address 0x59.

Bit 0—SYNC Pin Edge Sensitivity

If Bit 1 is set high, setting Bit 0 to a 0 causes the SYNC input to respond to a falling edge. If this bit is set, the SYNC input respond to a rising edge.

NCO Control 2 (Register 0x5A)

Bits[7:1]—Reserved

Bit 0—Low Latency NCO Select

If Bit 0 is set to a 1, the low latency NCO is selected. This bit should be selected for the fixed-frequency NCO, 95 MHz FIR filter mode of operation. When this bit is set, the NCO value must be set to either 0x40000000 or 0xC0000000.

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting system level design and layout of the AD6649, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements needed for certain pins.

Power and Ground Recommendations

When connecting power to the AD6649, it is recommended that two separate 1.8 V supplies be used: one supply should be used for analog (AVDD), and a separate supply should be used for the digital outputs (DRVDD). The designer can employ several different decoupling capacitors to cover both high and low frequencies. These capacitors should be located close to the point of entry at the PC board level and close to the pins of the part with minimal trace length.

A single PCB ground plane should be sufficient when using the AD6649. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. A continuous, exposed (no solder mask) copper plane on the PCB should mate to the AD6649 exposed paddle, Pin 0.

The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be filled or plugged with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and the PCB, a silkscreen should be overlaid to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. See the evaluation board for a PCB layout example. For detailed information about packaging and PCB layout of chip scale packages, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

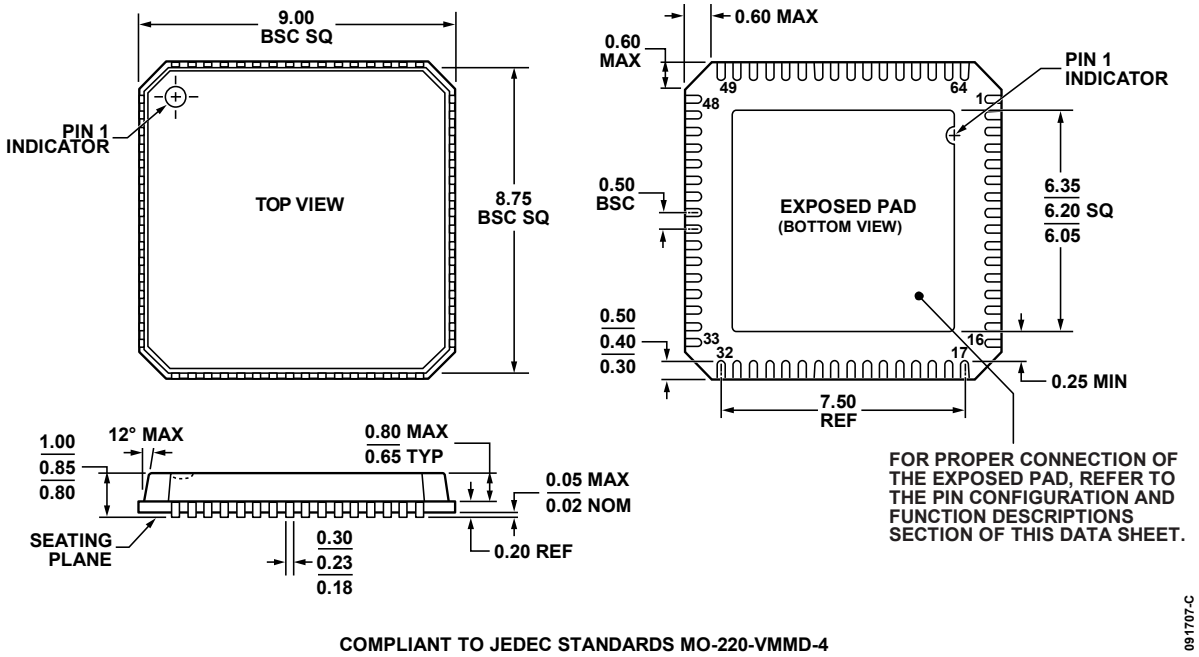
VCM

The VCM pin should be decoupled to ground with a 0.1 μF capacitor, as shown in Figure 28. For optimal channel-to-channel isolation, a 33 Ω resistor should be included between the AD6649 VCM pin and the Channel A analog input network connection and between the AD6649 VCM pin and the Channel B analog input network connection.

SPI Port

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD6649 to keep these signals from transitioning at the converter inputs during critical sampling periods.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 47. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD6649BCPZ	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-4
AD6649BCPZRL7	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-4
AD6649EBZ		Evaluation Board with AD6649	

[1] Z = RoHS Compliant Part.

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