

8A, 60V, 0.300 Ohm, P-Channel Power MOSFETs

These are P-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFD8P06E, RFD8P06ESM and RFP8P06E incorporate ESD protection and are designed to withstand 2kV (Human Body Model) of ESD.

Formerly developmental type TA49044.

Ordering Information

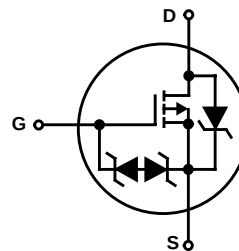
PART NUMBER	PACKAGE	BRAND
RFP8P06E	TO-220AB	RFP8P06E
RFD8P06ESM	TO-252AA	D8P06E
RFD8P06E	TO-251AA	D8P06E

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e. RFD8P06ESM9A.

Features

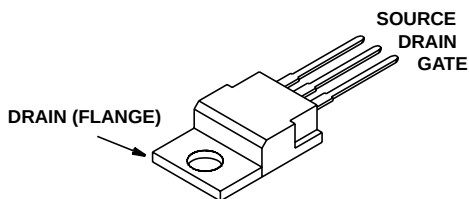
- 8A, 60V
- $r_{DS(ON)} = 0.300\Omega$
- Temperature Compensating PSPICE® Model
- 2kV ESD Protected
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

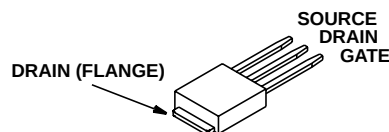


Packaging

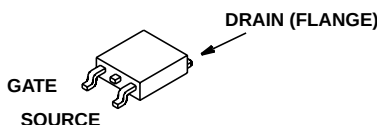
JEDEC TO-220AB



JEDEC TO-251AA



JEDEC TO-252AA



Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$

	RFD8P06E, RFD8P06ESM, RFP8P06E	UNITS
Drain to Source Voltage (Note 1)	V_{DSS} -60	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR} -60	V
Gate to Source Voltage	V_{GS} ± 20	V
Continuous Drain Current	I_D 8	A
Pulsed Drain Current (Note 3)	I_{DM} Refer to Peak Current Curve	A
Single Pulse Avalanche Rating (Note 4)	E_{AS} Refer to UIS Curve	
Power Dissipation	P_D 48	W
Linear Derating Factor	0.32	W/ $^{\circ}\text{C}$
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD 2	kV
Operating and Storage Temperature	T_J, T_{STG} -55 to 175	$^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L 300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg} 260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V		-60	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V		-	-	-1.0	μA
		V _{DS} = 0.8 x Rated BV _{DSS} , T _C = 150 ⁰ C		-	-	-25	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V		-	-	±10	μA
Drain to Source On Resistance (Note 3)	r _{DS(ON)}	I _D = 8A, V _{GS} = -10V		-	-	0.300	Ω
Turn-On Time	t _{ON}	V _{DD} = -30V, I _D ≈ 8A, R _L = 3.75Ω, V _{GS} = -10V, R _G = 2.5Ω (Figure 13)		-	-	70	ns
Turn-On Delay Time	t _{d(ON)}			-	15	-	ns
Rise Time	t _r			-	30	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	40	-	ns
Fall Time	t _f			-	25	-	ns
Turn-Off Time	t _{OFF}			-	-	100	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0 to -20V	V _{DD} = -48V, I _D = 8A, R _L = 6Ω I _{g(REF)} = -1.45mA	-	30	36	nC
Gate Charge at 5V	Q _{g(-10)}	V _{GS} = 0 to -10V		-	15	18	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0 to -2V		-	1.15	1.5	nC
Input Capacitance	C _{ISS}	V _{DS} = -25V, V _{GS} = 0V, f = 1MHz		-	600	-	pF
Output Capacitance	C _{OSS}			-	160	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	35	-	pF
Thermal Resistance Junction to Case	R _{θJC}	Figure 12		-	-	3.125	⁰ C/W
Thermal Resistance Junction to Ambient	R _{θJA}	TO-220		-	-	62	⁰ C/W
		TO-251, TO-252		-	-	100	⁰ C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = -8\text{A}$	-	-	-1.5	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = -8\text{A}, dI_{SD}/dt = -100\text{A}/\mu\text{s}$	-	-	125	ns

NOTES:

2. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

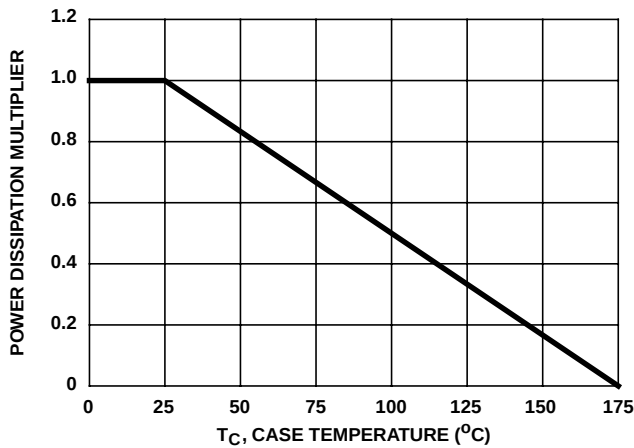


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

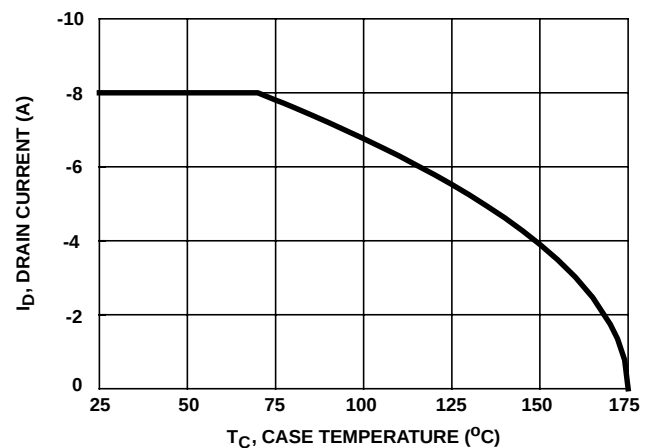


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

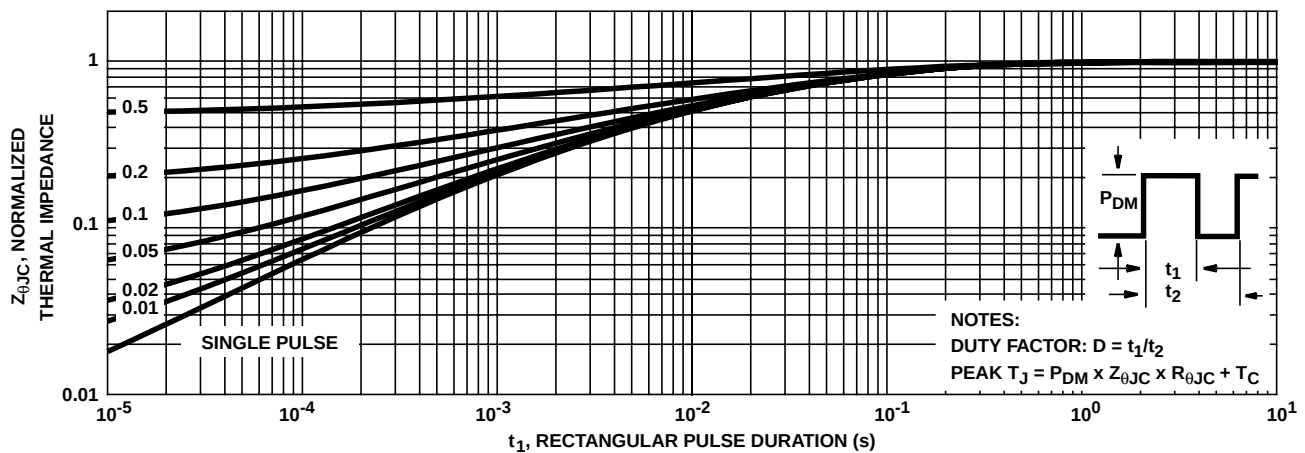


FIGURE 3. NORMALIZED TRANSIENT THERMAL IMPEDANCE

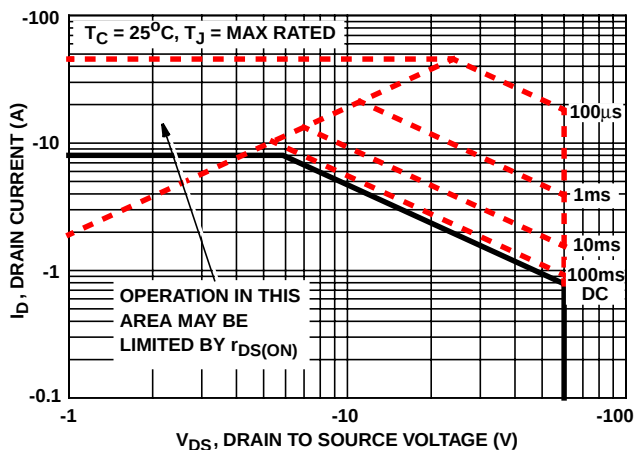


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

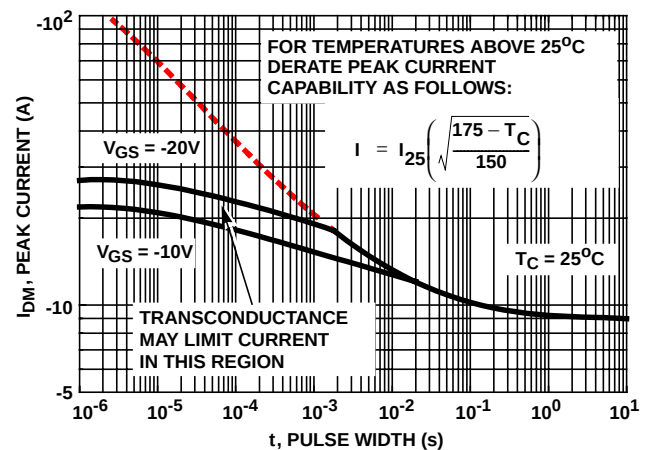


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)

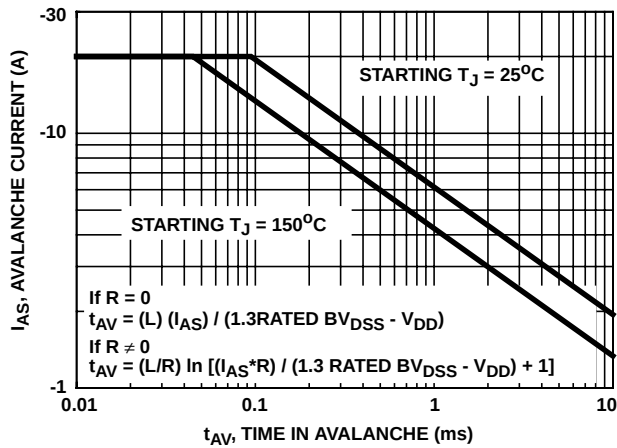


FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

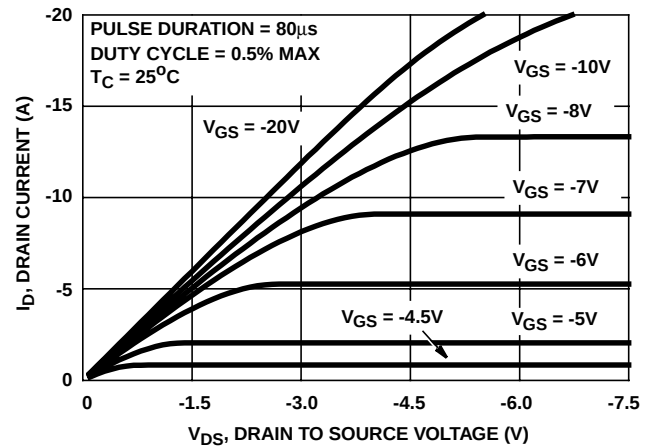


FIGURE 7. SATURATION CHARACTERISTICS

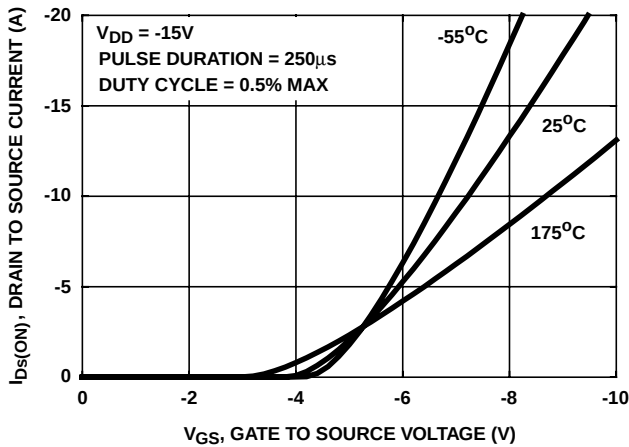


FIGURE 8. TRANSFER CHARACTERISTICS

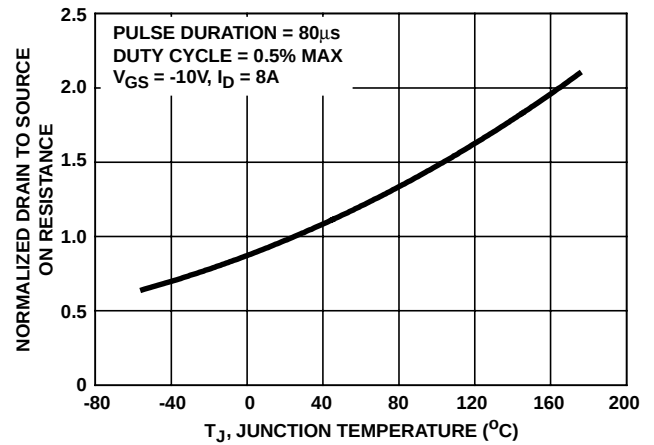


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

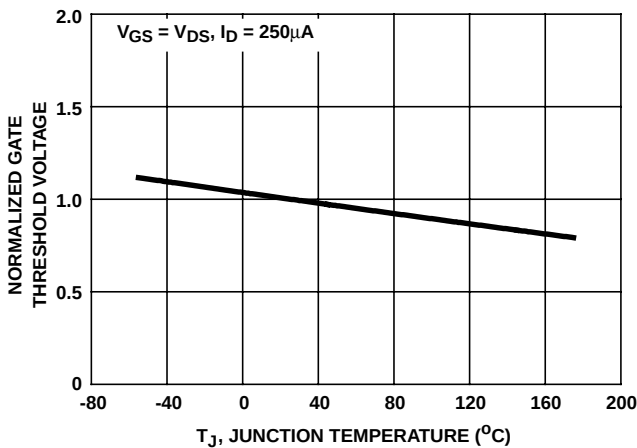


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

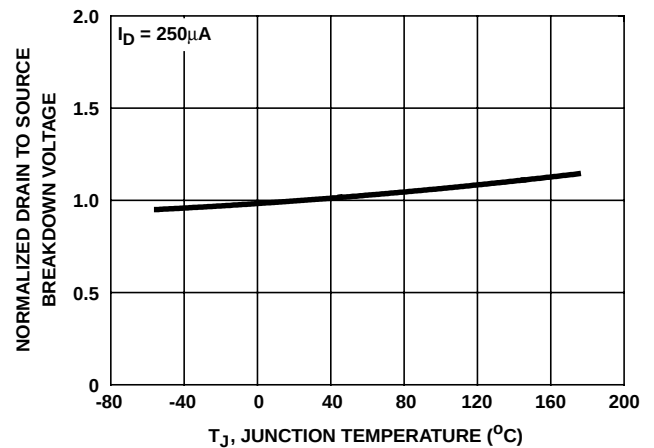


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

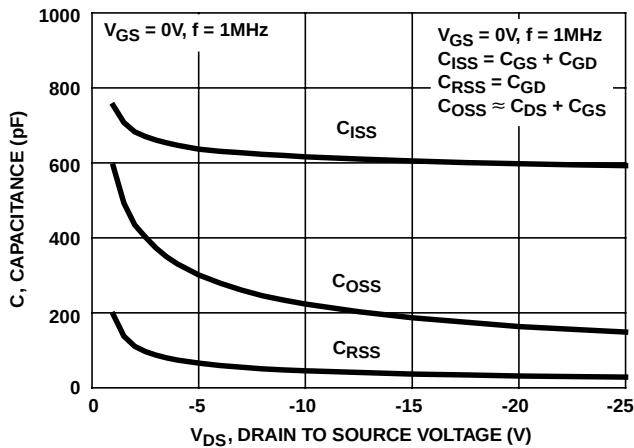
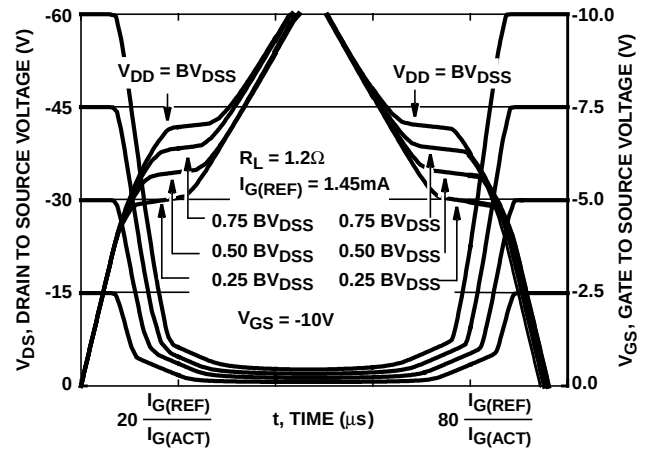


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

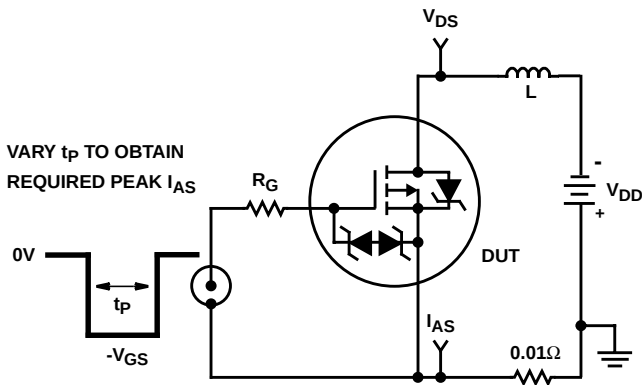


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

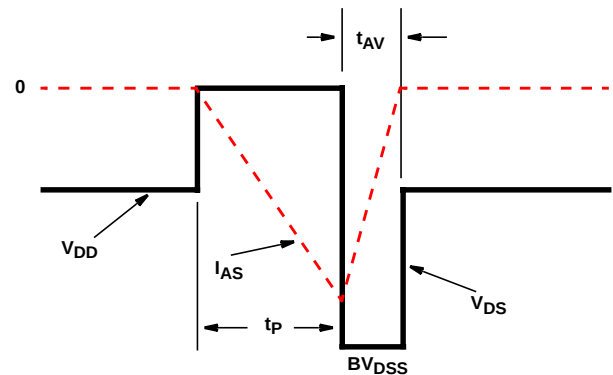


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

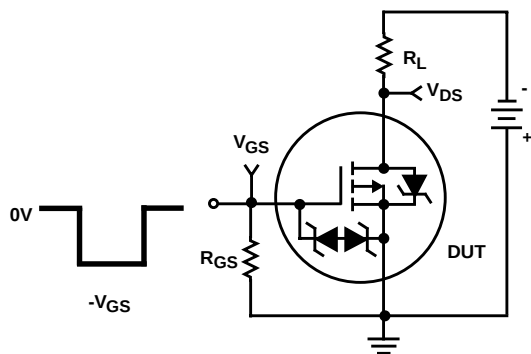


FIGURE 16. SWITCHING TIME TEST CIRCUIT

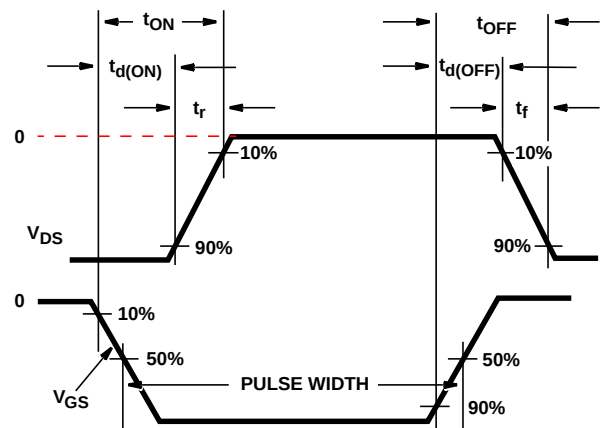


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

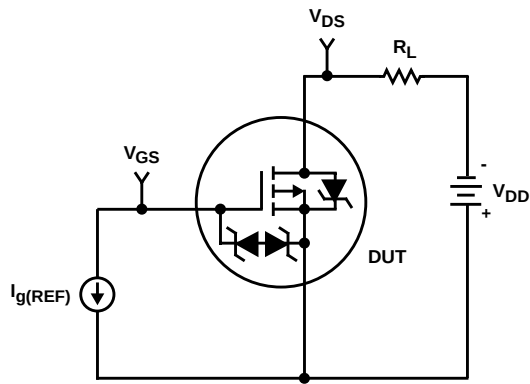


FIGURE 18. GATE CHARGE TEST CIRCUIT

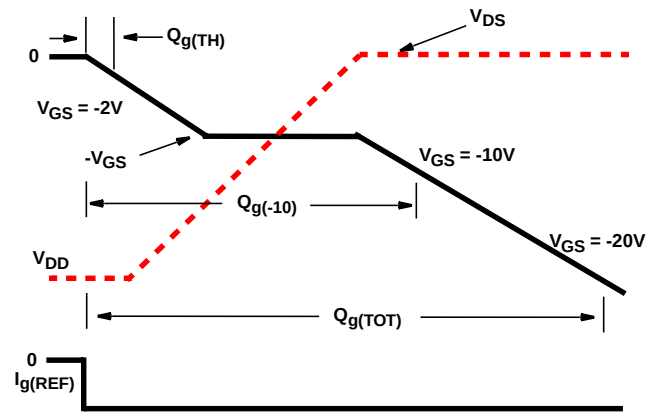


FIGURE 19. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

.SUBCKT RFP8P06E 2 1 3 REV 6/23/94

CA 12 8 7.24e-10
CB 15 14 8.04e-10
CIN 6 8 6.00e-10

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -79.2
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 6 8 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-10
LGATE 1 9 2.92e-9
LSOURCE 3 7 2.92e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 95.2e-3
RGATE 9 20 3.95
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 143.6e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

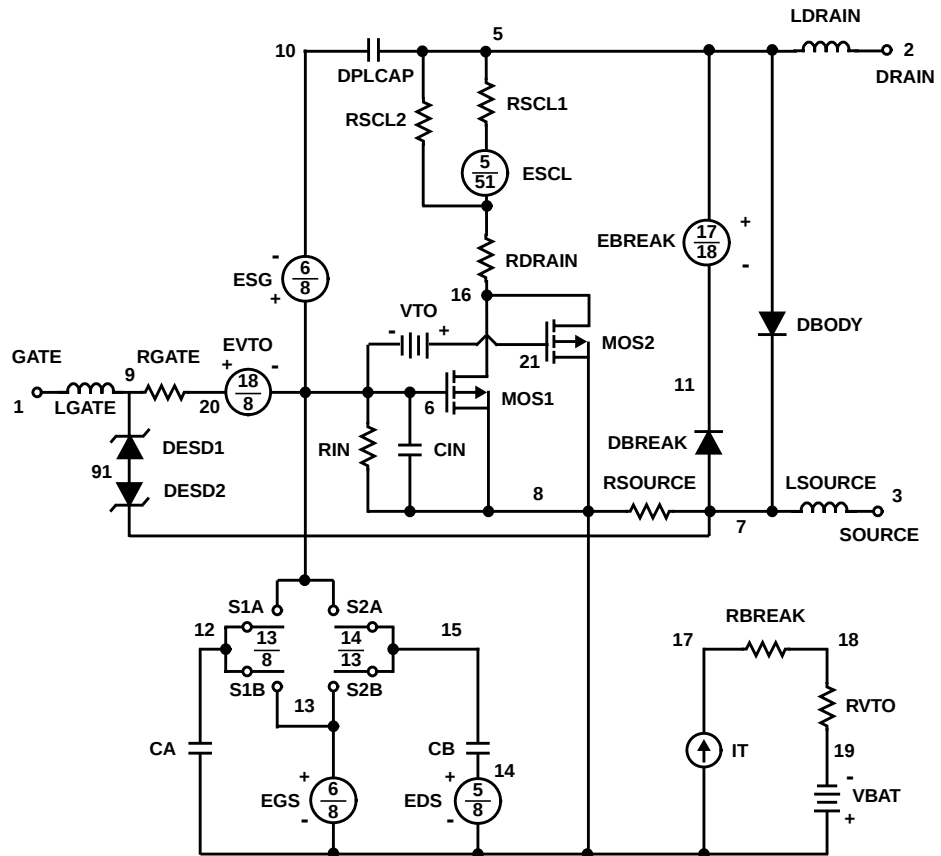
VBAT 8 19 DC 1
VTO 21 6 -0.804

ESCL 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))^(PWR(V(5,51)*1e6/22,9))}}

.MODEL DBDMOD D (IS=4.15e-15 RS=5.54e-2 TRS1=-1.32e-3 TRS2=-2.48e-6 CJO=6.06e-10 TT=7.50e-8)
.MODEL DBKMOD D (RS=4.66e-1 TRS1=1.58e-3 TRS2=-7.49e-6)
.MODEL DESD1MOD D (BV=20.2 TBV1=-1.25e-3 TBV2=5.79e-7 RS=36 NBV=50 IBV=7e-6)
.MODEL DESD2MOD D (BV=25.4 TBV1=-8.3e-4 TBV2=8.9e-7 NBV=50 IBV=7e-6)
.MODEL DPLCAPMOD D (CJO=2.49e-10 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.824 KP=5.163 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.48e-4 TC2=-1.42e-7)
.MODEL RDSMOD RES (TC1=5.40e-3 TC2=1.25e-5)
.MODEL RSCLMOD RES (TC1=1.75e-3 TC2=3.90e-6)
.MODEL RVTOMOD RES (TC1=-3.55e-3 TC2=-3.43e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=5.10 VOFF=3.10)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.10 VOFF=5.10)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.1 VOFF=-2.9)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.9 VOFF=2.1)

.ENDS

NOTE: For further discussion of the PSPICE model consult A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options; written by William J. Hepp and C. Frank Wheatley.



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