Features

- Overvoltage Monitoring
- Undervoltage Monitoring
- Cell Temperature Monitoring
- Self-diagnosis including
  - Comparator Functions
  - Communication Lines
  - Short and Open Measuring Lines
- Hot Plug-in Capable
- Less than 10 µA Stand-by Current
- Low Cell Imbalance Current (< 10 µA)
- Circuit Customization, e.g. for Over/Undervoltage Thresholds Possible for Adequate Volumes
- Cost-efficient Solution Due to Cost Optimized 30V CMOS Technology
- Daisy-chainable
  - Each IC Monitors 6 Battery Cells
  - 16 ICs (96 Cells) per String
  - No Limit on Number of Strings
  - Reliable Communication between Stacked ICs Due to Level Shifters with Current Sources
- Package SSO28

Applications

- Backup Battery-Cell Monitoring System for Li-ion Batteries
- Emergency Indicator in Li-ion Batteries
- Monitoring System in Li-ion Batteries

Benefits

- Highest Safety Level for Li-ion Battery Systems
- Circuit Customization, e.g. Over and Undervoltage Thresholds, Possible for Large Production Volumes

1. General Description

The ATA6871 is a battery cell monitoring circuit designed to act as an emergency, safety, or backup circuit in Li-ion battery systems for electrical and hybrid electrical vehicles (EV/HEV). It monitors overvoltage, undervoltage, and the cell temperature in Li-ion batteries without the need of a microcontroller. The circuit has an advanced self-test functionality, which checks the proper functionality of the monitoring comparators as well as the communication lines. It can be used as a monitoring circuit as well as an emergency indicator or as a backup system in Li-ion battery management systems. The ATA6871 can monitor four, five, or six battery cells. Up to 16 IC's can be cascaded. If one or more battery cells exceed the over or undervoltage thresholds for longer than 2 seconds, or if the temperature input exceeds the temperature limit for more than 2 seconds, a digital output signal is set to high.

Li-ion Battery Management Monitoring Emergency and Backup Circuit

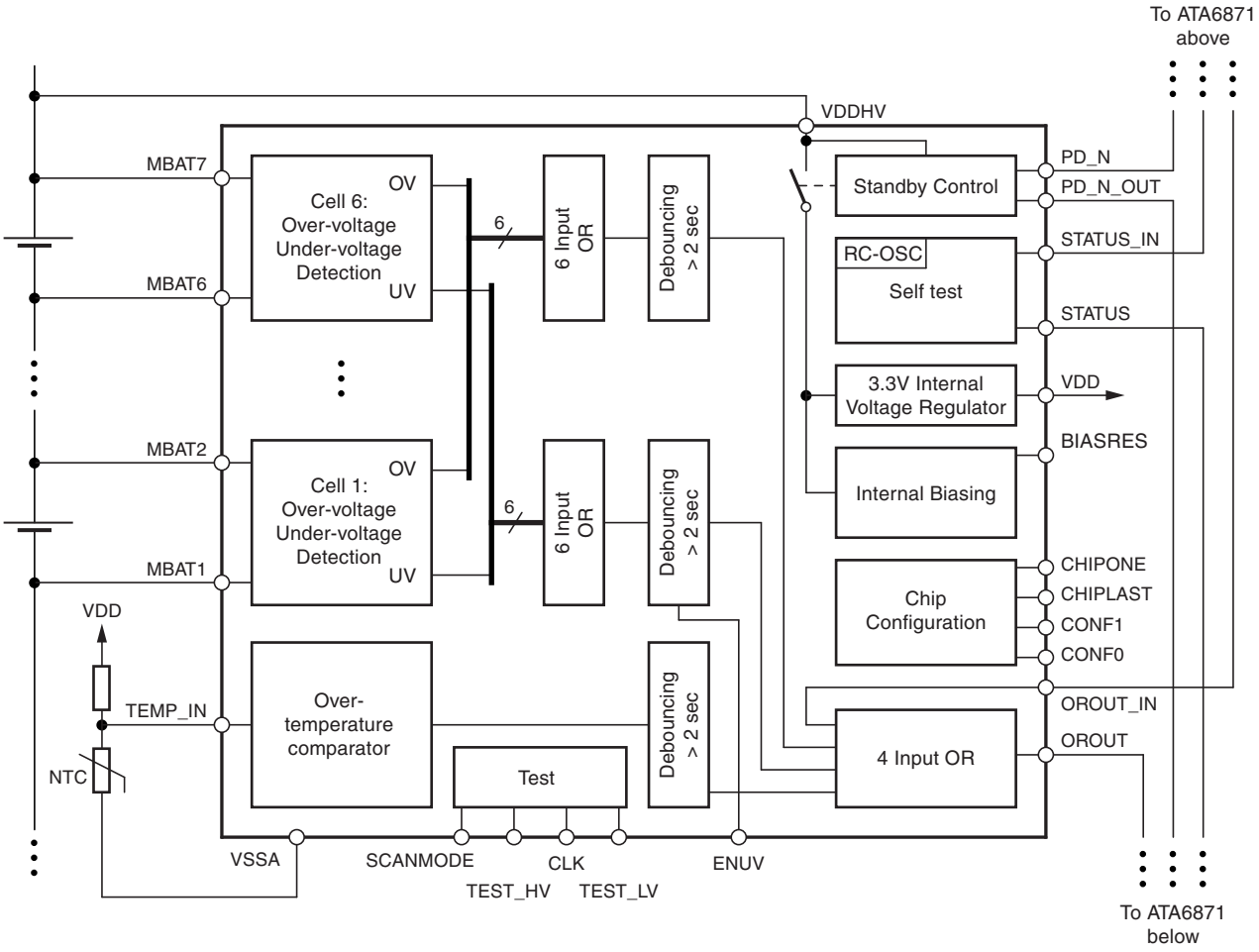
ATA6871

Preliminary

9123B–AUTO–07/09

2. Block Diagram

Figure 2-1. Top-level Block Diagram



3. Pin Configuration

Figure 3-1. Pinning SSO28

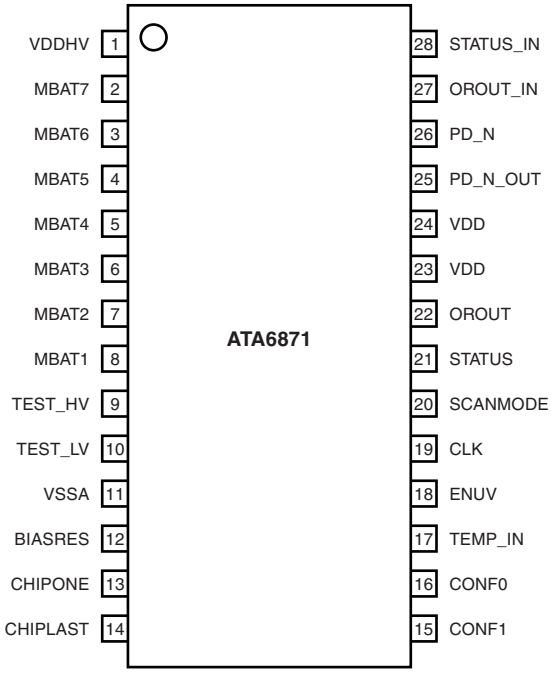


Table 3-1. Pin Description

Pin	Symbol	Function	Remark
1	VDDHV	Supply voltage	
2	MBAT7	Battery monitoring line	
3	MBAT6	Battery monitoring line	
4	MBAT5	Battery monitoring line	
5	MBAT4	Battery monitoring line	
6	MBAT3	Battery monitoring line	
7	MBAT2	Battery monitoring line	
8	MBAT1	Battery monitoring line	
9	TEST_HV	Test-mode pin	Keep pin open (output)
10	TEST_LV	Test-mode pin	Keep pin open (output)
11	VSSA	Negative supply voltage	
12	BIASRES	Internal supply current adjustment	
13	CHIPONE	Indicates circuit position in battery string (first, middle, last)	
14	CHIPLAST	Indicates circuit position in battery string (first, middle, last)	
15	CONF1	Programs how many cells will be monitored (4, 5, or 6 cells operating)	
16	CONF0	Programs how many cells will be monitored (4, 5, or 6 cells operating)	
17	TEMP_IN	Input for battery-cell temperature monitoring	
18	ENUV	Enable/Disable under-voltage detection	

Table 3-1. Pin Description

Pin	Symbol	Function	Remark
19	CLK	Test-mode pin	Connected to VSSA
20	SCANMODE	Test-mode pin	Connected to VSSA
21	STATUS	Status output	
22	OROUT	Output signal battery-cells in limits/out of limits	
23	VDD	Voltage regulator output	
24	VDD	Voltage regulator output	Internally connected to pin 23
25	PD_N_OUT	Power down output	
26	PD_N	Power down input	
27	OROUT_IN	Input for the OROUT signal of the upper ATA6871 circuit	
28	STATUS_IN	Input for the STATUS signal of the upper ATA6871 circuit	

4. System Overview

The ATA6871 can be stacked in one string up to 16 times.

Figure 4-1. Battery Management Architecture with one Battery String

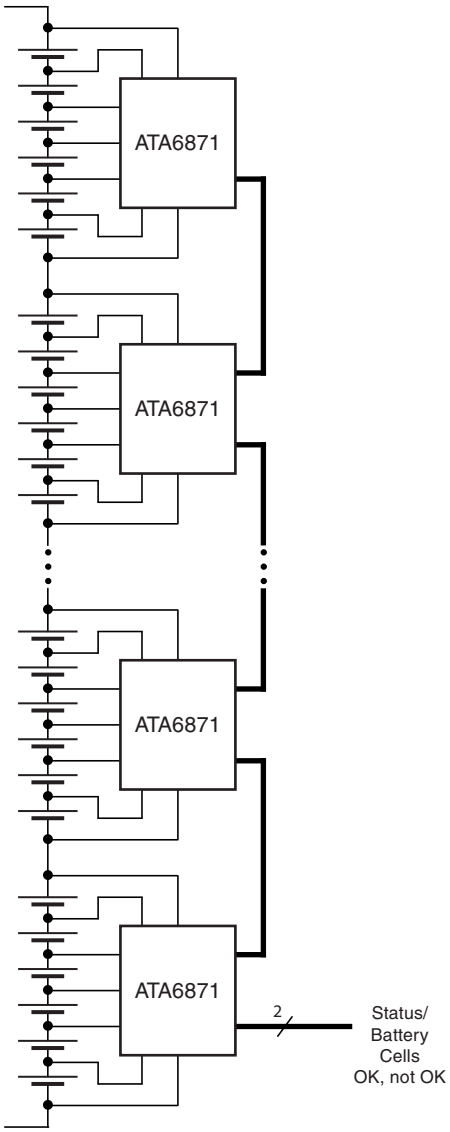
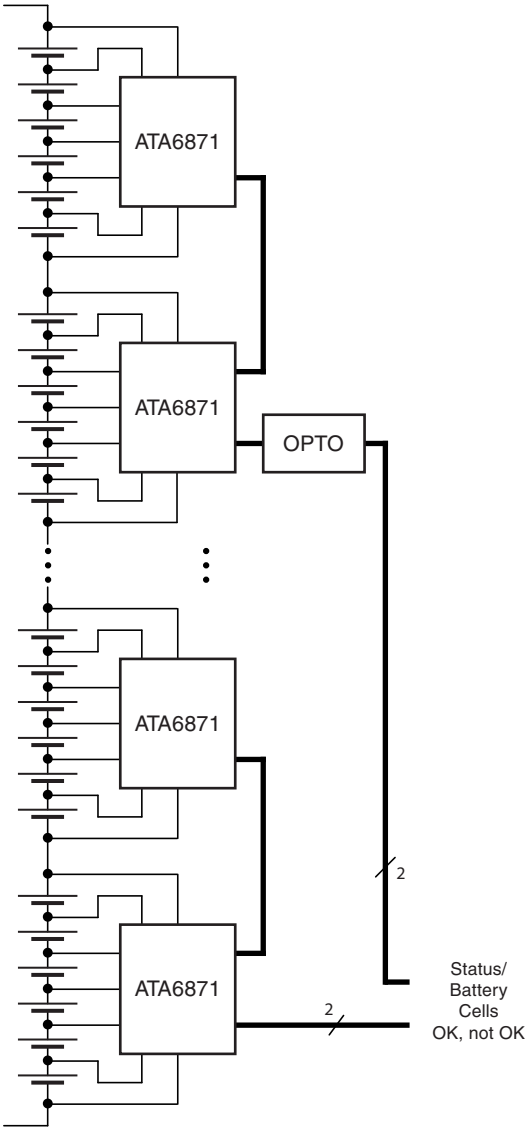


Figure 4-2. Battery Management Architecture with Several Battery Strings



5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Unless otherwise specified all voltages refer to pin VSSA. Logic Levels: 0 = VSSA, 1 = VDD.

Parameters	Pin	Symbol	Min.	Max.	Unit
Ambient temperature		T_A	–40	+85	°C
Junction temperature		T_J	–40	+125	°C
Storage temperature		T_S	–40	+150	°C
Battery cell voltage		$V_{(MBATi+1)} - V_{MBATi}$	–0.3	+5.5	V
$V_{VDDHV} - V_{VMBAT7}$max		$V_{VDDHV} - V_{VMBAT7}$	–5.5	+0.3	V
V_{MBAT1}	MBAT1	V_{MBAT1}	–0.3	+0.3	V
Supply voltage	VDDHV	V_{VDDHV}	–0.3	+30	V
Supply voltage (regulator is off)	VDD	V_{VDD}	–0.3	+5.5	V
Input voltage for logic I/O pins	CHIPONE, CHIPLAST, CONF0, CONF1, SCANMODE, CLK, TEST_HV, TEST_LV, ENUV, OROUT	$V_{CHIPONE}$, $V_{CHIPLAST}$, V_{CONF0}, V_{CONF1}, $V_{SCANMODE}$, V_{CLK}, V_{TEST_HV}, V_{TEST_LV}, V_{ENUV}, V_{OROUT}	–0.3	VDD + 0.3	V
Input voltage for analog low voltage input pins	BIASRES, TEMP_IN	$V_{BIASRES}$, V_{TEMP_IN}	–0.3	VDD + 0.3	V
Input voltage for digital high voltage input pins	OROUT_IN, STATUS_IN	V_{OROUT_IN}, V_{STATUS_IN}	VDDHV – 0.3	VDDHV + 0.3	V
Logic output pin STATUS	STATUS	V_{STATUS}	–0.3	+5.5	V
Input	PD_N	V_{PD_N}	VDDHV – 5.5	VDDHV + 0.3	V
Output	PD_N_OUT	$V_{PD_N_OUT}$	–5.5	+0.3	V
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		ESD	±2		kV
CDM ESD STM 5.3.1			500		V
CDM ESD STM 5.3.1	VDDHV, CHIPLAST, CONF1, STATUS_IN	ESD	750		V
Latch Up according to AECQ100-004		LATCH-UP	±100		mA

6. Thermal Resistance

Parameters	Symbol	Value	Unit
Maximum thermal resistance junction-ambient	R_{thja} max	49	K/W

7. Circuit Description and Electrical Characteristics

Unless otherwise specified, all parameters in this section are valid for a supply voltage range of 6.9V < V_{VDDHV} < 30V and a battery cell voltage of $V_{(MBATi+1)} - V_{MBATi}$ = 0V to 5V, –40°C < TA < 85°C, all values refer to pin VSSA, unless otherwise specified.

7.1 Operating Modes

The ATA6871 has two operation modes:

1) Power-down Mode

2) ON Mode/Selfdiagnosis

7.1.1 Power-down Mode

In Power-down Mode all blocks of the IC are switched off.

The circuit can be switched from Power-down to ON Mode or back via the PD_N input. If the pin is connected to VDDHV, for example, via an external optocoupler the circuit is in ON Mode. If several ATA6871 are stacked, the power-down signal must be only provided for the IC on the top level of the stack. The next lower IC is getting this information from the PD_N_OUT output of it's upper IC. The PD_N_OUT pin must be connected either to the PD_N pin of the next lower ATA6871 or to VSSA.

Figure 7-1. Power-down

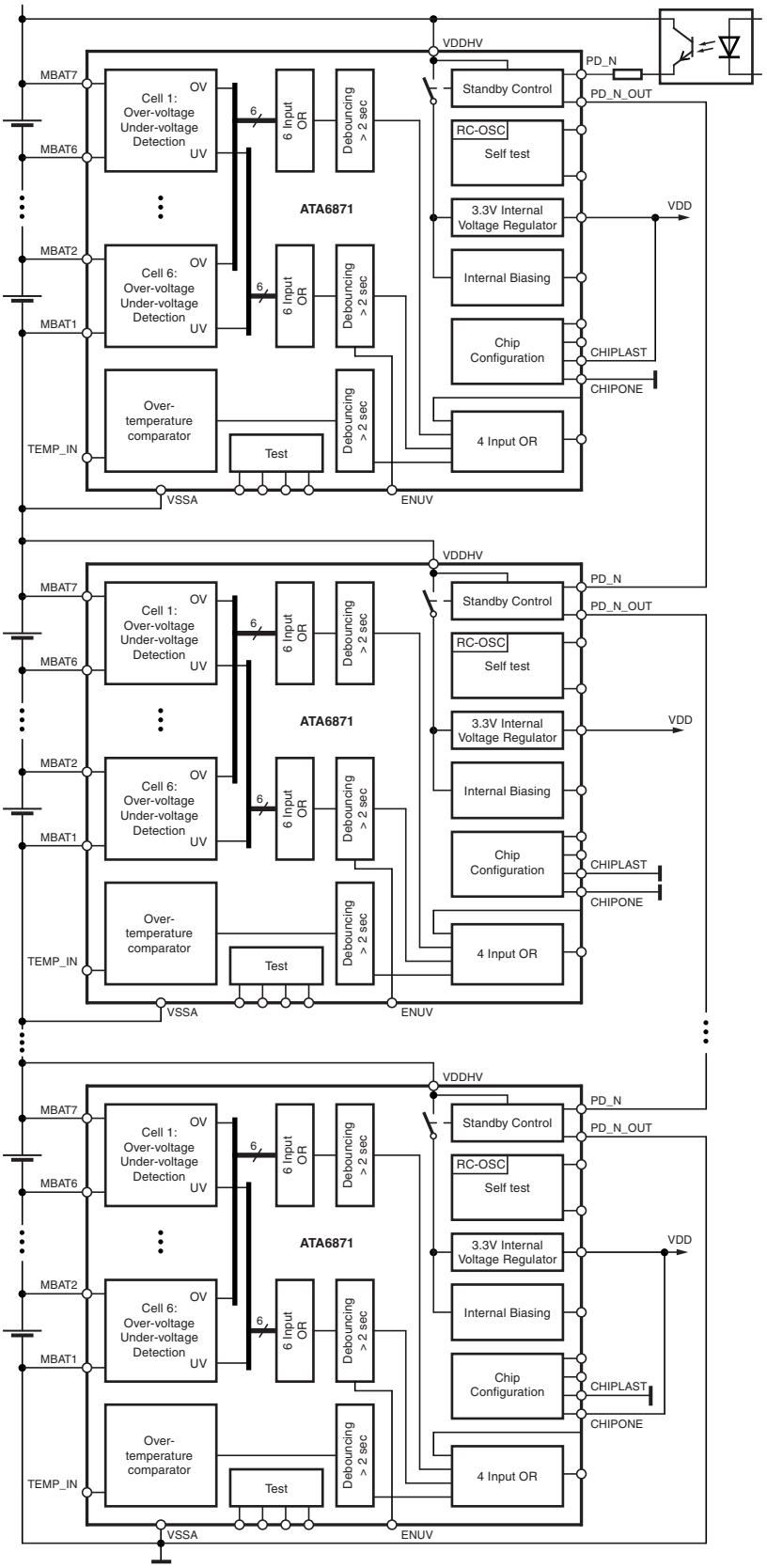


Table 7-1. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	Maximum allowed input current in Power-down Mode (e.g., leakage current of an optocoupler)		PD_N	I_{PD_N}			50	µA	A
1.2	Input current in ON Mode		PD_N	I_{PD_N}	2.5		5	mA	A
1.3	Current consumption in Power-down Mode IVDDHV + IMBATi_max(1)	VMBAT(i+1) – VMBAT(i) = 3.7V					10	µA	A
1.4	Imbalance from battery cell to battery cell in Power-down Mode	VMBAT(i+1) – VMBAT(i) = 3.7V					10	µA	A
1.5	Maximum input voltage (Power-down Mode)	I_{PD_N} = 0 to 50 µA	PD_N	$V_{VDDHV} - V_{PD_N}$			5	V	A
1.6	Propagation delay time from Power-down Mode to ON Mode	C_{VDD} = 10 nF	VDD	t_{VDDON}			1	ms	A
1.7	Propagation delay time from ON Mode to Power-down Mode	C_{VDD} = 10 nF	VDD	t_{VDDOFF}			11	ms	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Largest input current of the inputs MBAT1 to MBAT7

7.1.2 ON Mode/Selfdiagnosis

When the PD_N-signal goes from low to high, the self diagnosis of the ATA6871 starts. During this self diagnosis the following tests are performed:

- Test if over/undervoltage or overtemperature comparators are able to switch or if they stuck to 0 or 1
- Test if pins OROUT_IN, OROUT in stacked ICs are able to switch or if they stuck to 0 or 1 and if the connection to next ATA6871 is available or not
- Test if pins STATUS_IN, STATUS are able to switch or if they stuck to 0 or 1 and if the connection to next ATA6871/MCU is available or not
- Detect open or shorted input pins MBAT1 to MBAT7
- Detect wrong setting of CONF0, CONF1 (e.g. 4 cell configuration programmed, 6 cells used)

If self diagnosis fails, the STATUS of the lowest ATA6871 is constant low. If the self diagnosis succeeds, the STATUS of the lowest ATA6871 is toggling.

The circuit will suppress failures detected during the self test and provide only results from good tested comparators connections to pin OROUT. This enables the system to monitor the rest of the battery cells if one connection/comparator fails. If, for example, the connection of the OROUT signal between two ATA6871s is open, the OROUT_IN signal of the lower ATA6871 will be ignored, but all the cells of this ATA6871 and ICs below will be observed in the normal way. If the battery cell voltage exceeds 4.9V or is below 1.5V during the self-diagnosis, the affected comparator will be detected as defect, and the output of the affected comparator will be also suppressed until the next self diagnosis.

If, after the self test has passed, one of the comparator in the stack detects under or overtemperature at a battery cell, the output OROUT switches from low to high. The battery cell undervoltage detection can be disabled with the digital input ENUV.

Table 7-2. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.1	Supply voltage		VDDHV	V_{VDDHV}	6.9		30	V	A
2.2	Current consumption	No external load	VDDHV	I_{VDDHV}			6	mA	A
2.3	Input current		MBAT(i)	$I_{MBAT(i)}$			5	µA	A
2.4	Digital output signal	Self diagnosis ongoing or failed	STATUS	V_{STATUS}		Constant low			A
		Self diagnosis passed successful			15	Toggle frequency	50	Hz	A
2.5	Self diagnosis time	i = number of stacked ICs		$t_{selfdiag}$	2 + 0.85 × i		8 + 2.2 × i	ms	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7.2 Battery Cell Over and Undervoltage Detection

If, after the self diagnosis of the chip has passed, one of the monitored battery cell voltages $V_{(MBATi+1)} - V_{MBATi}$ is above the overvoltage threshold or below the undervoltage threshold for $t > t_{Debounce}$, the OROUT output goes high. The battery cell undervoltage detection can be disabled with the digital input ENUV.

Table 7-3. Truth Table:

PIN	Symbol	Value	Function
ENUV	V_{ENUV}	0	Undervoltage detection disabled
		1	Undervoltage detection enabled

Table 7-4. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.1	Overvoltage detection on threshold		MBAT(i)	$V_{(MBAT(i+1))} - V_{MBAT(i)}$	4.3	4.45	4.6	V	A
3.2	Overvoltage detection off threshold		MBAT(i)	$V_{(MBAT(i+1))} - V_{MBAT(i)}$	4.2	4.35	4.5	V	A
3.3	Overvoltage detection hysteresis		MBAT(i)	$\Delta V_{(MBAT(i+1))} - V_{MBAT(i)}$	70			mV	A
3.4	Undervoltage detection on threshold		MBAT(i)	$V_{(MBAT(i+1))} - V_{MBAT(i)}$	1.7	1.8	1.9	V	A
3.5	Undervoltage detection off threshold		MBAT(i)	$V_{(MBAT(i+1))} - V_{MBAT(i)}$	1.8	1.9	2.0	V	A
3.6	Undervoltage detection hysteresis		MBAT(i)	$\Delta V_{(MBAT(i+1))} - V_{MBAT(i)}$	70			mV	A
3.7	Debouncing time			$t_{Debounce}$	1		3	s	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7.3 Battery Cell Overtemperature Detection

If the voltage at the input TEMP_IN is less than the half of VDD threshold for $t > t_{Debounce}$, the OROUT output goes high.

To disable this function, connect TEMP_IN to VDD.

If the input is open (high impedance), an internal current will force the comparator to the overtemperature state and OROUT will switch to high.

Figure 7-2. Overtemperature Detection

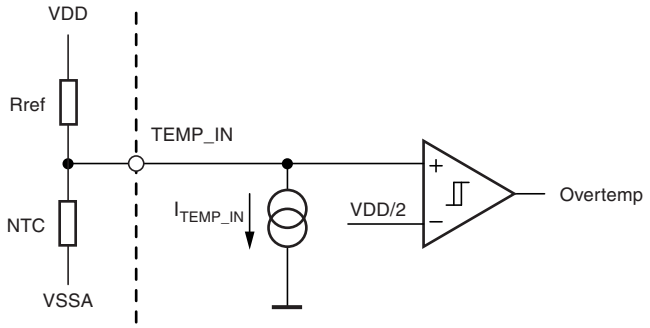


Table 7-5. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.1	Overtemperature detection on threshold		TEMP_IN	V_{TEMP_IN}	VDD/2 – 100 mV	VDD/2	VDD/2 + 100 mV	V	A
4.2	Overtemperature detection off threshold		TEMP_IN	V_{TEMP_IN}	VDD/2 – 50 mV	VDD/2 + 50 mV	VDD/2 + 150 mV	V	A
4.3	Overtemperature detection hysteresis		TEMP_IN	ΔV_{TEMP_IN}	30			mV	A
4.4	Resistor Divider			$R_{Divider} = R_{NTC} + R_{Rref}$	3		1000	kΩ	D
4.5	Input Current	V_{TEMP_IN}=1.65V	TEMP_IN	I_{TEMP_IN}	0.4		0.6	µA	A
4.6	Debouncing Time			$t_{Debounce}$	1		3	s	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7.4 ATA6871 Configuration

7.4.1 Device Position

The ATA6871 can be cascaded up to 16 times in one string. The input pins CHIPONE and CHIPLAST define the first and the last IC in a string.

Table 7-6. Device Position

CHIPONE	CHIPLAST	Configuration
0	0	ICs between the first and the last IC (up to 14 ICs)
0	1	Last cascaded chip, connected to power down optocoupler
1	0	First chip in a string (master)
1	1	First and last chip: (if only one IC is used per string)

7.4.2 Number of Cells Configuration

The ATA6871 can work with either four, five, or six cells. This can be programmed with the input pins CONF0 and CONF1. When used with 5 cells, the inputs MBAT5 and 6 must be connected together, when used with 4 cells the inputs MBAT4, MBAT5 and MBAT6 must be connected together (see also Figure 7-3 to Figure 7-5).

Table 7-7. Cells Configuration

CONF1	CONF0	Configuration	Notes
0	0	4 cells configuration	Over/undervoltage comparators between MBAT4,5 and MBAT6 are disabled
0	1	5 cells configuration	Over/undervoltage comparator between MBAT5 and MBAT6 is disabled
1	0	Do not use, reserved for test purposes	
1	1	6 cells configuration	

Figure 7-3. 6 Cells Operation

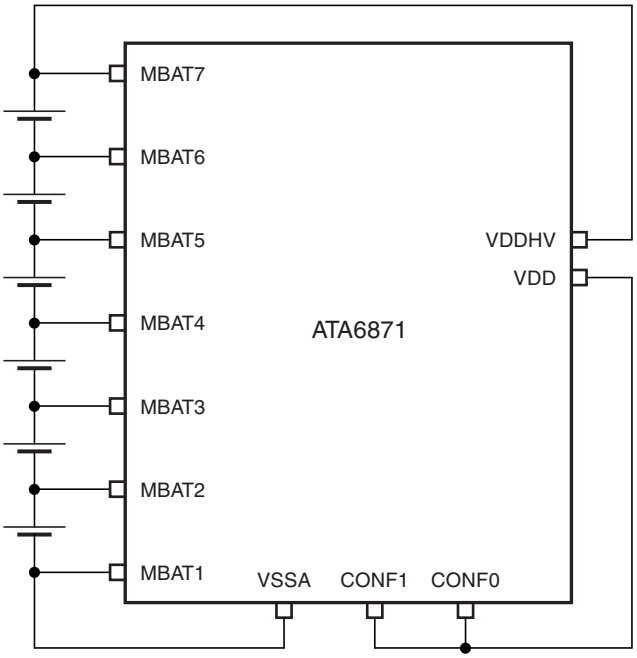


Figure 7-4. 5 Cells Operation

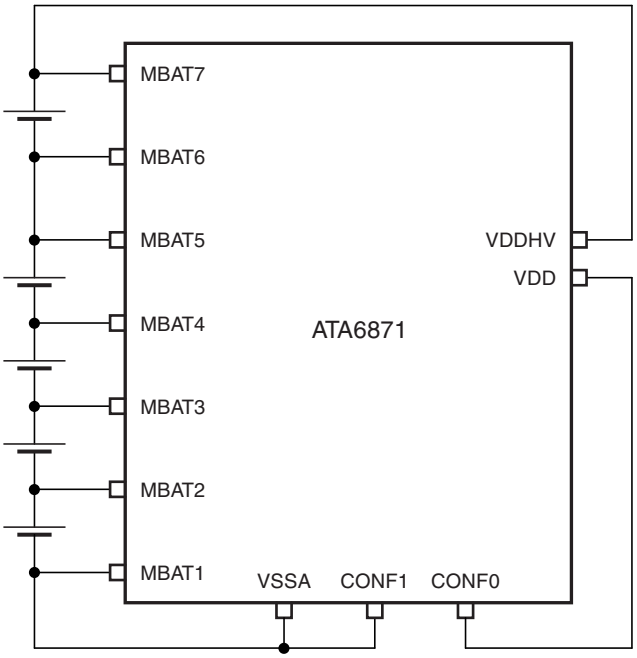
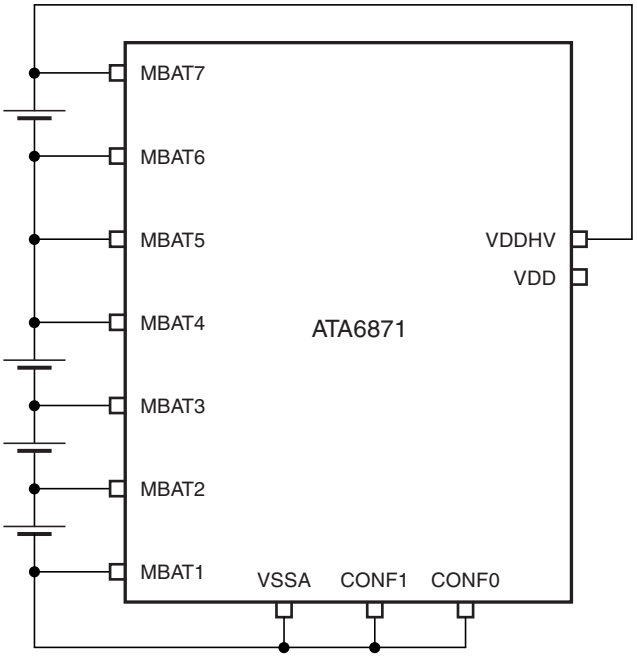


Figure 7-5. 4 Cells Operation



7.5 Supplies

7.5.1 Voltage Regulator

The circuit includes a linear 3.3V voltage regulator, which supplies internal blocks as well as external components, e.g., the resistor divider for the over-temperature measurement. The regulator is supplied out of VDDHV. A load capacitor of 10 nF has to be used for stabilization purposes.

Table 7-8. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5.1	Output voltage		VDD	V_{VDD}	3.1	3.3	3.5	V	A
5.2	Maximum output current for external components		VDD	I_{VDD}	–5			mA	A
5.3	Load capacitor		VDD	C_{load}	8	10	12	nF	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7.5.2 Central Biasing

This block generates a precise bias current to supply internal blocks of the IC.

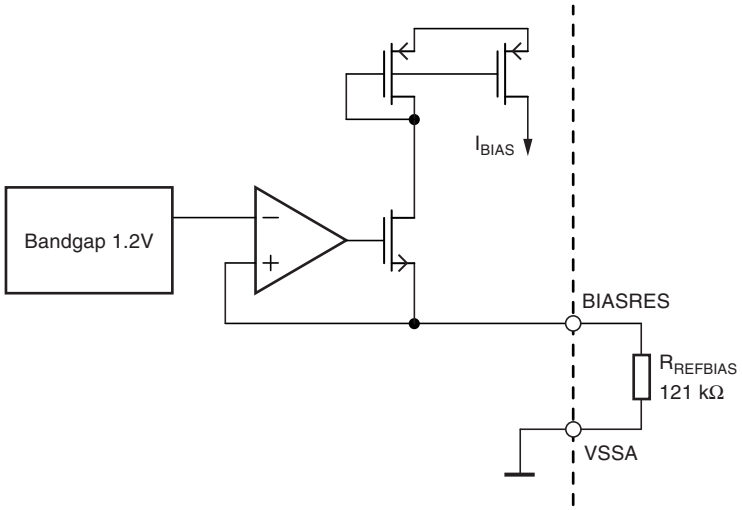
External load cannot be connected to this pin.

Table 7-9. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
6.1	Biasing voltage		BIASRES	$V_{BIASRES}$		1.2		V	A
6.2	External resistor			$R_{Refbias}$		121		kΩ	D
6.3	Tolerance			$\Delta R_{Refbias}$	–1		+1	%	D
6.4	Maximum external parasitic capacitor		BIASRES	$C_{External}$			50	pF	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 7-6. Internal Bias Current Generation



7.6 Digital Inputs and Outputs

7.6.1 Digital Output Characteristics

If the ATA6871 is configured as first IC (master) in a string (CHIPONE = 1, CHIPLAST = 0 or 1), the output OROUT acts as a push-pull output, the output STATUS as an open drain output. If the ATA6871 is configured to be a stacked IC (CHIPONE = 0, CHIPLAST = 0 or 1), the output signals STATUS and OROUT coming from the upper IC need to be transferred to the STATUS and OROUT output of the master in the string via the STATUS_IN and OROUT_IN inputs. In this case the OROUT and STATUS outputs act as level shifters based on current sources.

Table 7-10. Digital Output Characteristics (OROUT, STATUS)

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.1	High-level output voltage	Iout = –5 mA CHIPONE = 1	OROUT	V_{OROUT},	0.8 × VDD			V	A
7.2	Low-level output voltage	Iout = +5 mA CHIPONE = 1	OROUT, STATUS	V_{OROUT}, V_{STATUS}			0.2 × VDD	V	A
7.3	Low-level output current	Vout = –0.3V to +0.3V, CHIPONE = 0	OROUT, STATUS	I_{OROUT}, I_{STATUS}	–13		–8	µA	A
7.4	High-level output current	Vout = –0.3V to +0.3V, CHIPONE = 0	OROUT, STATUS	I_{OROUT}, I_{STATUS}	–65		–44	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7.6.2 Digital Input Characteristics

Table 7-11. Digital Input Characteristics (OROUT_IN, STATUS_IN)

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.1	Low-level input current	(VDDHV + 1.4V) ±300 mV	OROUT_IN, STATUS_IN	I_{OROUT_IN}, I_{STATUS_IN}	15			µA	A
8.2	High-level input current	(VDDHV + 1.4V) ±300 mV	OROUT_IN, STATUS_IN	I_{OROUT_IN}, I_{STATUS_IN}			42	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Table 7-12. Digital Input Characteristics PINs CHIPONE, CHIPLAST, CONF0, CONF1, ENUV

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.1	High-level input voltage		CHIPONE, CHIPLAST, CONF0, CONF1, ENUV	$V_{CHIPONE}$, $V_{CHIPLAST}$, V_{CONF0}, V_{CONF1}, V_{ENUV}	0.7 × VDD		VDD	V	A
9.2	Low-level input voltage		CHIPONE, CHIPLAST, CONF0, CONF1, ENUV	$V_{CHIPONE}$, $V_{CHIPLAST}$, V_{CONF0}, V_{CONF1}, V_{ENUV}			0.3 × VDD	V	A
9.3	Hysteresis		CHIPONE, CHIPLAST, CONF0, CONF1, ENUV	$V_{CHIPONE}$, $V_{CHIPLAST}$, V_{CONF0}, V_{CONF1}, V_{ENUV}	0.05 × VDD			V	C
9.4	Input current		CHIPONE, CHIPLAST, CONF0, CONF1, ENUV	$V_{CHIPONE}$, $V_{CHIPLAST}$, V_{CONF0}, V_{CONF1}, V_{ENUV}			1	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7.6.3 Test-mode Pins

The test-mode pins TEST_HV, TEST_LV (outputs) have to be kept open in the application. The test-mode pins CLK, SCANMODE (inputs) have to be connected to VSSA. These inputs have an internal pull-down resistor.

Table 7-13. Digital Input Characteristics PINs SCANMODE, CLK

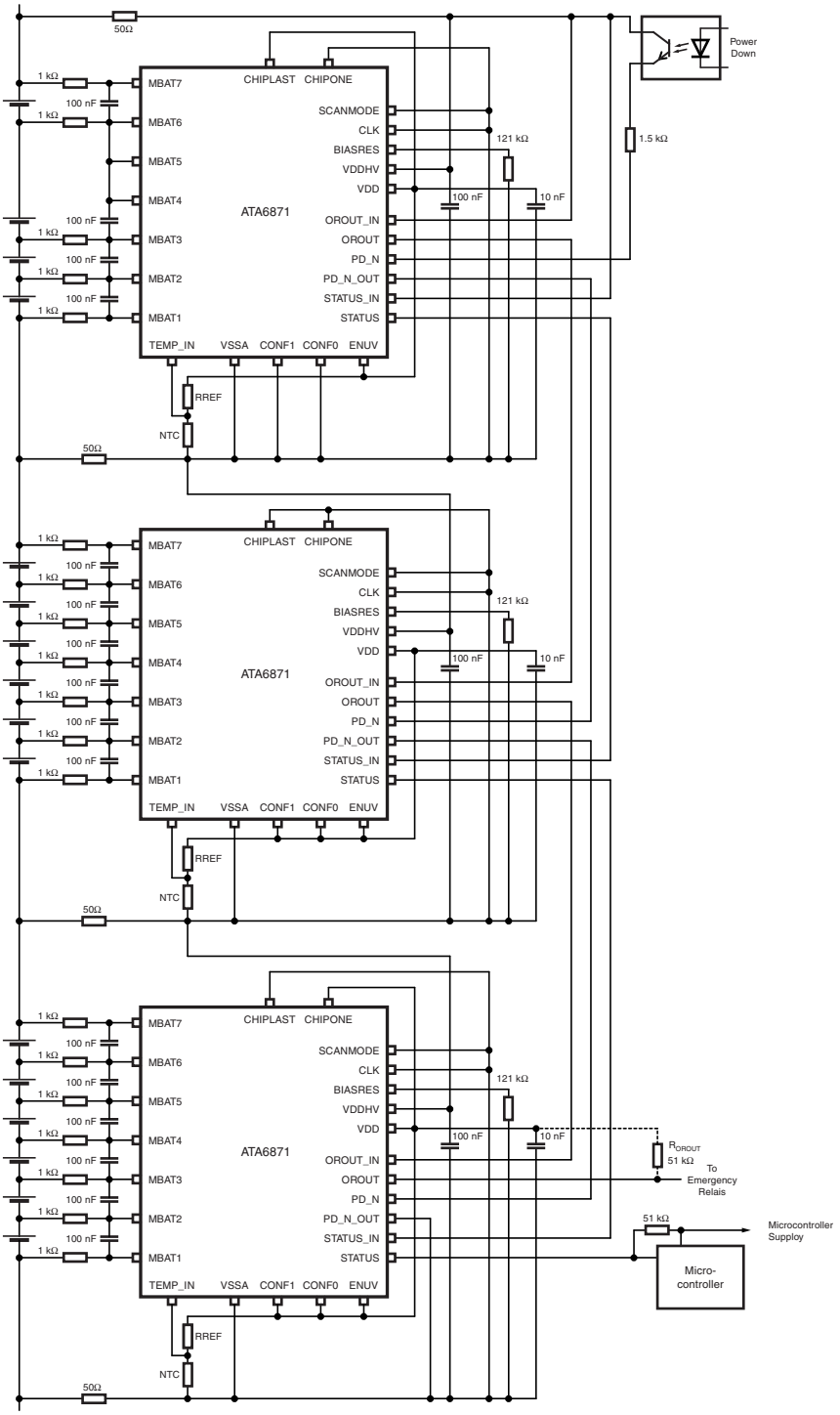
No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.1	Pull-down resistor		SCANMODE, CLK	$R_{SCANMODE}$, R_{CLK}	50		200	kΩ	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Application

Figure 8-1 shows an application with 3 stacked ATA6871s. The ATA6871 on the highest potential, is configured to monitor only four instead of six battery cells.

Figure 8-1. Typical Application



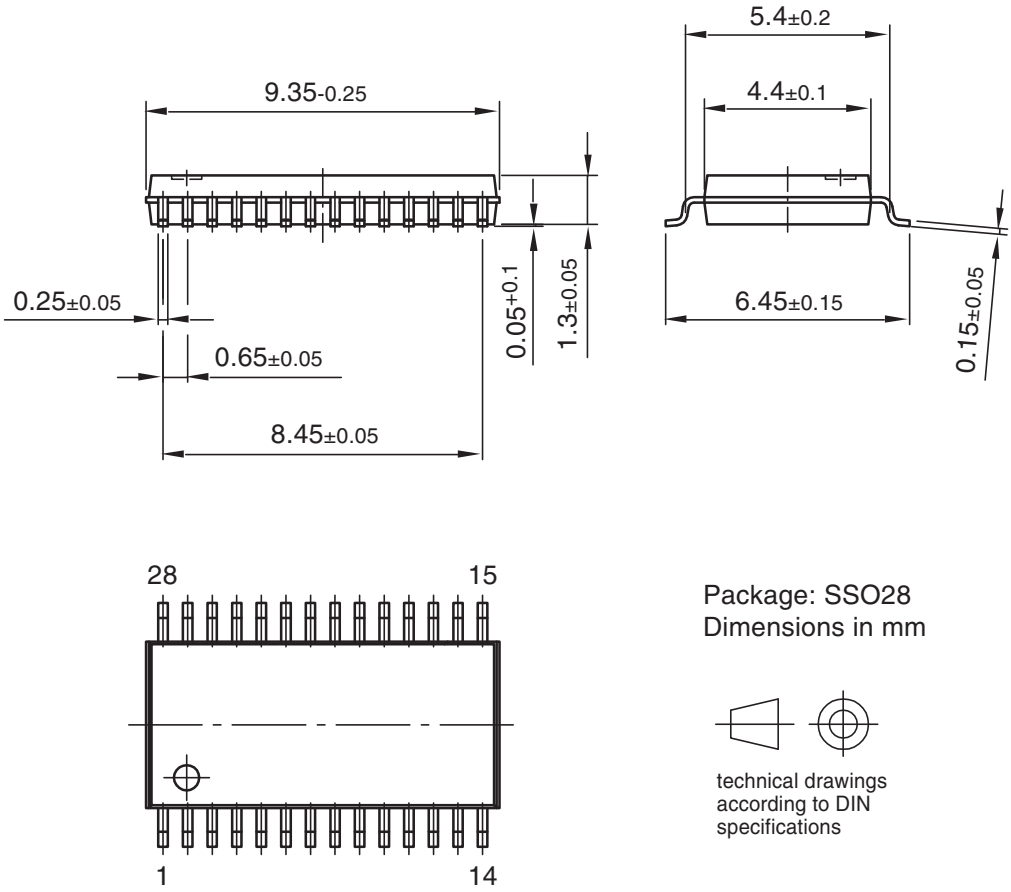
Note: R_{OROUT} can be used to check if the connection between the lowest ATA6871 and the emerging Relays is available.

9. Ordering Information

Extended Type Number	Package	MOQ
ATA6871-TLPW	SSO28	1,000 pieces
ATA6871-TLQW	SSO28	4,000 pieces

10. Package Information

The IC is packaged in a SSO28 package — green (lead-free/RoHS) package.



Package: SSO28
Dimensions in mm

technical drawings
according to DIN
specifications

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11. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9123B-AUTO-07/09	• Table 5 “Absolute Maximum Ratings” on page 7 changed • Table 7-1 “Electrical Characteristics” on page 10 changed • Heading “ON-Mode/Selfdiagnosis” on page 10 changed • Table 7-4 “Electrical Characteristics” on page 12 changed • Table 7-8 “Electrical Characteristics” on page 16 changed • Table 7-10 “Digital Output Characteristics (OROUT, STATUS)” on page 19 changed • Table 7-11 “Digital Input Characteristics (OROUT_IN, STATUS_IN)” on page 19 changed • Table 7-12 “Digital Input Characteristics PINs CHIPONE, CHIPLAST, CONF0, CONF1, ENUV” on page 19 changed

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
auto_control@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

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