May 2001

National Semiconductor

# LM2640
# Dual Adjustable Step-Down Switching Power Supply Controller

## General Description

The LM2640 is a dual step-down power supply controller intended for application in notebook personal computers and other battery-powered equipment.

Fixed-frequency synchronous drive of logic-level N-channel power MOSFETs is combined with an optional pulse-skipping mode to achieve ultra efficient power conversion over a 1000:1 load current range. The pulse-skipping mode can be disabled in favor of fixed-frequency operation regardless of the load current level.

High DC gain and current-mode feedback control assure excellent line and load regulation and a wide loop bandwidth for fast response to dynamic loads.

An internal oscillator fixes the switching frequency at 200 kHz. Optionally, switching can be synchronized to an external clock running as fast as 400 kHz.

An optional soft-start feature limits current surges from the input power supply at start up and provides a simple means of start-up sequencing.

Logic-level inputs allow the controllers to be turned ON and OFF separately.

## Key Specifications

- 96% efficient
- 5.5 to 30V input range
- Dual outputs adjustable from 2.2 to 6V
- 0.5% typical load regulation error
- 0.002%/V typical line regulation error

## Features

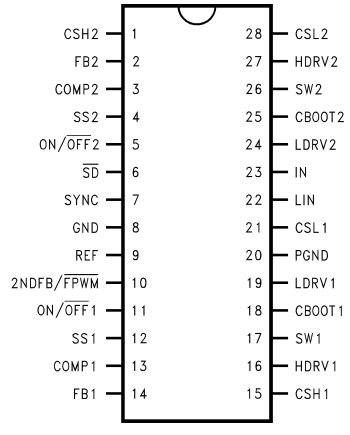
- 200 kHz fixed-frequency switching
- Switching synchronization with an external signal up to 400 kHz
- Optional pulse-skipping mode
- Adjustable secondary feedback
- Input undervoltage lockout
- Output undervoltage shutdown protection
- Output overvoltage shutdown protection
- Programmable soft-start (each controller)
- 5V, 50 mA linear regulator output
- Precision 2.5V reference output
- 28-pin TSSOP

## Applications

- Notebook and subnotebook computers
- Wireless data terminals
- Battery-powered instruments

## Connection Diagram and Ordering Information

**28-Lead TSSOP (MTC)**




10014801

**Top View**
**Order Number LM2640MTC-ADJ**
**See NS Package Number MTC28**

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## Pin Description

(Refer to Typical Application Circuits)

| Pin # | Name | Function |
|---|---|---|
| 1 | CSH2 | The sense point for the positive side of the voltage across the current sense resistor (R13) placed in series with output #2. |
| 2 | FB2 | The regulated output voltage appearing at output #2 is sensed using this pin by connecting it to the center of the output resistive divider (R15 and R16). |
| 3 | COMP2 | An R-C network made up of R11, C10, and C12 is connected to this pin which provides loop compensation for regulated output #2. |
| 4 | SS2 | This provides programmable soft-start for the #2 output along with capacitor C15. |
| 5 | ON/$\overline{\text{OFF}}$2 | This pin turns off only output #2. |
| 6 | $\overline{\text{SD}}$ | The part can be put into “sleep” mode using this pin, where both outputs are off and the internal chip functions are shut down. |
| 7 | SYNC | The internal oscillator may be synchronized to an external clock via this pin. |
| 8 | GND | Connect this pin to circuit Signal Ground. |
| 9 | REF | Internal 2.5V reference voltage. This voltage is turned off by the $\overline{\text{SD}}$ pin, but remains on if either or both ON/$\overline{\text{OFF}}$ pins are pulled low, which turns off the regulated output(s). |
| 10 | 2NDFB/$\overline{\text{FPWM}}$ | A 12V supply can be generated using an auxiliary winding on the 5V output inductor. Feedback to control this 12V output is brought in through this pin. If the 12V supply is not required, this pin can also force the chip to operate at fixed frequency at light loads by pulling the pin low (this is the “forced-PWM” mode of operation). This will prevent the converter from operating in pulse-skipping mode. |
| 11 | ON/$\overline{\text{OFF}}$1 | This pin turns off only output #1. |
| 12 | SS1 | This provides programmable soft-start for the #1 output along with capacitor C3. |
| 13 | COMP1 | An R-C network made up of R6, C5, and C7 is connected to this pin which provides loop compensation for regulated output #1. |
| 14 | FB1 | The regulated output voltage appearing at output #1 is sensed using this pin by connecting it to the center of the output resistive divider (R1 and R2). |
| 15 | CSH1 | The sense point for the positive side of the voltage across the current sense resistor (R4) placed in series with output #1. |
| 16 | HDRV1 | The drive for the gate of the high-side switching FET used for output #1. |
| 17 | SW1 | This is the switching output drive point of the two power FETs which produce output #1. |
| 18 | CBOOT1 | The bootstrap capacitor (C8) for output #1 is returned to this point. |
| 19 | LDRV1 | The drive for the gate of the low-side switching FET (synchronous rectifier) used for output #1. |
| 20 | PGND | Connect this pin to circuit Power Ground. |
| 21 | CSL1 | The sense point for the negative side of the voltage across the current sense resistor (R4) placed in series with output #1. |
| 22 | LIN | This pin provides a low-current (50 mA max) 5V output. This output is always on, and can not be turned off by either the $\overline{\text{SD}}$ or ON/$\overline{\text{OFF}}$ pins. |
| 23 | IN | This is the connection for the main input power. |
| 24 | LDRV2 | The drive for the gate of the low-side switching FET (synchronous rectifier) used for output #2. |
| 25 | CBOOT2 | The bootstrap capacitor (C9) for output #2 is returned to this point. |
| 26 | SW2 | This is the switching output drive point of the two power FETs which produce output #2. |
| 27 | HDRV2 | The drive for the gate of the high-side switching FET used for output #2. |
| 28 | CSL2 | The sense point for the negative side of the voltage across the current sense resistor (R13) placed in series with output #2. |

## Typical Application Circuits

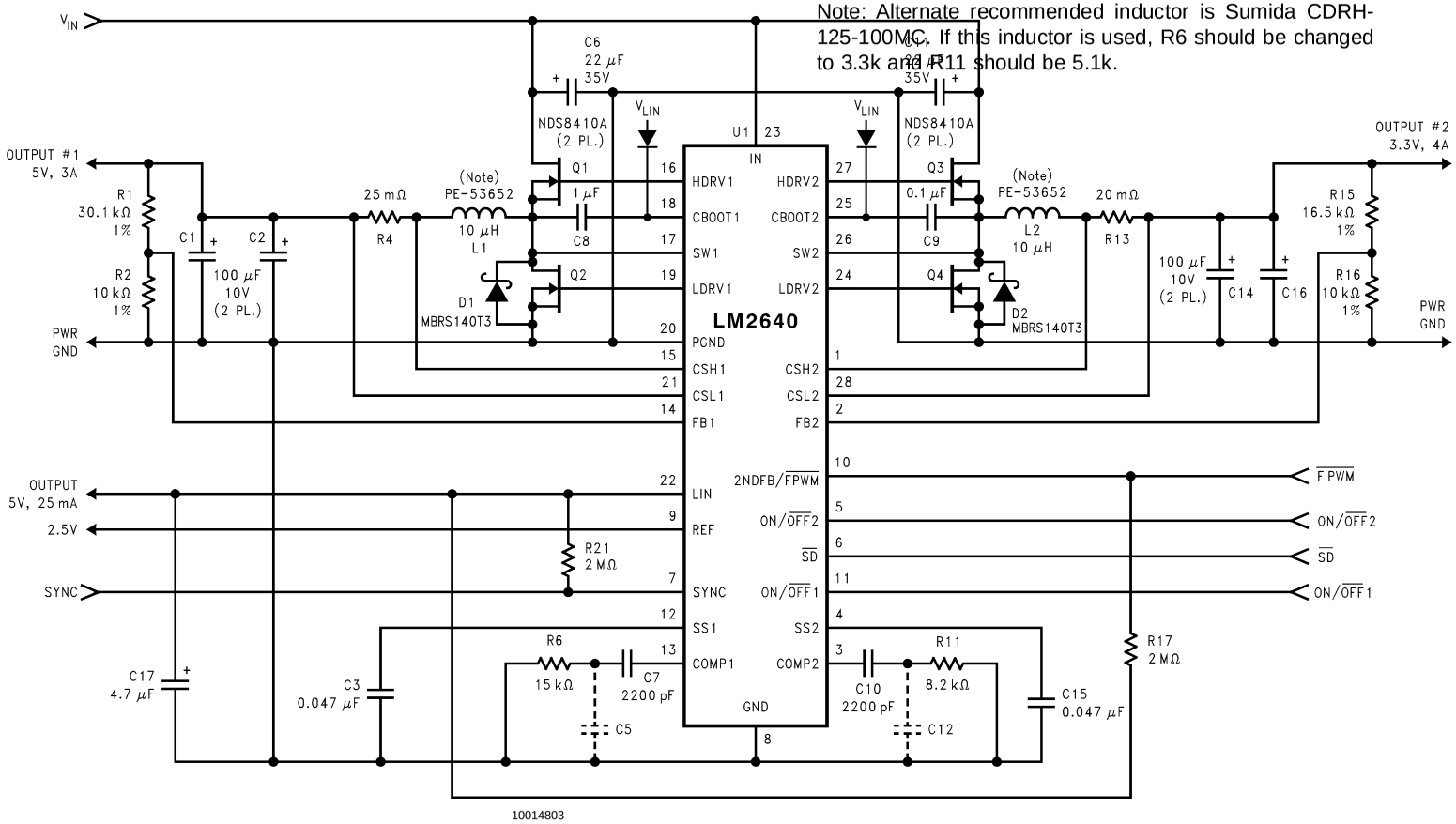



**FIGURE 1. Application With 5V/3A and 3.3V/4A Outputs**

## Typical Application Circuits (Continued)

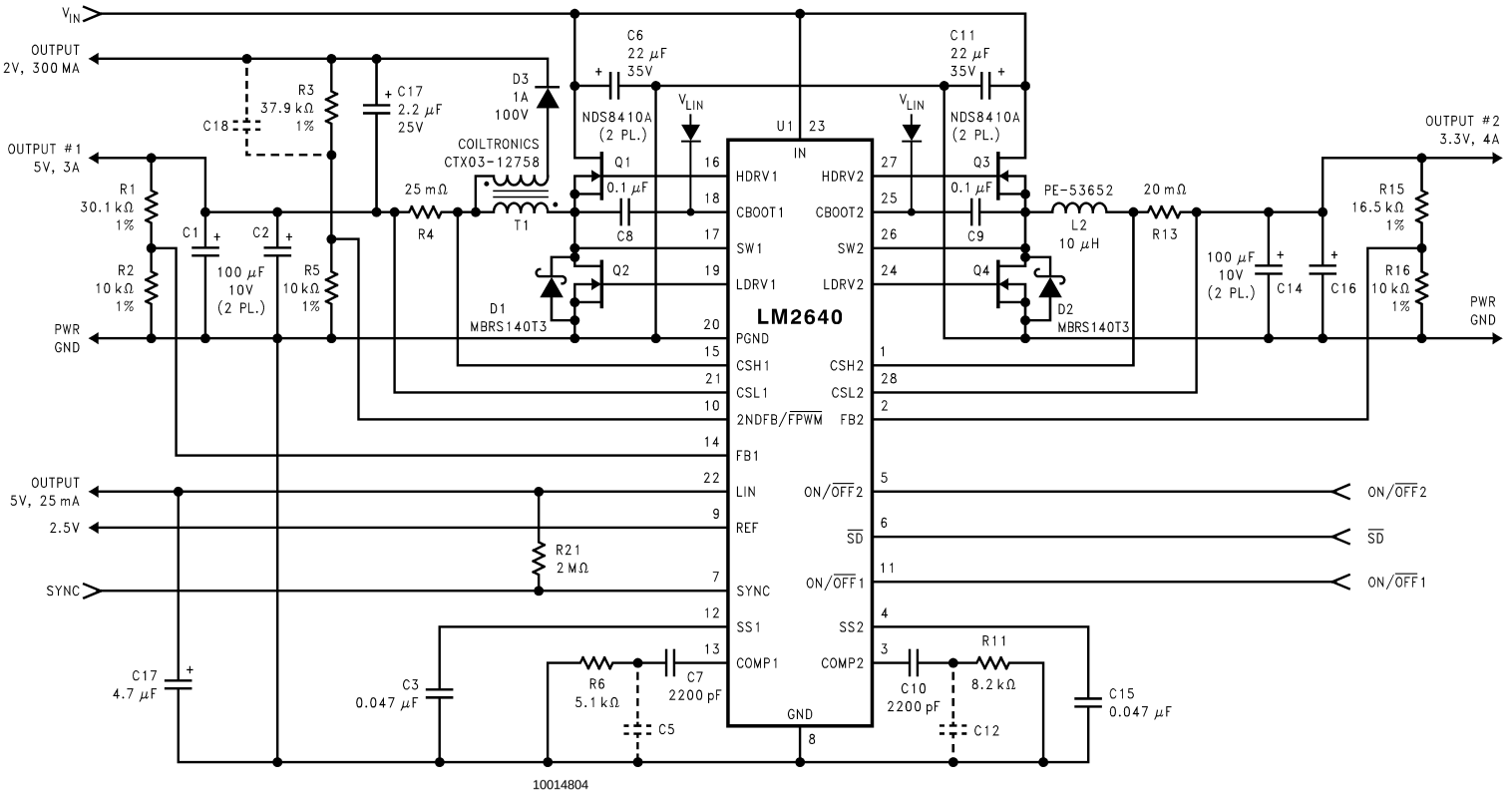



**FIGURE 2. Application With 5V/3A, 3.3V/4A, and 12V/0.3A Outputs**

## Absolute Maximum Ratings (Notes 2, 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| IN, SW1, and SW2 | −0.3 to 31V |
| FB1 and FB2 | −0.3 to 3V |
| $\overline{SD}$, ON/$\overline{OFF}$1, ON/$\overline{OFF}$2, 2NDFB/$\overline{FPWM}$, SYNC, REF, SS1, SS2, COMP1, COMP2 and CSL1 | −0.3 to ($V_{LIN}$ +0.3)V |
| LIN | −0.3 to 6V |
| CSH1, CSH2, and CSL2 | −0.3 to 7V |
| Voltage from CBOOT1 to SW1 and from CBOOT2 to SW2 | −0.3 to 5V |
| Voltage from HDRV1 to SW1 and from HDRV2 to SW2 | −0.3V |
| Voltage from CBOOT1 to HDRV1 and from CBOOT2 HDRV2 | −0.3V |
| Junction Temp. | +150˚C |
| Power Dissipation (Note 3) | 883 mW |
| Ambient Storage Temp. ($T_J$) | −65 to +150˚C |
| Soldering Dwell Time, Temp. (Note 4) | |
| Wave | 4 sec, 260˚C |
| Infrared | 10 sec, 240˚C |
| Vapor Phase | 75 sec, 219˚C |
| ESD Rating (Note 5) | 2 kV |

## Operating Ratings (Notes 1, 2)

| | |
|---|---|
| $V_{IN}$ | 5.5 to 30V |
| Junction Temp. ($T_J$) | 0 to +125˚C |

## Electrical Characteristics

Typicals and limits appearing in regular type apply for $T_J$ = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, 0 to +125˚C. Unless otherwise specified under the Parameter or Conditions columns, $V_{IN}$ = 10V, and $V_{\overline{SD}}$ = $V_{ON/\overline{OFF1}}$ = $V_{ON/\overline{OFF2}}$ = 5V. (Note 2), (Note 6) and (Note 7)

| Symbol | Parameter | Conditions | Typical | Limit | Units |
|---|---|---|---|---|---|
| **System** | | | | | |
| $V_{IN}$ | Input Supply Voltage Range | | | **5.5** | V(min) |
| | | | | **30** | V(max) |
| $V_{OUT}$ | Output Voltage Adjustment Range | | | **2.2** | V(min) |
| | | | | **6.0** | V(max) |
| $\Delta V_{OUT}/V_{OUT}$ | Load Regulation | 0 mV ≤ (CSH1-CSL1) ≤ 80 mV, 0 mV ≤ (CSH2-CSL2) ≤ 80 mV | 0.5 | | % |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line Regulation | 5.5V ≤ $V_{IN}$ ≤ 30V | 0.002 | | %/V |
| $I_{IN}$ | Input Supply Current | ON (Note 8) | 0.6 | | mA |
| | | $V_{FB1}$ = $V_{FB2}$ = 1.4V, $V_{CSH1}$ = 5.2V, $V_{CSL1}$ = 5V, $V_{CSH2}$ = 3.5V, $V_{CSL2}$ = 3.3V | | **1** | mA(max) |
| | | Standing By (Note 9) | 80 | | µA |
| | | $V_{ON/\overline{OFF1}}$ = $V_{ON/\overline{OFF2}}$ = 0V | | **150** | µA(max) |
| | | Shut Down (Note 10) | 25 | | µA |
| | | $V_{\overline{SD}}$ = 0V | | **60** | µA(max) |
| $I_{SS1}$, $I_{SS2}$ | Soft-Start Source Current | $V_{SS1}$ = $V_{SS2}$ = 1V | 4.75 | | µA |
| | | | | **2.0** | µA(min) |
| | | | | **7.0** | µA(max) |
| | Soft-Start Sink Current | | 10 | | µA |
| $V_{PCL}$ | Positive Current Limit Voltage (Voltage from CSH1 to CSL1 and from CSH2 to CSL2) | | 100 | | mV |
| | | | | **80** | mV(min) |
| | | | | **140** | mV(max) |
| | | −40˚C ≤ $T_J$ ≤ +125˚C | 100 | **75** | mV(min) |
| $V_{NCL}$ | Negative Current Limit Voltage (Voltage from CSH1 to CSL1 and from CSH2 to CSL2) | $V_{2NDFB/\overline{FPWM}}$ = 0.8V | −100 | | mV |
| | | | | **−80** | mV(min) |
| | | | | **−140** | mV(max) |

## Electrical Characteristics (Continued)

Typicals and limits appearing in regular type apply for $T_J$ = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, 0 to +125˚C. Unless otherwise specified under the Parameter or Conditions columns, $V_{IN}$ = 10V, and $V_{\overline{SD}}$ = $V_{ON/\overline{OFF1}}$ = $V_{ON/\overline{OFF2}}$ = 5V. (Note 2), (Note 6) and (Note 7)

| Symbol | Parameter | Conditions | Typical | Limit | Units |
|---|---|---|---|---|---|
| | $V_{OUT}$ Undervoltage Shutdown Latch Threshold | | 70 | | % |
| | | | | 60 | %(min) |
| | | | | 80 | %(max) |
| | $V_{OUT}$ Overvoltage Shutdown Latch Threshold | | 150 | | % |
| | | | | 135 | %(min) |
| | | | | 165 | %(max) |
| | Secondary Feedback Threshold Voltage (2NDFB/FPWM) | | 2.5 | | V |
| | | | | **2.4** | V(min) |
| | | | | **2.6** | V(max) |
| | (2NDFB/FPWM) Pin Pull-Up Current | $V_{\overline{SD}}$ = 2.4V<br>$V_{ON/\overline{OFF1}}$ = 0V<br>$V_{ON/\overline{OFF2}}$ = 2.4V | 40 | 80 | µA(max) |
| | (2NDFB/FPWM) Pin Input Leakage Current | $V_{\overline{SD}}$ = 2.4V<br>$V_{ON/\overline{OFF1}}$ = 0V<br>$V_{ON/\overline{OFF2}}$ = 2.4V | ±0.1 | | µA |
| **Gate Drive** | | | | | |
| $V_{BOOT}$ | Bootstrap Voltage (Voltage from CBOOT1 to SW1 and from CBOOT2 to SW2) | CBOOT1 and CBOOT2 Source 1 µA Each | 4.5 | | V |
| | | | | 4.3 | V(min) |
| | HDRV1 and HDRV2 Sink and Source Current | | 0.35 | | A |
| | LDRV1 and LDRV2 Sink and Source Current | | 0.35 | | A |
| | HDRV1 and HDRV2 High-Side On-Resistance | $V_{CBOOT1}$ = $V_{CBOOT2}$ = 5V, $V_{SW1}$ = $V_{SW2}$ = 0V | 6 | | Ω |
| | HDRV1 and HDRV2 Low-Side On-Resistance | $V_{CBOOT1}$ = $V_{CBOOT2}$ = 5V, $V_{SW1}$ = $V_{SW2}$ = 0V | 4 | | Ω |
| | LDRV1 and LDRV2 High-Side On-Resistance | $V_{LIN}$ = 5V | 8 | | Ω |
| | LDRV1 and LDRV2 Low-Side On-Resistance | $V_{LIN}$ = 5V | 4 | | Ω |
| **Oscillator** | | | | | |
| $F_{OSC}$ | Oscillator Frequency | | 200 | | kHz |
| | | | | **170** | kHz(min) |
| | | | | **230** | kHz(max) |
| | | −40˚C ≤ $T_J$ ≤ +125˚C | 200 | **160** | kHz(min) |
| | | | | **230** | kHz(max) |
| | Minimum OFF-Time | $V_{FB1}$ = 1V, Measured at HDRV1 | 250 | | ns |
| | | | | **350** | ns(max) |
| | Maximum Frequency of Synchronization | | | 400 | kHz(min) |
| | Minimum Width of Synchronization Pulses | SYNC Pulses are Low-Going | | 200 | ns(min) |
| **Error Amplifier** | | | | | |
| $I_{FB1}$, $I_{FB2}$ | Feedback Input Bias Current | $V_{FB1}$ = $V_{FB2}$ = 1.4V | 100 | | nA |
| | | | | **250** | nA(max) |
| | | $V_{FB1}$ = $V_{FB2}$ = 1.4V<br>−40˚C ≤ $T_J$ ≤ +125˚C | 100 | **360** | nA(max) |

## Electrical Characteristics (Continued)

Typicals and limits appearing in regular type apply for $T_J$ = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, 0 to +125˚C. Unless otherwise specified under the Parameter or Conditions columns, $V_{IN}$ = 10V, and $V_{\overline{SD}} = V_{ON/\overline{OFF1}} = V_{ON/\overline{OFF2}}$ = 5V. (Note 2), (Note 6) and (Note 7)

| Symbol | Parameter | Conditions | Typical | Limit | Units |
|---|---|---|---|---|---|
| $I_{COMP1}$, $I_{COMP2}$ | COMP Output Source Current | $V_{FB1} = V_{FB2}$ = 1V, $V_{COMP1} = V_{COMP2}$ = 1V | 90 | | µA |
| | | | | 40 | µA(min) |
| $I_{COMP1}$, $I_{COMP2}$ | COMP Output Sink Current | $V_{FB1} = V_{FB2}$ = 1.4V, $V_{COMP1} = V_{COMP2}$ = 0.2V | 60 | | µA |
| | | | | 40 | µA(min) |
| **Voltage References and Linear Voltage Regulator** | | | | | |
| $V_{BG}$ | Bandgap Voltage | | 1.238 | | V |
| $V_{REF}$ | Reference Voltage | 0.01 mA ≤ $I_{REF}$ ≤ 5 mA Source, $V_{LIN}$ ≤ 6V | 2.5 | | V |
| | | | | **2.45** | V(min) |
| | | | | **2.55** | V(max) |
| | | 0.01 mA ≤ $I_{REF}$ ≤ 5 mA Source, $V_{LIN}$ ≤ 6V, −40˚C ≤ $T_J$ ≤ +125˚C | 2.5 | **2.45** | V(min) |
| | | | | **2.555** | V(max) |
| $V_{LIN}$ | Output Voltage of the Linear Voltage Regulator | 6V ≤ $V_{IN}$ ≤ 30V, 0 mA ≤ $I_{LIN}$ ≤ 25 mA | 5 | | V |
| | | | | **4.6** | V(min) |
| | | | | **5.4** | V(max) |
| $V_{UVLO}$ | Undervoltage Lockout Threshold | (Note 11) | 4.0 | | V |
| | | | | **3.6** | V(min) |
| | | | | **4.4** | V(max) |
| | | (Note 11) −40˚C ≤ $T_J$ ≤ +125˚C | 4.0 | **3.6** | V(min) |
| | | | | **4.42** | V(max) |
| | LIN-to-$V_{OUT}$ Switch-Over Threshold | $V_{OUT}$ taken at CSL1 | 4.8 | | V |
| **Logic Inputs** | | | | | |
| $V_{IH}$ | Minimum High Level Input Voltage ($\overline{SD}$, ON/$\overline{OFF}$1, ON/$\overline{OFF}$2, and SYNC) | | | **2.4** | V(min) |
| | | −40˚C ≤ $T_J$ ≤ +125˚C | | **2.45** | V(min) |
| $V_{IH}$ | Minimum High Level Input Voltage (2NDFB/$\overline{FPWM}$) | | | **2.6** | V(min) |
| $V_{IL}$ | Maximum Low Level Input Voltage ($\overline{SD}$, ON/$\overline{OFF}$1, ON/$\overline{OFF}$2, SYNC, and 2NDFB/$\overline{FPWM}$) | | | **0.8** | V(max) |
| | Maximum Input Leakage Current ($\overline{SD}$, ON/$\overline{OFF}$1, ON/$\overline{OFF}$2, and SYNC) | Logic Input Voltage 0 or 5V | ±0.1 | | µA |

**Note 1:** Unless otherwise specified, all voltages are with respect to the voltage at the GND and PGND pins.

**Note 2:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

**Note 3:** The Absolute Maximum power dissipation depends on the ambient temperature. The 883 mW rating results from substituting 150˚C, 70˚C, and 90.6˚C/W for $T_{Jmax}$, $T_A$, and $\theta_{JA}$ respectively into the formula $P_{max} = (T_{Jmax} - T_A)/\theta_{JA}$, where $P_{max}$ is the Absolute Maximum power dissipation, $T_{Jmax}$ is the Absolute Maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance of the package. A $\theta_{JA}$ of 90.6˚C/W represents the worst-case condition of no heat sinking of the 28-pin TSSOP. Heat sinking allows the safe dissipation of more power. The Absolute Maximum power dissipation must be derated by 11.04 mW per ˚C above 70˚C ambient. The LM2640 actively limits its junction temperature to about 150˚C.

**Note 4:** For detailed information on soldering plastic small-outline packages, refer to the Packaging Databook available from National Semiconductor Corporation.

**Note 5:** For testing purposes, ESD was applied using the human-body model, a 100 pF capacitor discharged through a 1.5 kΩ resistor.

**Note 6:** A typical is the center of characterization data taken with $T_A = T_J$ = 25˚C. Typicals are not guaranteed.

**Note 7:** All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with $T_A$ = 25˚C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

## Electrical Characteristics (Continued)

**Note 8:** Both controllers are ON but not switching. Currents entering the IC at IN, CSL1, CSH1, CSL2, and CSH2 are measured. Those entering at CSL1 and CSH1 are multiplied by 0.50 to emulate the effect of a switching conversion from 10V down to 5V. Those entering at CSL2 and CSH2 are multiplied by 0.33 to emulate the effect of a switching conversion from 10V down to 3.3V. After multiplication, all five currents are added. Because the voltage at the CSL1 input is greater than the LIN-to-$V_{OUT}$ switchover threshold, most of the input supply current enters the IC via the CSL1 input.

**Note 9:** Both switching controllers are OFF. The 5V, 50 mA linear regulator (output at LIN) and the precision 2.5V reference (output at REF) remain ON.

**Note 10:** Both switching controllers and the 2.5V precision reference are OFF. The 5V, 50 mA linear regulator remains ON.

**Note 11:** The controllers remain OFF until the voltage of the 5V, 50 mA linear regulator (output at LIN) reaches this threshold.

## Block Diagram

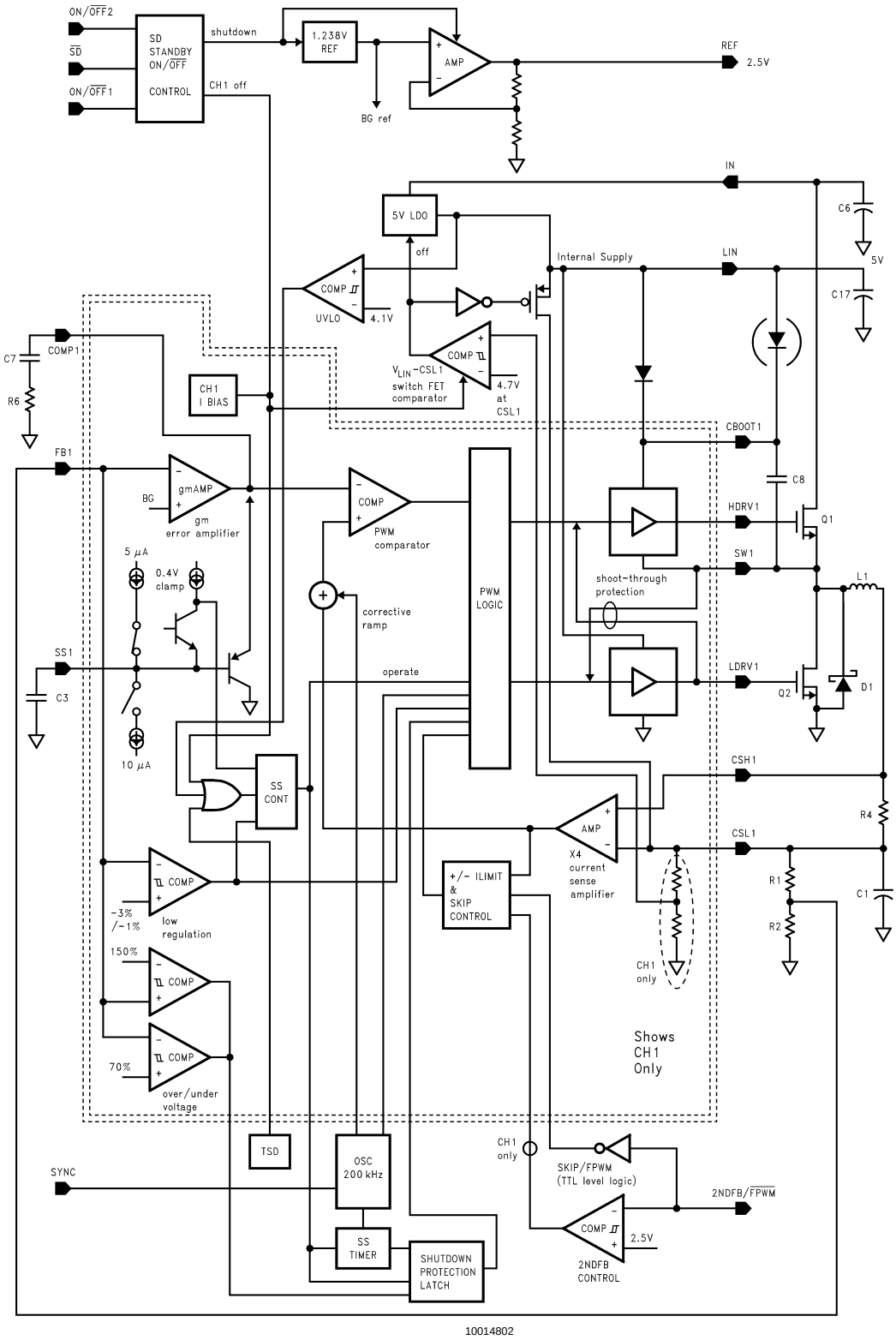
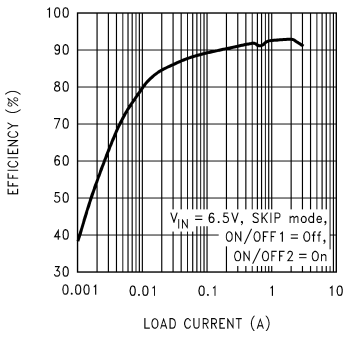



**FIGURE 3. LM2640 Block Diagram**

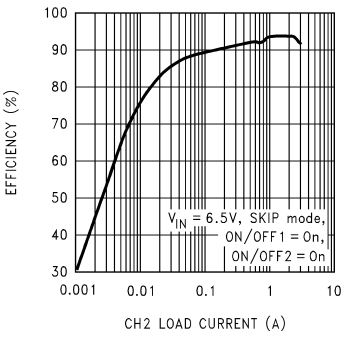
## Typical Performance Characteristics

**Efficiency vs Load Current**



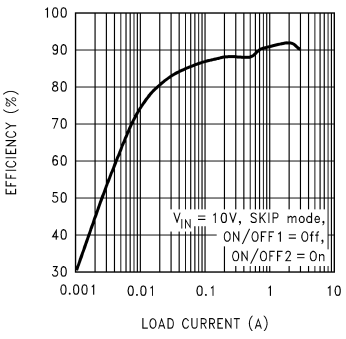

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**Efficiency vs Load Current**



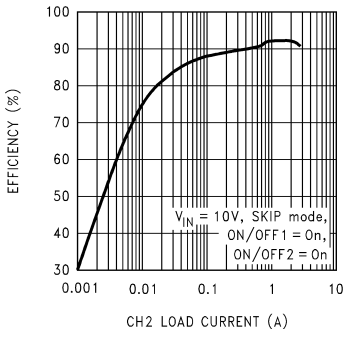

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**Efficiency vs Load Current**



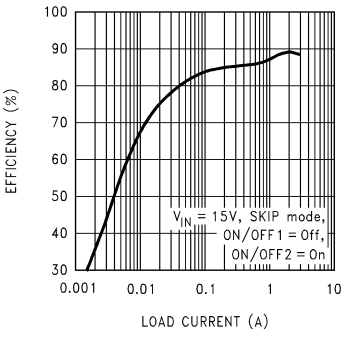

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**Efficiency vs Load Current**



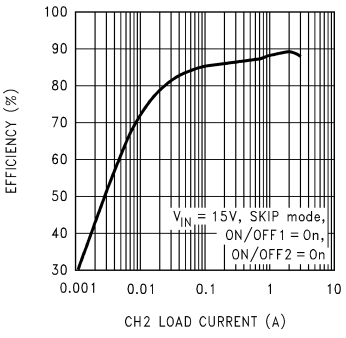

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**Efficiency vs Load Current**



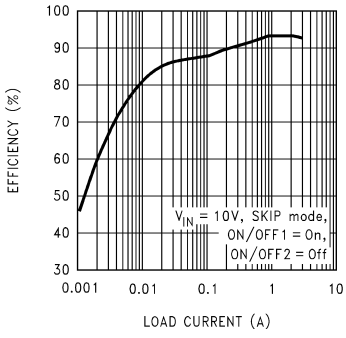

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**Efficiency vs Load Current**



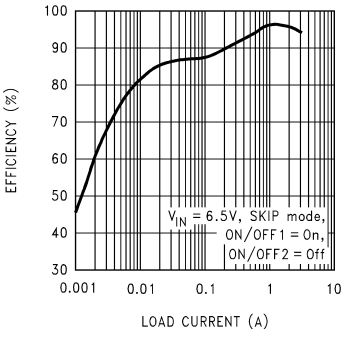

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**Efficiency vs Load Current**



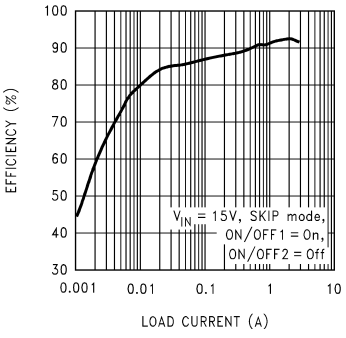

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**Efficiency vs Load Current**



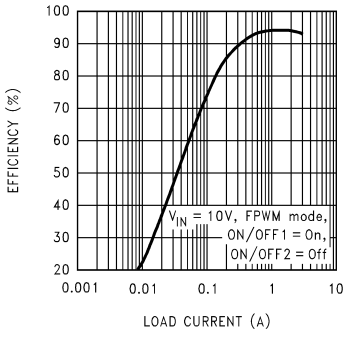

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**Efficiency vs Load Current**



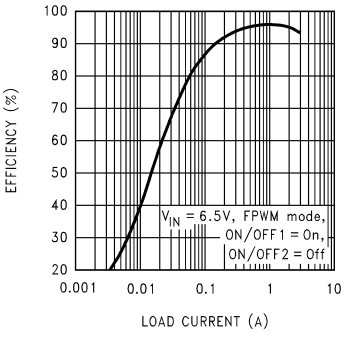

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**Efficiency vs Load Current**



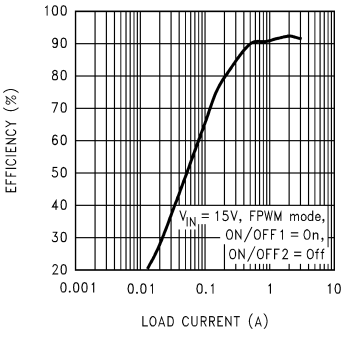

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**Efficiency vs Load Current**




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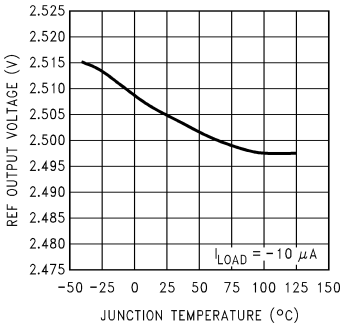
**Efficiency vs Load Current**




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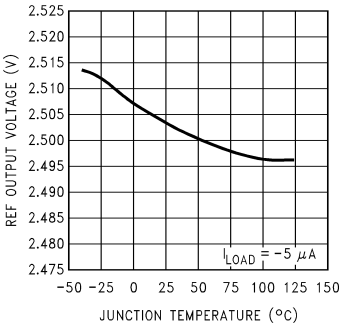
## Typical Performance Characteristics (Continued)

**REF Output Voltage**



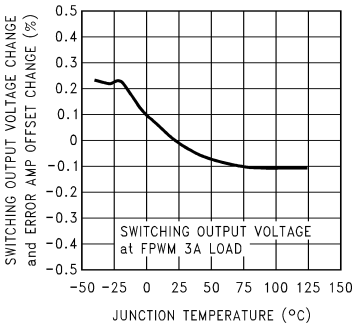

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**REF Output Voltage**



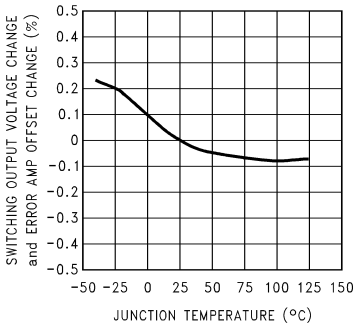

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**Normalized Switching Output Voltage vs Junction Temperature**



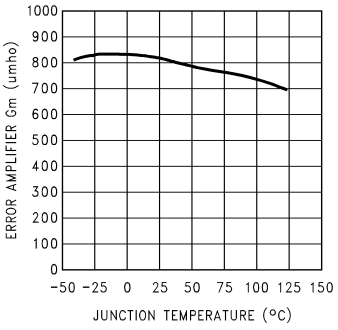

10014828

**Normalized Error Amplifier Offset vs Junction Temperature**



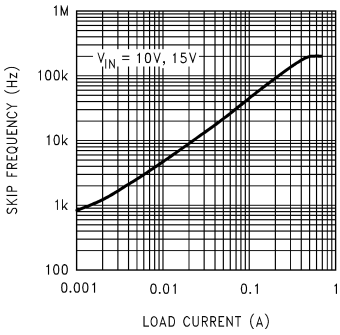

10014829

**Error Amplifier Gm vs Junction Temperature**



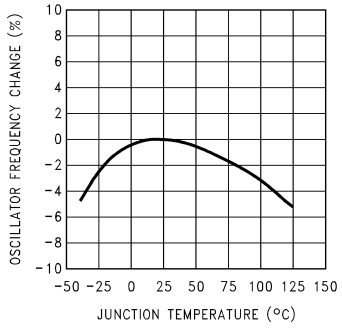

10014830

**CH1 Skip Frequency vs Load Current**



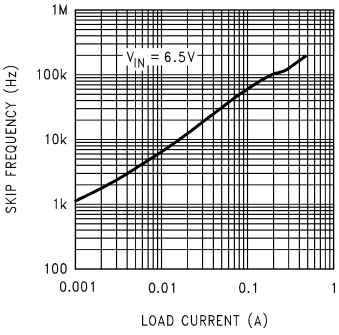

10014831

**Normalized Oscillator Frequency vs. Junction Temperature**



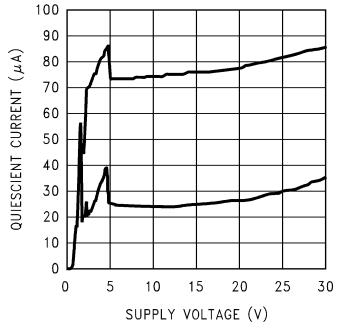

10014832

**CH1 Skip Frequency vs Load Current**




10014833

**Shutdown Quiescent Current And Standby Quiescent Current vs Supply Voltage**




10014834

# Theory of Operation

### Basic Operation of the Current-Mode Controller

The output voltage is held at a constant value by the main control loop, which is made up of the *error amplifier*, the *current sense amplifier*, and the *PWM comparator* (refer to the Block Diagram, *Figure 3*).

The LM2640 controller has two primary modes of operation: *Forced Pulse-Width Modulation (FPWM)* where the controller always operates at a fixed frequency, and *Pulse-Skipping* mode where the controller frequency decreases at reduced output loads to improve light-load efficiency.

### FPWM Mode of Operation

Pulling the FPWM pin low initiates a mode of operation called Forced Pulse-Width Modulation (FPWM). This means that the LM2640 will *always* operate at a fixed frequency, regardless of output load. The cycle of operation is:

The high-side FET switch turns ON at the beginning of every clock cycle, causing current to flow through the inductor. The inductor current ramps up, causing a voltage drop across the sense resistor, and this voltage is amplified by the current sense amplifier.

The voltage signal from the current sense amplifier is applied to the input of the PWM comparator, where it is compared to the control level set by the error amplifier. Once the current sense signal reaches this control voltage, the PWM comparator resets the driver logic which turns OFF the high-side FET switch.

The low-side FET switch turns on after a delay time which is the lesser of either:

(a) The time it takes the SW pin voltage to reach zero (this voltage is sensed by the shoot-through protection circuitry).

(b) 100 ns, which is the pre-set value for maximum delay.

When operating at very light loads (in FPWM mode), the inductor current must flow in a negative direction through the low-side FET switch in order to maintain the fixed-frequency mode of operation. For this reason, the built-in zero cross detector is disabled when ever FPWM mode is activated (that is, when ever the FPWM pin is pulled to a low state).

It should be noted that if the FPWM pin is high (operation described in next section), the zero cross detector will turn OFF the low-side FET switch anytime the inductor current drops to zero (which prevents negative inductor current).

### Pulse-Skipping Mode of Operation

Pulling the FPWM pin high allows the LM2640 to operate in pulse-skipping mode at light loads, where the switching frequency decreases as the output load is reduced. The controller will operate in fixed-frequency mode, as described in the previous section, if the output load current is sufficiently high.

Pulse-skipping results in higher efficiency at light loads, as decreasing the switching frequency reduces switching losses. The load current value where the transition from fixed-frequency to pulse-skipping operation occurs is the point where the inductor current goes low enough to cause the voltage measured across the current sense resistor (R4 or R13) to drop below 25 mV.

In pulse-skipping mode, the high-side FET switch will turn ON at the beginning of the first clock cycle which occurs after the voltage at the feedback pin falls below the reference voltage. The high-side FET switch remains ON until the voltage across the current sense resistor rises to 25 mV (and then it turns OFF).

### Ramp Compensation

All current-mode controllers require the use of ramp compensation to prevent subharmonic oscillations, and this compensation is built into the LM2640. The internal compensation assumes an $R_{SENSE}$ value of 25 mΩ, inductor value of 10 µH, and a maximum output voltage of 6V.

To prevent oscillations, the slope M of the compensation ramp must be equal to the maximum downward slope of the voltage waveform at the output of the current sense amplifier. The relationship of the slope M to the external components is given by:

$M_{COMP} = M_{CS\ AMP}$ (max) = N X $R_{SENSE}$ X $V_{OUT}$ (max) / L

Where:

$M_{COMP}$ is the slope of the compensation ramp.

$M_{CS\ AMP}$(max) is the maximum downward slope of the voltage at the output of the current sense amplifier.

N is the gain of the current sense amplifier.

$R_{SENSE}$ is the value of the current sense resistor.

$V_{OUT}$ (max) is the maximum output voltage.

L is the inductance of the output inductor.

It is important to note that since the value $R_{SENSE}$ appears in the numerator and L is in the denominator, these two values may be increased or decreased at the same ratio without changing the slope.

At higher values of load current, a lower value $R_{SENSE}$ will be selected. The inductance value for the output inductor should be decreased by the same percentage to maintain correct ramp compensation.

# Application Information

### Improved Transient Response

If the output voltage falls below 97% of the nominal value, the low-voltage regulation (LREG) comparator will activate logic which turns ON the high-side FET switch continuously until the output returns to nominal. The low-side FET switch is held OFF during this time.

This action will improve transient response since it bypasses the error amplifier and PWM comparator, forcing the high-side switch ON until the output returns to nominal. This feature is disabled during start-up.

### Boost High-Side Gate Drive

A “flying” bootstrap capacitor is used to generate the gate drive voltage used for the high-side FET switch. This bootstrap capacitor is charged up to about 5V using an internal supply rail and diode when ever the low-side FET switch is ON. When the high-side FET switch turns ON, the Source is pulled up near the input voltage. The voltage across the bootstrap capacitor boosts up the gate drive voltage, ensuring that the Gate is driven at least 4.3V higher than the Source.

### Reference

The internal bandgap reference is used to generate a 2.5V reference voltage which is connected to the REF pin. The guaranteed tolerance of the REF voltage is ±2% over the full operating temperature range, as long as the current drawn is ≤ 5 mA.

A bypass capacitor on the REF pin is not required, but may be used to reduce noise.

## Application Information (Continued)

### 5V LIN Output

The LM2640 contains a built-in 5V/50 mA LDO regulator whose output is connected to the LIN pin. Since this is an LDO regulator, it does require an external capacitor to maintain stability. The minimum amount of capacitance required for stability is 4.7 µF, with ESR in the range of about 100 mΩ to 3Ω. A good quality solid Tantalum capacitor is recommended (ceramics can not be used because the ESR is too low). If cold temperature operation is required, a capacitor must be selected which has an ESR that is in the stable range over the entire operating temperature range of the application.

Since the current limit for this LDO regulator is set at about 85 mA, it can be used at load currents up to about 50 mA (assuming total IC power dissipation does not exceed the maximum value).

Guaranteed specifications are provided for worst-case values of $V_{LIN}$ over the full operating temperature range for load currents up to 25 mA (see Electrical Characteristics). To estimate how the $V_{LIN}$ output voltage changes when going from $I_{LIN}$ = 25 mA to $I_{LIN}$ = 50 mA, a change in $V_{LIN}$ of about −30 mV should be expected due to loading (typical value only, not guaranteed). This decrease in $V_{LIN}$ is linear with increasing load current.

It must be understood that the maximum allowable current of 50mA must include the current drawn by the gate drive circuitry. This means that the maximum current available for use at the LIN pin is 50 mA minus whatever is being used internally for gate drive.

The amount of current used for gate drive by each switching output can be calculated using the formula:

$$I_{GD} = 2 \times Q \times F_{OSC}$$

Where:

$I_{GD}$ is the gate drive current supplied by $V_{LIN}$.

Q is the gate charge required by the selected FET (see FET data sheet: Gate Charge Characteristics).

$F_{OSC}$ is the switching frequency.

Example: As shown in the typical application, if the FET NDS8410 is used with the LM2640, the turn-on gate voltage ($V_{GS}$) is 5V − $V_{DIODE}$ = 4.3V. Referring to the NDS8410 data sheet, the curve Gate Charge Characteristics shows that the gate charge for this value of $V_{GS}$ is about 24 nC.

Assuming 200 kHz switching frequency, the gate drive current used by each switching output is:

$$I_{GD} = 2 \times Q \times F_{OSC}$$
$$= 2 \times (24 \times 10^{-9}) \times (2 \times 10^{5})$$
$$= 9.6 \text{ mA}$$

If both outputs are switching, the total gate drive current drawn would be twice this (19.2 mA).

Note that in cases where the voltage at switching output #1 is 4.8V or higher, the internal gate drive current is obtained from that output (which means the full 50 mA is available for external use at the LIN pin).

### SYNC Pin

The basic operating frequency of 200 kHz can be increased to up to 400 kHz by using the SYNC pin and an external CMOS or TTL clock. The synchronizing pulses must have a minimum pulse width of 200 ns.

If the sync function is not used, the SYNC pin must be connected to the LIN pin or to ground to prevent false triggering.

### Current Limit Circuitry

The LM2640 is protected from damage due to excessive output current by an internal current limit comparator, which monitors output current on a cycle-by-cycle basis. The current limiter activates when ever the absolute magnitude of the voltage developed across the output sense resistor exceeds 100 mV (positive or negative value).

If the sensed voltage exceeds 100 mV, the high-side FET switch is turned OFF. If the sensed voltage goes below -100 mV, the low-side FET switch is turned OFF. It should be noted that drawing sufficient output current to activate the current limit circuits can cause the output voltage to drop, which could result in a under-voltage latch-OFF condition (see next section).

### Under-voltage/Over-voltage Protection

The LM2640 contains protection circuitry which activates if the output voltage is too low (UV) or too high (OV). In the event of either a UV or OV fault, the LM2640 is latched off and the high-side FET is turned off, while the low-side FET is turned on.

If the output voltage drops below 70% of nominal value, the under-voltage comparator will latch OFF the LM2640. To restore operation, power to the device must be shut off and then restored.

It should be noted that the UV latch provides protection in cases where excessive output current forces the output voltage down. The UV latch circuitry is disabled during start-up.

If the output voltage exceeds 150% of nominal, the over-voltage comparator latches off the LM2640. As stated before, power must be cycled OFF and then ON to restore operation.

It must be noted that the OV latch can not protect the load from damage in the event of a high-side FET switch failure (where the FET shorts out and connects the input voltage to the load).

Protection for the load in the event of such a failure can be implemented using a fuse in the power lead. Since the low-side FET switch turns ON whenever the OV latch activates, this would blow a series fuse if the FET and fuse are correctly sized.

### Soft-Start

An internal 5 µA current source connected to the soft-start pins allows the user to program the turn-on time of the LM2640. If a capacitor is connected to the SS pin, the voltage at that pin will ramp up linearly at turn ON. This voltage is used to control the pulse widths of the FET switches.

The pulse widths start at a very narrow value and linearly increase up to the point where the SS pin voltage is about 1.3V. At that time, the pulse-to-pulse current limiter controls the pulse widths until the output reaches its nominal value (and the PWM current-mode control loop takes over).

The LM2640 contains a digital counter (referenced to the oscillator frequency) that times the soft-start interval. The maximum allotted SS time period is 4096 counts of the oscillator clock, which means the time period varies with oscillator frequency:

$$\text{max. allowable SS interval} = 4096 / F_{OSC}$$

## Application Information (Continued)

If the output voltage does not move to within −1% of nominal in the period of 4096 counts, the device will latch OFF. To restore operation, the power must be cycled OFF to ON.

**Minimum Pulse Width**

As the input voltage is increased, the pulse widths of the switching FET's decreases. If the pulse widths become narrower than 350 ns, pulse jitter may occur as the pulses alternate with slightly different pulse widths. This is does not affect regulator stability or output voltage accuracy.

**Start-Up Issues**

The LM2641 contains an output undervoltage protection circuit which is made up of a digital counter and a comparator which monitors $V_{OUT}$. During turn-on, the counter begins counting clock cycles when the input voltage reaches approximately 3V. If the counter reaches 4096 cycles before the output voltage rises to within 1% of nominal value, the IC will be latched off in an undervoltage fault condition.

The function of this protection is to shut the regulator off if the output is overloaded (such as a short to ground). However, the UV latch can cause start-up problems if the circuit is not properly designed. The following two sections explain how to avoid these types of problems:

**Input Voltage Rise Time**

If the input voltage rises too slowly, the LM2641 will latch off in an undervoltage condition. To avoid this problem, the input voltage must rise quickly enough to allow the output to get into regulation before the 4096 count time interval elapses. For a switching frequency of 300 kHz, 4096 cycles will be completed in 13.6 milliseconds.

In reality, the total rise time of $V_{IN}$ should not approach the 4096 clock cycle limit if reliable start-up is to be assured. It should be noted that the total rise time of $V_{IN}$ is also affected by current loading when the power converter begins switching (which draws power from the input capacitors) causing their voltage to sag (details of input capacitor requirements are outlined in the next section).

It is also important to note that this type of start-up problem is more likely to occur at higher values of output voltage, since the input voltage must rise to a higher voltage to allow the output voltage to regulate (which means the input dV/dt rate has to be faster). The recommended output voltage limit of 6V should not be exceeded.

**Input Capacitance**

The amount and type of input capacitance present is directly related to how well the regulator can start up. The reason is that the input capacitors serve as the source of energy for the power converter when the regulator begins switching. Typically, the input voltage (which is the voltage across the input capacitors) will sag as the power converter starts drawing current which will cause a dip in $V_{IN}$ as it is ramping up. If the input capacitors are too small or have excessive ESR, the input volatge may not be able to come up fast enough to allow the output volatge to get into regulation before the digital clock counts off 4096 cycles and the part will latch off as an undervoltage fault.

To prevent this type of start-up problem:

1. The input capacitors must provide sufficient bulk capacitance and have low impedance. Solid Tantalum capacitors designed for high-frequency switching applications are recommended as they generally provide the best cost/performance characteristics and maintain a very low ESR even at cold temperatures. Ceramic capacitors also have very low ESR over the full temperature range, but X5R/X7R dielectric types should be used to assure sufficient capacitance will be provided (Z5U or Y5F types are not suitable).

   Some of the newer electrolytic types such as POSCAP, OSCON, and polymer electrolytic may also be usable as input capacitors. However, care must be taken if the application will be used at low temperatures as the ESR of these capacitors may increase significantly at temperatures below 0˚C. Most aluminum electrolytes are not usable with this IC at temperatures below this limit. Check the ESR specifications of the selected capacitor carefully if low temperature operation will be required.
2. The input capacitors must be physically located not more than one centimeter away from the switching FET's, as trace inductance in the switching current path can cause problems.

**Loop Compensation**

The LM2640 must be properly compensated to assure stable operation and good transient response. As with any control loop, best performance is achieved when the compensation is optimized so that maximum bandwidth is obtained while still maintaining sufficient phase margin for good stability.

Best performance for the LM2640 is typically obtained when the loop bandwidth (defined as the frequency where the loop gain equals unity) is in the range of $F_{OSC}/10$ to $F_{OSC}/5$.

In the discussion of loop stability, it should be noted that there is a high-frequency pole $f_p(HF)$, whose frequency can be approximated by:

$f_p(HF) \sim F_{OSC}/2 \times Q_S$ (Assumes $Q_S < 0.5$)

Where:

$$Q_S = \frac{2}{\pi\left(1 + 2\left(\frac{6 - V_{OUT}}{V_{IN}}\right)\right)}$$

As can be seen in the approximation for $Q_S$, the highest frequency for $f_p(HF)$ occurs at the maximum value of $V_{IN}$. The lowest frequency for $f_p(HF)$ is about $F_{OSC}/10$ (when $V_{IN}$= 4.5V and $V_{OUT}$ = 1.8V).

As noted above, the location of the pole $f_p(HF)$ is typically in the range of about $F_{OSC}/10$ to $F_{OSC}/4$. This pole will often be near the unity-gain crossover frequency, and it can significantly reduce phase margin if left uncompensated. Fortunately, the ESR of the output capacitor(s) forms a zero which is usually very near the frequency of $f_p(HF)$, and provides cancellation of the negative phase shift it would otherwise cause. For this reason, the output capacitor must be carefully selected.

Most of the loop compensation for the LM2640 is set by an R-C network from the output of the error amplifier to ground (see *Figure 4*). Since this is a transconductance amplifier, it has a very high output impedance (160 kΩ).

## Application Information (Continued)

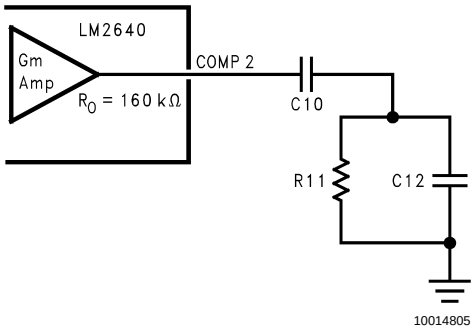



**FIGURE 4. Typical Compensation Network**

The components shown will add poles and zeros to the loop gain as given by the following equations:

C10 adds a pole whose frequency is given by:

$f_p(C10) = 1 / [2\pi \times C10 (R11 + 160k)]$

C12 adds a pole whose frequency is given by:

$f_p(C12) = 1 / [2\pi \times C12 (R11 \parallel 160k)]$

R11 adds a zero whose frequency is given by:

$f_z(R11) = 1 / [2\pi \times R11 (C10 + C12)]$

The output capacitor adds both a pole and a zero to the loop:

$f_p(C_{OUT}) = 1 / [2\pi \times R_L \times C_{OUT}]$

$f_z(ESR) = 1 / [2\pi \times ESR \times C_{OUT}]$

Where $R_L$ is the load resistance, and ESR is the equivalent series resistance of the output capacitor(s).

The function of the compensation components will be explained in a qualitative discussion of a typical loop gain plot for an LM2640 application, as illustrated in *Figure 5*.

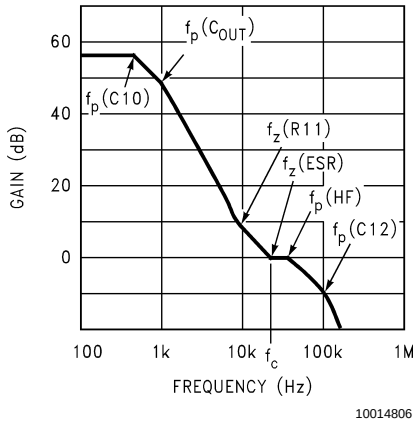



**FIGURE 5. Typical Loop Gain Plot**

C10 and R11 form a pole and a zero. Changing the value of C10 moves the frequency of both the pole and the zero. Changing R11 moves the zero without significantly affecting the pole.

The C10 pole is typically referred to as the dominant pole, and its primary function is to roll off loop gain and reduce the bandwidth.

The R11 zero is required to add some positive phase shift to offset some of the negative phase shift from the two low-frequency poles. Without this zero, these two poles would cause −180° of phase shift at the unity-gain crossover, which is clearly unstable. Best results are typically obtained if R11 is selected such that the frequency of $f_z(R11)$ is in the range of $f_c/4$ to $f_c$ where $f_c$ is the unity-gain crossover frequency.

The output capacitor (along with the load resistance $R_L$) forms a pole shown as $f_p(C_{OUT})$. Although the frequency of this pole varies with $R_L$, the loop gain also varies proportionally which means the unity-gain crossover frequency stays essentially constant regardless of $R_L$ value.

C12 can be used to create an additional pole most often used for bypassing high-frequency switching noise on the COMP pin. In many applications, this capacitor is unnecessary.

If C12 is used, best results are obtained if the frequency of the pole is set in the range $F_{OSC}/2$ to $2F_{OSC}$. This will provide bypassing for the high-frequency noise caused by switching transitions, but add only a small amount of negative phase shift at the unity-gain crossover frequency.

The ESR of $C_{OUT}$ (as well as the capacitance of $C_{OUT}$) form the zero $f_z(ESR)$, which typically falls somewhere between 10 kHz and 50 kHz. This zero is very important, as it cancels phase shift caused by the high-frequency pole $f_p(HF)$. It is important to select $C_{OUT}$ with the correct value of capacitance and ESR to place this zero near $f_c$ (typical range $f_c/2$ to $f_c$).

As an example, we will present an analysis of the loop gain plot for the 3.3V output shown in the Typical Application Circuit. Values used for calculations are:

$V_{IN}$ = 12V

$V_{OUT}$ = 3.3V @ 4A

$C_{OUT}$ = C14 + C16 = 200 µF

ESR = 60 mΩ(each) = 30 mΩ total

$F_{OSC}$ = 200 kHz

$f_p(HF) \sim 40$ kHz

R13 = 20 mΩ

L2 = 10 µH

$R_L$ = 0.825Ω

DC gain = 55 dB

The values of compensation components will be: C10 = 2200 pF, R11 = 8.2k, and C12 will not be used. Using this data, the poles and zeros are calculated:

$f_p(C10) = 1 / [2\pi \times C10 (R11 + 160k)] = 430$ Hz

$f_z(R11) = 1 / [2\pi \times R11 (C10 + C12)] = 8.8$ kHz

$f_p(C_{OUT}) = 1 / [2\pi \times R_L \times C_{OUT}] = 960$ Hz

$f_z(ESR) = 1 / [2\pi \times ESR \times C_{OUT}] = 27$ kHz

$f_p(HF) \sim 40$ kHz

Using these values, the calculated gain plot is shown in *Figure 6*.

## Application Information (Continued)

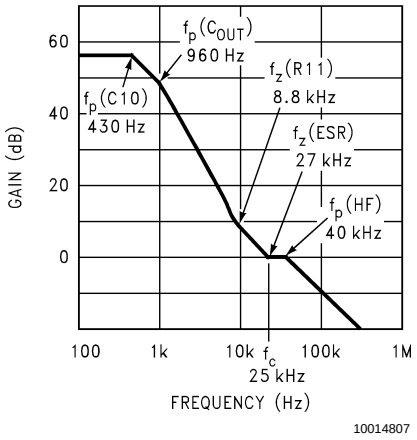



**FIGURE 6. Calculated Gain Plot for 3.3V/4A Application**

Looking at the plot, it can be seen that the unity-gain crossover frequency $f_c$ is expected to be about 25 kHz. Using this value, the phase margin at the point is calculated to be about 84˚.

To verify the accuracy of these calculations, the circuit was bench tested using a network analyzer. The measured gain and phase are shown plotted in *Figure 7*.

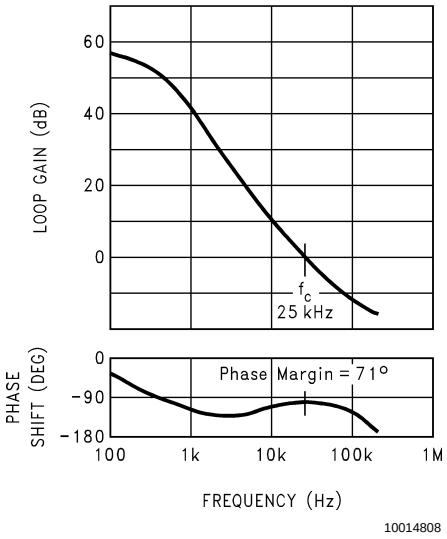



**FIGURE 7. Measured Gain/Phase Plot for 3.3V/4A Application**

The measured gain plot agrees very closely to the predicted values. The phase margin at 0 dB is slightly less than predicted (71˚ vs. 84˚), which is to be expected due to the negative phase shift contributions of high frequency poles not included in this simplified analysis.

It should be noted that 70˚ phase margin with 25 kHz bandwidth is excellent, and represents the optimal compensation for this set of values for $V_{IN}$, $V_{OUT}$, inductor and $R_L$.

### Optimizing Stability

The best tool for measuring both bandwidth and phase margin is a network analyzer. If this is not available, a simple method which gives a good measure of loop stability is to apply a minimum to maximum step of output load current and observe the resulting output voltage transient. A design which has good phase margin (>50˚) will typically show no ringing after the output voltage transient returns to its nominal value.

It should be noted that the stability (phase margin) does not have to be optimal for the regulator to be stable. The design analyzed in the previous section was re-compensated by changing R11 and C10 to intentionally reduce the phase margin to about 35˚ and re-tested for step response. The output waveform displayed slight ringing after the initial return to nominal, but was completely stable otherwise.

In most cases, the compensation components shown in the Typical Application Circuits will give good performance. To assist in optimizing phase margin, the following guidelines show the effects of changing various components.

**$C_{OUT}$:** Increasing the capacitance of $C_{OUT}$ moves the frequency of the pole $f_p(C_{OUT})$ to a lower value and reduces loop bandwidth. Increasing $C_{OUT}$ can be beneficial (increasing the phase margin) if the loop bandwidth is too wide (>$F_{OSC}$/5) which places the high-frequency poles too close to the unity-gain crossover frequency.

**ESR of $C_{OUT}$:** The ESR forms a zero $f_z$(ESR), which is needed to cancel negative phase shift near the unity-gain frequency. High-ESR capacitors can not be used, since the zero will be too low in frequency which will make the loop bandwidth too wide.

**R11/C10:** These form a pole and a zero. Changing the value of C10 changes the frequency of both the pole and zero. Note that since this causes the frequency of both the pole and zero to move up or down together, adjusting the value of C10 does not significantly affect loop bandwidth.

Changing the value of R11 moves the frequency location of the zero $f_z$(R11), but does not significantly shift the C10 pole (since the value of R11 is much less than the 160 kΩ output impedance of the Gm amplifier). Since only the zero is moved, this affects both bandwidth and phase margin. This means adjusting R11 is an easy way to maximize the positive phase shift provided by the zero. Best results are typically obtained if $f_z$(R11) is in the frequency range of $f_c$/4 to $f_c$ (where $f_c$ is the unity-gain crossover frequency).

## Design Procedure

This section presents guidelines for selecting external components.

### INDUCTOR SELECTION

In selecting an inductor, the parameters which are most important are inductance, current rating, and DC resistance.

#### Inductance

It is important to understand that all inductors are not created equal, as the method of specifying inductance varies widely.

It must also be noted that the inductance of every inductor decreases with current. The core material, size, and construction type all contribute the the inductor's dependence on current loading. Some inductors exhibit inductance curves which are relatively flat, while others may vary more than 2:1 from minimum to maximum current. In the latter

## Design Procedure (Continued)

case, the manufacturer's specified inductance value is usually the maximum value, which means the actual inductance in your application will be much less.

An inductor with a flatter inductance curve is preferable, since the loop characteristics of any switching converter are affected somewhat by inductance value. An inductor which has a more constant inductance value will give more consistent loop bandwidth when the load current is varied.

The data sheet for the inductor must be reviewed carefully to verify that the selected component will have the desired inductance at the frequency and current for the application.

**Current Rating**

This specification may be the most confusing of all when picking an inductor, as manufacturers use different methods for specifying an inductor's current rating.

The current rating specified for an inductor is typically given in RMS current, although in some cases a peak current rating will also be given (usually as a multiple of the RMS rating) which gives the user some indication of how well the inductance operates in the saturation region.

Other things being equal, a higher peak current rating is preferred, as this allows the inductor to tolerate high values of ripple current without significant loss of inductance.

In the some cases where the inductance vs. current curve is relatively flat, the given current rating is the point where the inductance drops 10% below the nominal value. If the inductance varies a lot with current, the current rating listed by the manufacturer may be the "center point" of the curve. This means if that value of current is used in your application, the amount of inductance will be less than the specified value.

**DC Resistance**

The DC resistance of the wire used in an inductor dissipates power which reduces overall efficiency. Thicker wire decreases resistance, but increases size, weight, and cost. A good tradeoff is achieved when the inductor's copper wire losses are about 2% of the maximum output power.

**Selecting An Inductor**

Determining the amount of inductance required for an application can be done using the formula:

$$L = \frac{(V_{IN} - V_{OUT})\, V_{OUT}}{V_{IN} \times I_{RIPPLE} \times F}$$

Where:

$V_{IN}$ is the maximum input voltage.

$V_{OUT}$ is the output voltage.

F is the switching frequency, $F_{OSC}$

$I_{RIPPLE}$ is the inductor ripple current. In general, a good value for this is about 30% of the DC output current.

It can be seen from the above equation, that increasing the switching frequency reduces the amount of required inductance proportionally. Of course, higher frequency operation is typically less efficient because switching losses become more predominant as a percentage of total power losses.

It should also be noted that reducing the inductance will increase inductor ripple current (other terms held constant). This is a good point to remember when selecting an inductor: increased ripple current increases the FET conduction losses, inductor core losses, and requires a larger output capacitor to maintain a given amount of output ripple voltage. This means that a cheaper inductor (with less inductance at the operating current of the application) will cost money in other places.

**INPUT CAPACITORS**

The switching action of the high-side FET requires that high peak currents be available to the switch or large voltage transients will appear on the $V_{IN}$ line. To supply these peak currents, a low ESR capacitor must be connected between the drain of the high-side FET and ground. The capacitor must be located as close as possible to the FET (maximum distance = 0.5 cm).

A solid Tantalum or low ESR aluminum electrolytic can be used for this capacitor. If a Tantalum is used, it must be able to withstand the turn-ON surge current when the input power is applied. To assure this, the capacitor must be surge tested by the manufacturer and guaranteed to work in such applications.

**Caution:** If a typical off-the-shelf Tantalum is used that has not been surge tested, it can be blown during power-up and will then be a dead short. This can cause the capacitor to catch fire if the input source continues to supply current.

**Voltage Rating**

For an aluminum electrolytic, the voltage rating must be at least 25% higher than the maximum input voltage for the application.

Tantalum capacit

## Notes

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