



## Features

- Lead free versions available
- RoHS compliant (lead free version)\*
- Bidirectional EMI filtering
- ESD protection > 25 k volts
- Protects 4 data lines

## Applications

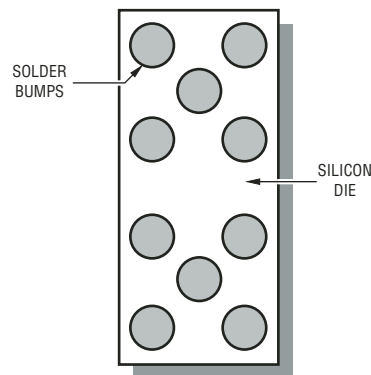
- Cell phones
- PDAs and notebooks
- Digital cameras
- MP3 players and GPS

## 2FAF-C10R - Integrated Passive & Active Device

### General Information

The 2FAF-C10R device, manufactured using Thin Film on Silicon technology, provides ESD protection and EMI filtering for the data ports of portable electronic devices such as cell phones, modems and PDAs. The device incorporates four low pass filter channels where each channel has a series 100 ohm resistor assuring a minimum of -28 dB attenuation from 800 MHz to 3 GHz. The device is suitable for EMI filtering of GSM, CDMA, W-CDMA, WLAN and Bluetooth frequencies.

Each internal and external port of the four channels includes a TVS diode for ESD protection. The ESD protection provided by the component enables a data port to withstand a minimum  $\pm 8$  KV Contact /  $\pm 15$  KV Air Discharge per the ESD test method specified in IEC 61000-4-2. The device measures 1.33 mm x 2 mm and is available in a 10 bump CSP package intended to be mounted directly onto an FR4 printed circuit board. The CSP device meets typical thermal cycle and bend test specifications without the use of an underfill material.



### Electrical Characteristics (@ $T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Per Line Specification	Symbol	Min.	Nom.	Max.	Unit
Resistance	R	80	100	120	—
Capacitance @ 2.5 V, 1 MHz	C	24	30	36	pF
Rated Standoff Voltage	$V_{WM}$		5.0		V
Breakdown Voltage @ 1 mA	$V_{BR}$	6.0			V
Forward Voltage @ 10 mA	$V_F$		0.8		V
Leakage Current @ 3.3 V	$I_R$		0.05	0.1	$\mu\text{A}$
Filter Attenuation @ 800-3000 MHz	S21	-28	-35		dB
ESD Protection: IEC 61000-4-2 Contact Discharge Air Discharge		$\pm 8$ $\pm 15$			kV kV
Power Dissipation per Resistor	$P_D$			100	mW

### Thermal Characteristics (@ $T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Min.	Nom.	Max.	Unit
Operating Temperature Range	$T_J$	-40	+25	+85	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-55	+25	+150	$^\circ\text{C}$

\*RoHS Directive 2002/95/EC Jan 27 2003, including Annex

Specifications are subject to change without notice.

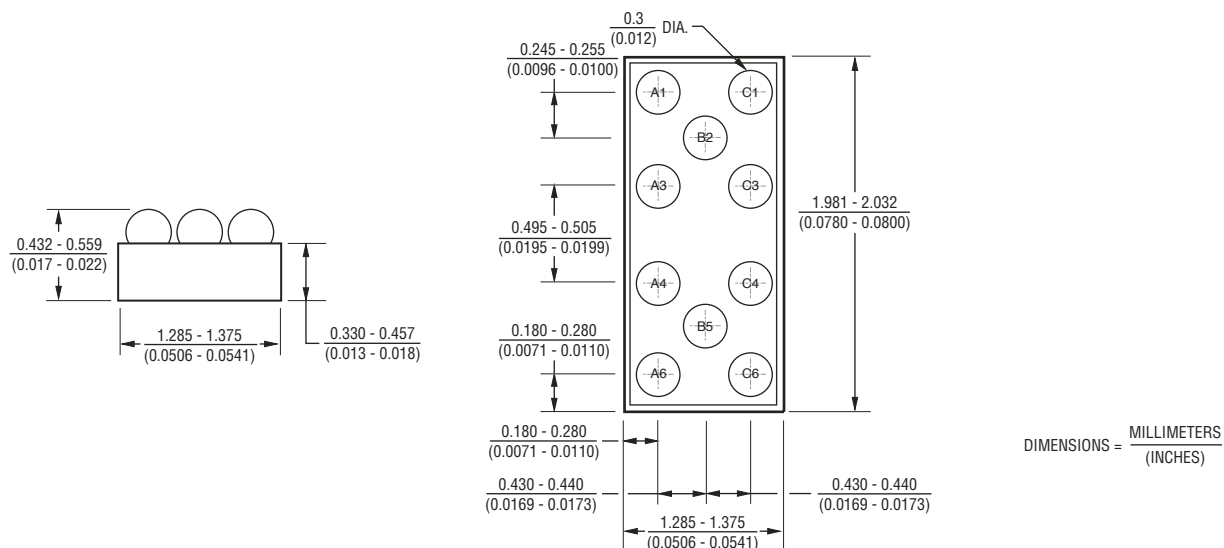
Customers should verify actual device performance in their specific applications.

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### Mechanical Characteristics

This is a silicon-based device and is packaged using chip scale packaging technology. Solder bumps, formed on the silicon die, provide the interconnect medium from die to PCB. The bumps are arranged on the die in a regular grid formation. The grid pitch is 0.5 mm and the dimensions for the packaged device are shown below.



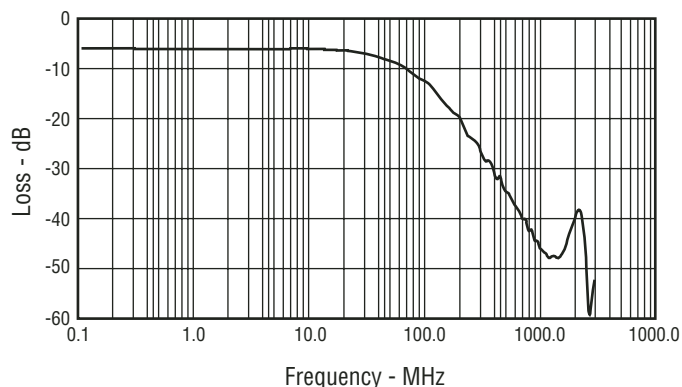
### Reliability Data

Reliability data is gathered on an ongoing basis for Bourns® Integrated Passive and Active Devices.

“Package level” testing of the integrity of the solder joint is carried out on an independent Daisy-Chain test device. A 25-Pin Daisy Chain component is available from Bourns for this purpose (part number 2TAD-C25R). This is a 5 x 5 array featuring 0.5 mm pitch solder bumps. The Distance to Neutral Point (DNP) on that component is larger than that of the 2FAF-C10R and is thus deemed suitable for Thermal Cycle testing.

“Silicon level” reliability performance is based on similarity to other integrated passive CSP devices from Bourns.

### Frequency Response



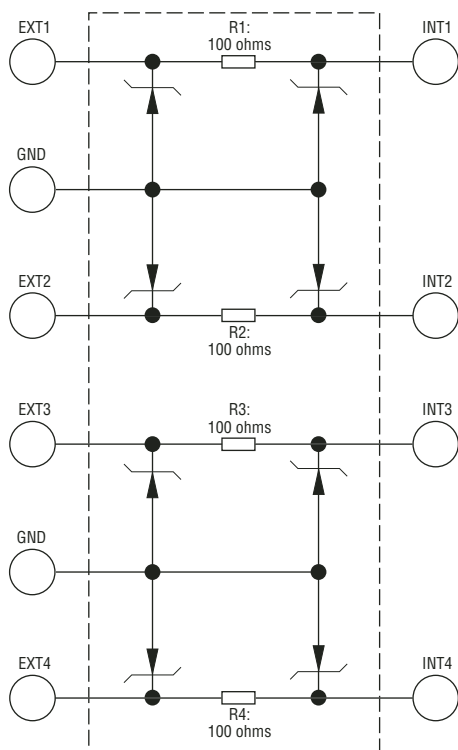
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### Block Diagram

The CSP device block diagram below includes the pin names and basic electrical connections associated with each channel.



### PCB Design and SMT Processing

Please consult the “Bourns Design Guide Using CSP” for notes on PCB design and SMT Processing.

### How to Order

**2 FAF - C10R**

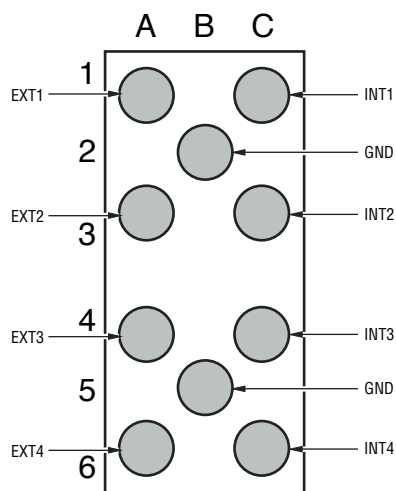
Thinfilim \_\_\_\_\_  
Model \_\_\_\_\_  
Chipscale \_\_\_\_\_  
No. of Solder Bumps \_\_\_\_\_  
Packaging Option \_\_\_\_\_  
    R = Tape and Reel  
    Packaged 5000 pcs. / 7" reel  
Terminations \_\_\_\_\_  
    LF = Sn/Ag/Cu (lead free)  
    \_\_ = Sn/Pb

## 2FAF-C10R - Integrated Passive & Active Device

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### Device Pin Out

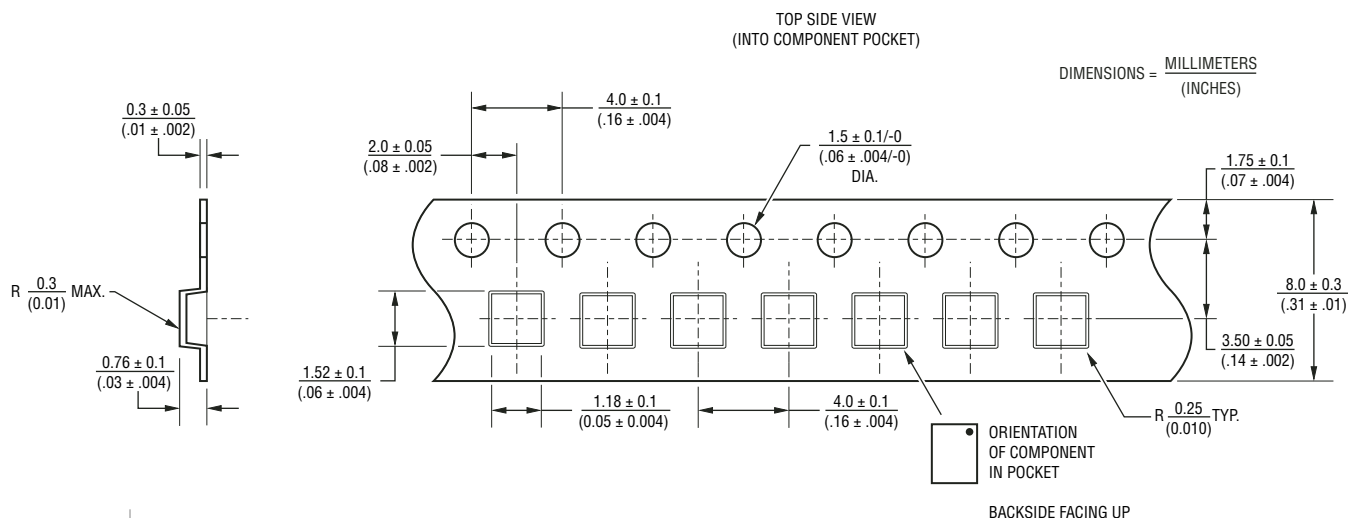
The Pin-Out for the device is shown below. Note also that the device is shown with bottom side solder pads facing up.



Pin Out	Function	Pin Out	Function
A1	EXT1	C1	INT1
A3	EXT2	C3	INT2
A4	EXT3	C4	INT3
A6	EXT4	C6	INT4
B2	GND	B5	GND

### Packaging

The surface mount product is packaged in an 8 mm x 4 mm Tape and Reel format per EIA-481 standard.



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