PRELIMINARY | Data Sheet | January 13, 2005 | FN8149.0

Penta-Power Sequence Controller with Hot swap and System Management

The X80010, X80011, X80012, X80013 contain three major functions: a power sequencing controller, a hotswap controller, and systems management support.

The power sequencer controller time sequences up to five DC/DC modules. The device allows various DC/DC power sequencing configurations, either parallel or relay modes. The power good, enable, and voltage good signals provide for flexible DC/DC timing configurations. Each voltage enable signal has a built-in delay while additional delay can be added with simple external passive components.

The hot swap controller allows a board to be safely inserted and removed from a live backplane without turning off the main power supply. The X80010 family of devices offers a modular, power distribution approach by providing flexibility to solve the hotswap and power sequencing issues for insertion, operations, and extraction. Hardshort Detection and Retry with Delay, Noise filtering, Insertion Overcurrent Bypass, and Gate Current selection are some of the integrated features of the device. During insertion, the gate of an external power MOSFET is clamped low to suppress contact bounce. The undervoltage/overvoltage circuits and the power on reset circuitry suppress the gate turn on until the mechanical bounce has ended. The X80010 turns on the gate with a user set slew rate to limit the inrush current and incorporates an electronic circuit breaker set by a sense resistor. After the load is successfully charged, the PWRGD signal is asserted; indicating that the device is ready to power sequence the DC/DC power bricks.

Systems management function provides a reset signal indicating that the power good and all the voltage good signals are active. The reset signal is asserted after a wait state delay. This signal is used to coordinate the hotswap and DC/DC module latencies during power up to avoid "power hang up". In addition, the CPU host can initiate soft insertion or DC voltage module re-sequencing.

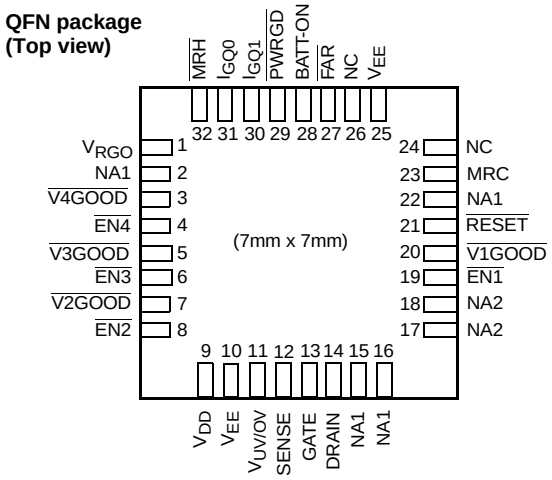
Features

- Integrates Three Major Functions
  - Power Sequencing
  - Hot Swap Controller
  - System Management Functions
- Penta-Power Sequencing
  - Sequence up to 5 DC/DC converters.
  - Four independent voltage enable pins
  - Four time delay circuits
  - Soft Power Sequencing - MRC pin restarts sequence without power cycling.
- Hot Swap Controller
  - Programmable overvoltage and undervoltage protection
  - Undervoltage lockout for battery/redundant supplies
  - Electronic circuit breaker - Overcurrent Detection and Gate Shut-off
  - Overcurrent limit during Insertion
  - Hardshort retry with retry failure flag
  - Selectable gate current using IGQ pins (10, 70, 150µA)
  - MRH pin controls board insertion/extraction.
  - Typically operates from -30V to -80V. Tolerates transients to -200V (limited by external components)
- System Management
  - Reset output, with delay, holds off host until all supplies are good
  - Host control of reinsertion with MRH input
  - Host control of resequencing using MRC input
- Available packages
  - 32-lead Quad No-Lead Frame (QFN)

Applications

- -48V Hot Swap Power Backplane/Distribution Central Office, Ethernet for VOIP
- Card Insertion Detection
- Power Sequencing DC/DC/Power Bricks
- IP Phone Applications
- Databus Power Interfacing
- Custom Industrial Power Backplanes
- Distributed Power Systems

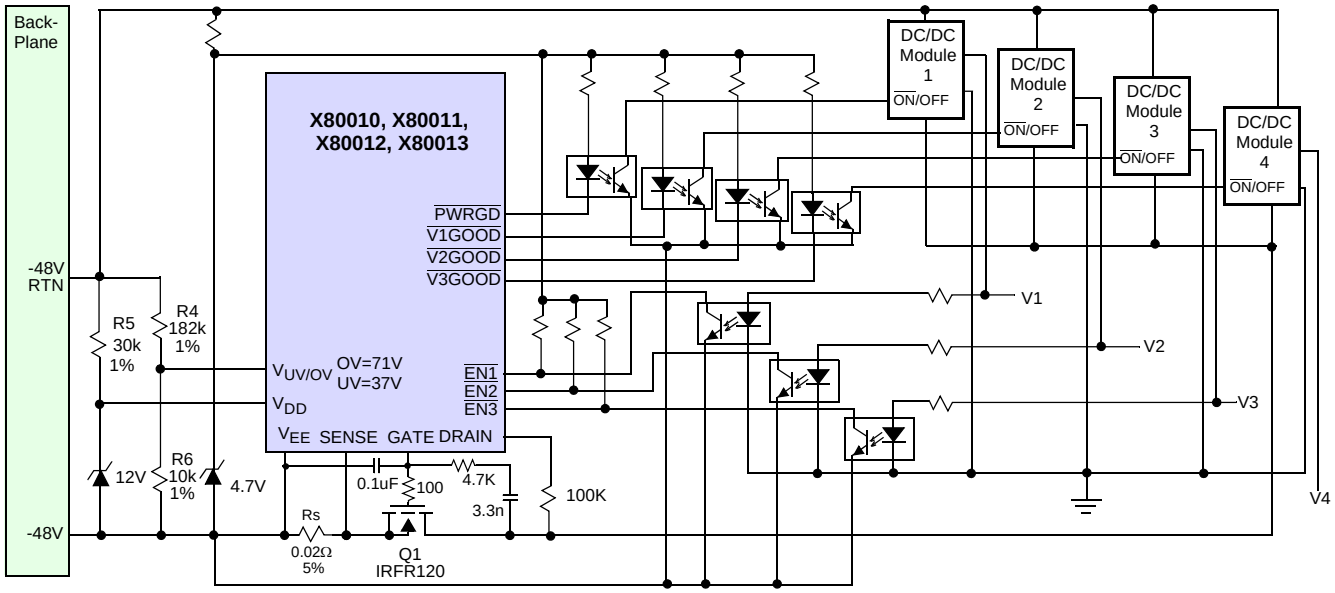
Pinout



Ordering Information

ORDER NUMBER	OV (V)	UV1 (V)	UV2 (V)	t_{NF} (us)	V_{OC} (mV)	V_{OCI} (mV)	OVER CURRENT RETRY	RETRY DELAY (ms)	I_{GATE} (µA)	T_{DELAY} (ms)	t_{POR} (ms)	TEMP RANGE (°C)	PART MARK
X80010Q32I	74.9	42.4	33.2	5	50	150	Always	100	50	100	100	-40 to 85	80010I
X80011Q32I	68.0	42.4	33.2	5	50	150	Always	100	50	100	100	-40 to 85	80011I
X80012Q32I	74.9	42.4	33.2	5	50	150	5 retries	100	50	100	100	-40 to 85	80012I
X80013Q32I	68.0	42.4	33.2	5	50	150	5 retries	100	50	100	100	-40 to 85	80013I

Typical Application



Absolute Maximum Ratings

Temperature under bias . . . . . –65°C to +135°C
Storage temperature . . . . . –65°C to +150°C
Voltage on given pin (Hot Side Functions):
$V_{ov/uv\ pin}$ . . . . . 5.5V + V_{EE}
SENSE pin . . . . . 400mV + V_{EE}
V_{EE} pin . . . . . -80V
DRAIN pin . . . . . 48V + V_{EE}
PWRGD pin . . . . . 7V + V_{EE}
GATE pin . . . . . V_{DD} + V_{EE}
FAR pin . . . . . 7V + V_{EE}
MRH pin . . . . . 5.5V + V_{EE}
BATT_ON pin . . . . . 5.5V + V_{EE}

Voltage on given pin (Cold Side Functions):
ENi pins (i = 1 to 4) 5V
ViGOOD pins (i = 1 to 4) . . . . . 5.5V + V_{EE}
RESET pin . . . . . 5.5V + V_{EE}
MRC pin . . . . . 5.5V + V_{EE}
IGQ1 and IGQ0 pins . . . . . 5.5V + V_{EE}
V_{DD} pin . . . . . 14V + V_{EE}
D.C. output current. 5mA
Lead temperature (soldering, 10 seconds) . . . . . 300°C

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to 85°C
Supply Voltage (V_{DD}) 12V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications (Standard Settings)

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
V_{DD}	Supply Operating Range		10	12	14	V
I_{DD}	Supply Current			2.5	5	mA
V_{RGO}	Regulated 5V output	I_{RGO} = 10µA	4.5		6.0	
I_{RGO}	V_{RGO} current output				50	µA
I_{GATE}	Gate Pin Current	Gate Drive On, V_{GATE} = V_{EE}, V_{SENSE} = V_{EE} (sourcing)	46.2	52.5	58.8	µA
		V_{GATE} - V_{EE} = 3V V_{SENSE}-V_{EE} = 0.1V (sinking)		9		mA
V_{GATE}	External Gate Drive (Slew Rate Control)	I_{GATE} = 50µA	V_{DD}-1		V_{DD}	V
V_{PGA}	Power Good Threshold (PWRGD High to Low)	Referenced to V_{EE} V_{UV1} < $V_{UV/OV}$ < V_{OV}	0.9	1	1.1	V
V_{IHB}	Voltage Input High (BATT_ON)		V_{EE} + 4		V_{EE} + 5	V
V_{ILB}	Voltage Input Low (BATT_ON)				V_{EE} + 2	V
I_{LI}	Input Leakage Current (MRH, MRC)	V_{IL} = GND to V_{CC}			10	µA
I_{LO}	Output Leakage Current (V1GOOD, V2GOOD, V3GOOD, V4GOOD, RESET)	All ENi = V_{RGO} for i = 1 to 4			10	µA
V_{IL}(3)	Input LOW Voltage (MRH, MRC, IGQ0, IGQ1)		-0.5 + V_{EE}		(V_{EE} + 5) x 0.3	V
V_{IH}(3)	Input HIGH Voltage (MRH, MRC, IGQ0, IGQ1)		(V_{EE} + 5) x 0.7		(V_{EE} + 5) + 0.5	V

Electrical Specifications (Standard Settings)

Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output LOW Voltage ($\overline{RESET}$, RESET, $\overline{V1GOOD}$, $\overline{V2GOOD}$, $\overline{V3GOOD}$, $\overline{V4GOOD}$, FAR, PWRGD)	I_{OL} = 4.0mA (V_{EE} + 2.7 to V_{EE} + 5.5V) I_{OL} = 2.0mA (V_{EE} + 2.7 to V_{EE} + 3.6V)			V_{EE} + 0.4	V
C_{OUT}(1)	Output Capacitance ($\overline{RESET}$, $\overline{V1GOOD}$, $\overline{V2GOOD}$, $\overline{V3GOOD}$, $\overline{V4GOOD}$, $\overline{FAR}$)	V_{OUT} = 0V			8	pF
C_{IN}(1)	Input Capacitance ($\overline{MRH}$, MRC)	V_{IN} = 0V			6	pF
V_{OC}	Over-current threshold	V_{OC} = V_{SENSE} - V_{EE}	45	50	55	mV
V_{OCI}	Over-current threshold (Insertion)	V_{OC} = V_{SENSE} - V_{EE} $\overline{PWRGD}$ = HIGH Initial Power Up condition	135	150	165	mV
V_{OVR}	Overvoltage threshold (rising) X80010, X80012 X80011, X80013	Referenced to V_{EE}	 3.85 3.49	 3.90 3.54	 3.95 3.59	V
V_{OVH}	Overvoltage hysteresis	Referenced to V_{EE}	12	18	24	mV
V_{UV1H}	Undervoltage 1 hysteresis	Referenced to V_{EE} BATT-ON = V_{EE}	12	18	24	mV
V_{UV1F}	Undervoltage 1 threshold (falling)		2.16	2.21	2.26	V
V_{UV2H}	Undervoltage 2 hysteresis	Referenced to V_{EE} BATT-ON = V_{RGO}	12	18	24	mV
V_{UV2F}	Undervoltage 2 threshold (falling)		1.68	1.73	1.78	V
V_{DRAINF}	Drain sense voltage threshold (falling)	Referenced to V_{EE}	0.9	1	1.1	V
V_{DRAINR}	Drain sense voltage threshold (rising)	Referenced to V_{EE}	1.2	1.3	1.4	V
V_{TRIP1}	$\overline{EN1}$ Trip Point Voltage	Referenced to V_{EE}	2.25	2.5	2.75	V
V_{TRIP2}	$\overline{EN2}$ Trip Point Voltage	Referenced to V_{EE}	2.25	2.5	2.75	V
V_{TRIP3}	$\overline{EN3}$ Trip Point Voltage	Referenced to V_{EE}	2.25	2.5	2.75	V
V_{TRIP4}	$\overline{EN4}$ Trip Point Voltage	Referenced to V_{EE}	2.25	2.5	2.75	V
AC CHARACTERISTICS						
t_{FOC}	Sense High to Gate Low		1.5	2.5	3.5	µs
t_{FUV}	Under Voltage conditions to Gate Low		0.5	1.0	1.5	µs
t_{FOV}	Overvoltage Conditions to Gate Low		1.0	1.5	2	µs
t_{VFR}	Overvoltage/undervoltage failure recovery time to Gate =1V.	V_{DD} does not drop below 3V, No other failure conditions.	1.2	1.6	2	µs
t_{BATT_ON}	Delay BATT_ON Valid			100		ns
t_{MRC}	Minimum time high for reset valid on the MRC pin		5			µs
t_{MRH}	Minimum time high for reset valid on the $\overline{MRH}$ pin		5			µs
t_{MRCE}	Delay from MRC enable to $\overline{PWRGD}$ HIGH	No Load	1.0		1.6	µs
t_{MRCD}	Delay from MRC disable to $\overline{PWRGD}$ LOW	Gate is On, No Load	200		400	µs
t_{MRHE}	Delay from $\overline{MRH}$ enable to Gate Pin LOW	I_{GATE} = 60µA, No Load	1.0	1.6	2.4	µs
t_{MRHD}	Delay from $\overline{MRH}$ disable to GATE reaching 1V	I_{GATE} = 60µA, No Load	1.8		2.6	µs

Electrical Specifications (Standard Settings)

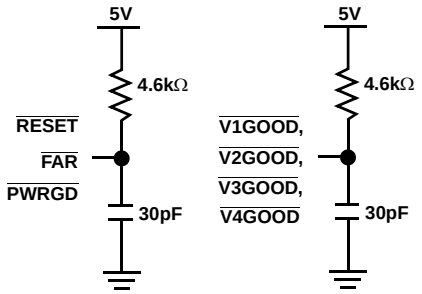
Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\overline{RESET}\_E}$	Delay from $\overline{PWRGD}$ or $\overline{ViGOOD}$ to $\overline{RESET}$ valid LOW				1	µs
t_{QC}	Delay from IGQ1 and IGQ0 to valid Gate pin current				1	µs
t_{SC_RETRY}	Delay between Retries		85	100	115	ms
t_{NF}	Noise Filter for Overcurrent		4.5	5	5.5	µs
t_{DPOR}	Device Delay before Gate assertion		45	50	55	ms
t_{SPOR}	Delay after $\overline{PWRGD}$ and all $\overline{ViGOOD}$ signals are active before $\overline{RESET}$ assertion		85	100	115	ms
t_{DELAY1}	Power Sequencing Time Delay TiD1 = 0; TiD0 = 0		85	100	115	ms
t_{DELAY2}						
t_{DELAY3}						
t_{DELAY4}						
t_{TO}	$\overline{ViGOOD}$ turn off time			50		ns
t_{PDHLPG}(1)	Delay from Drain good to $\overline{PWRGD}$ LOW	Gate = V_{DD}			1	µs
t_{PDLHPG}(1)	Delay from Drain fail to $\overline{PWRGD}$ HIGH	Gate = V_{DD}			1	µs
t_{PGHLPG}(1)	Delay from Gate good to $\overline{PWRGD}$ LOW	Drain = V_{EE}			1	µs
t_{PGLHPG}(1)	Delay from Gate fail to $\overline{PWRGD}$ HIGH	Drain = V_{EE}			1	µs

NOTE:

1. This parameter is based on characterization data.

Equivalent A.C. Output Load Circuit



A.C. Test Conditions

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing levels	V_{CC} x 0.5
Output load	Standard output load

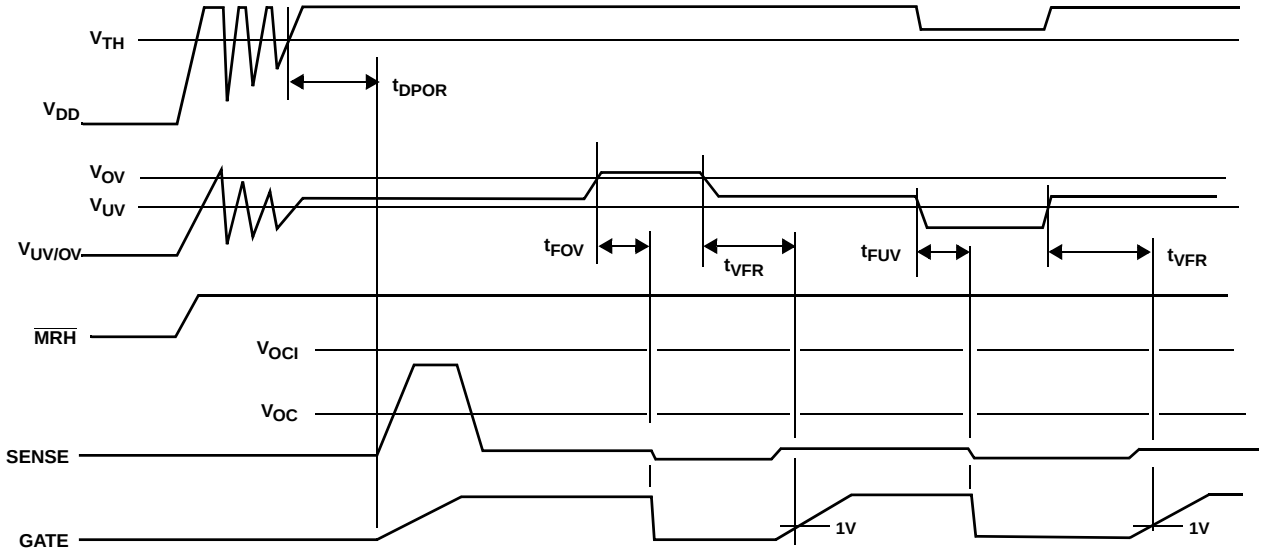


FIGURE 1. OVERVOLTAGE/UNDERVOLTAGE GATE TIMING

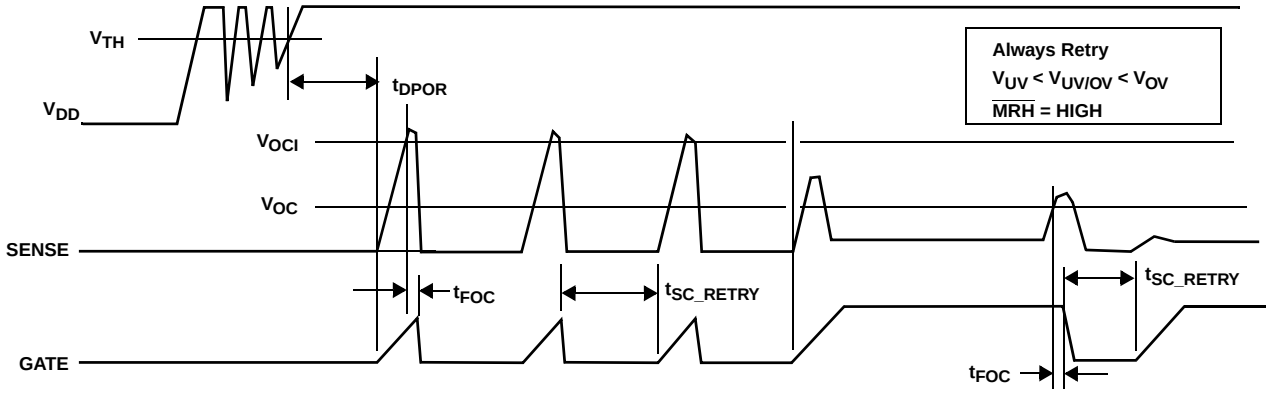


FIGURE 2. OVERCURRENT GATE TIMING

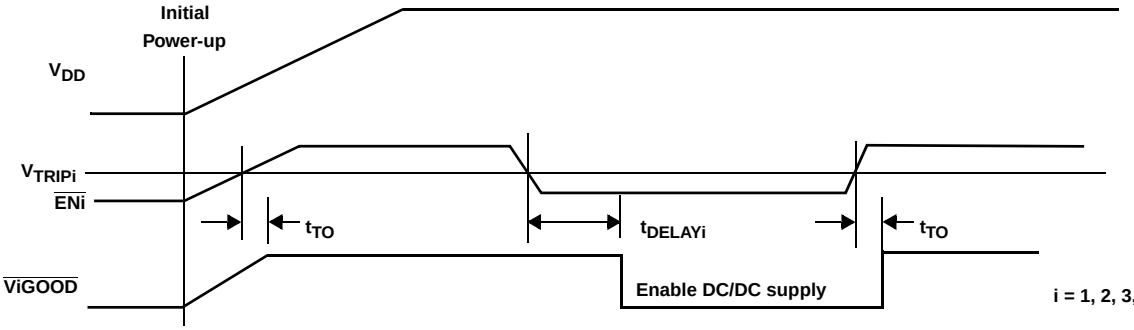


FIGURE 3. $\overline{ViGOOD}$ TIMINGS

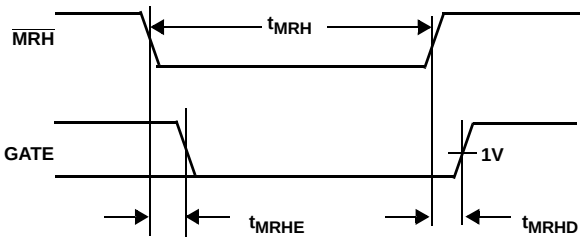


FIGURE 4. MANUAL RESET (HOT SIDE) $\overline{MRH}$

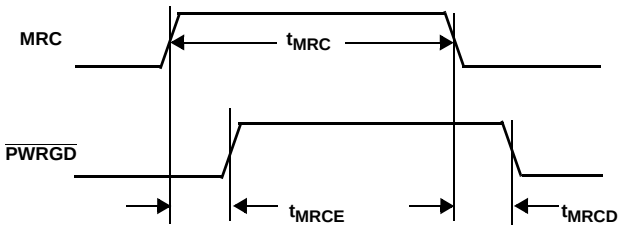


FIGURE 5. MANUAL RESET (COLD SIDE) MRC

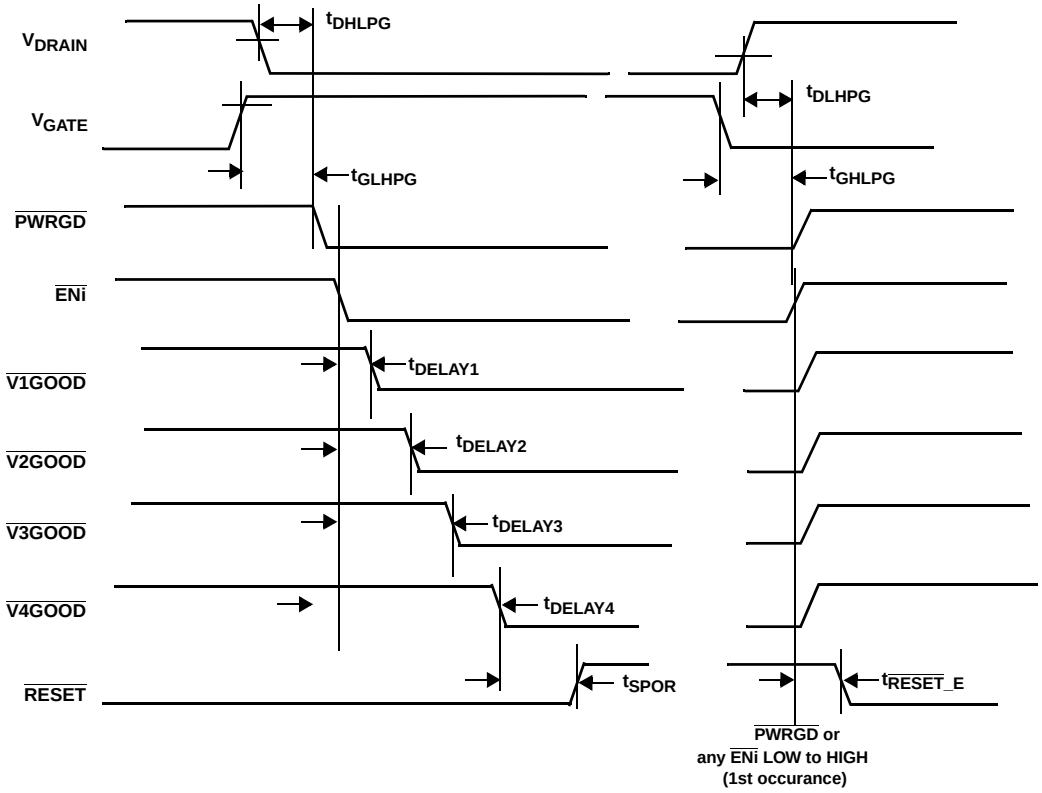


FIGURE 6. $\overline{RESET}$ TIMINGS

Typical Performance Characteristics

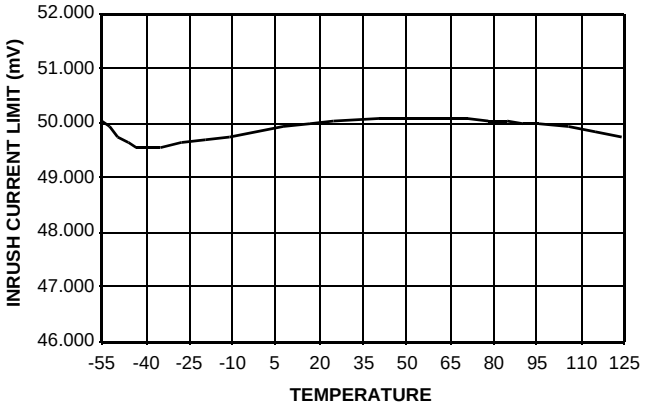


FIGURE 7. OVER CURRENT THRESHOLD vs TEMPERATURE

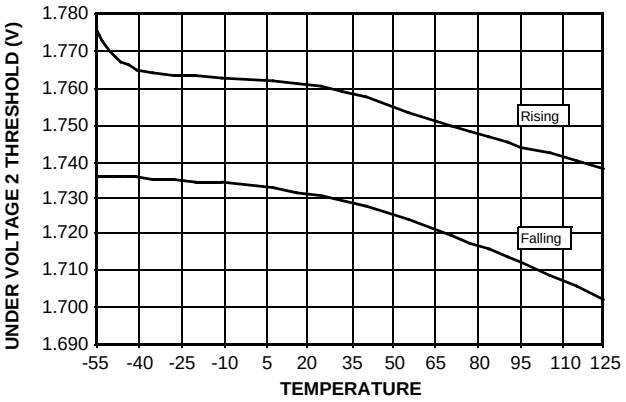


FIGURE 8. UNDERVOLTAGE 2 THRESHOLD vs TEMPERATURE

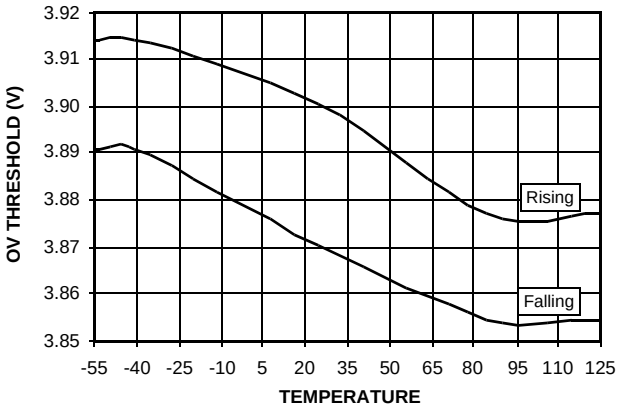


FIGURE 9. OVERVOLTAGE THRESHOLD vs TEMPERATURE

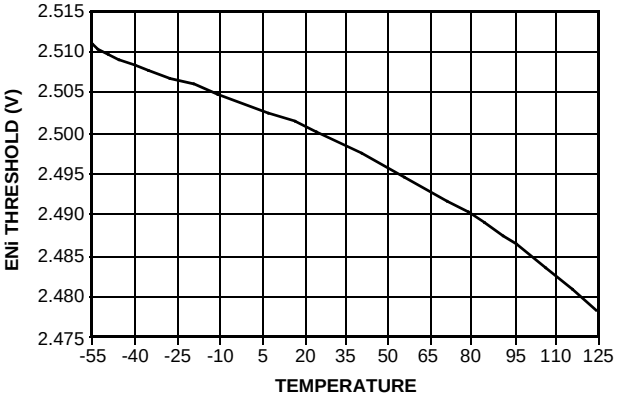


FIGURE 10. $\overline{ENi}$ THRESHOLD vs TEMPERATURE

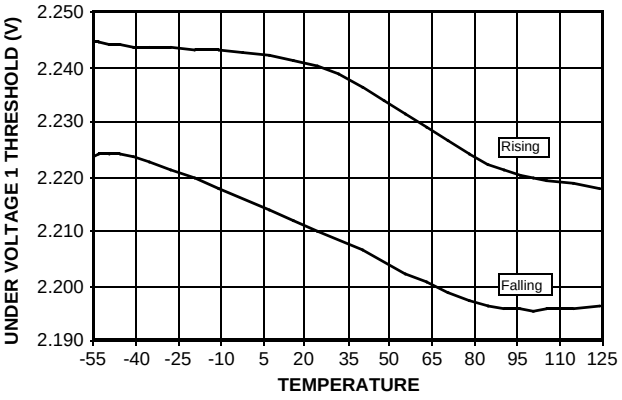


FIGURE 11. UNDERVOLTAGE 1 THRESHOLD vs TEMPERATURE

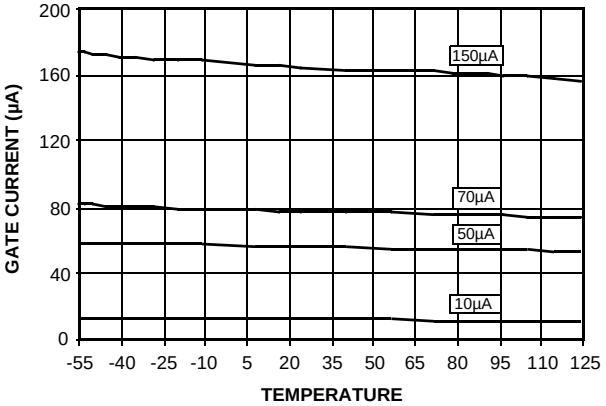


FIGURE 12. I_{GATE} (SOURCE) vs TEMPERATURE

Typical Performance Characteristics (Continued)

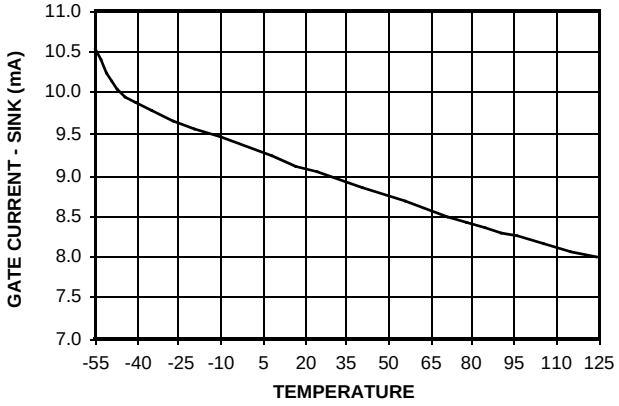


FIGURE 13. I_{GATE} (SINK) vs TEMPERATURE

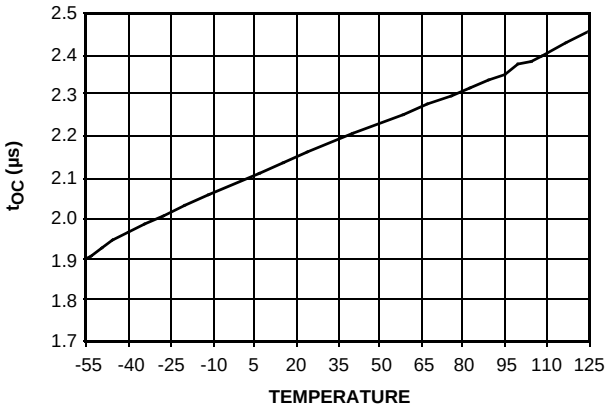


FIGURE 14. T_{FOC} vs TEMPERATURE

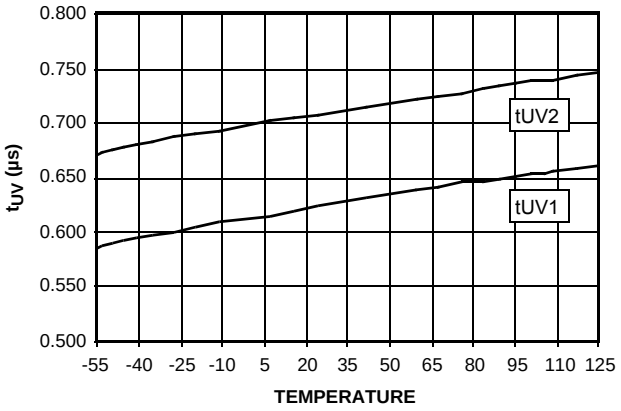


FIGURE 15. t_{FUV} vs TEMPERATURE

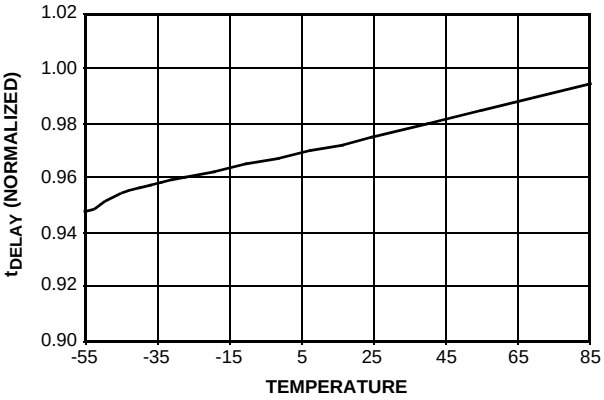


FIGURE 16. t_{DELAYi} vs TEMPERATURE

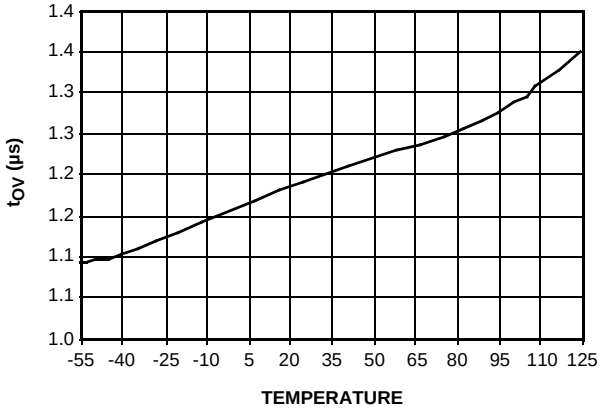


FIGURE 17. t_{FOV} vs TEMPERATURE

Typical Performance Characteristics (Continued)

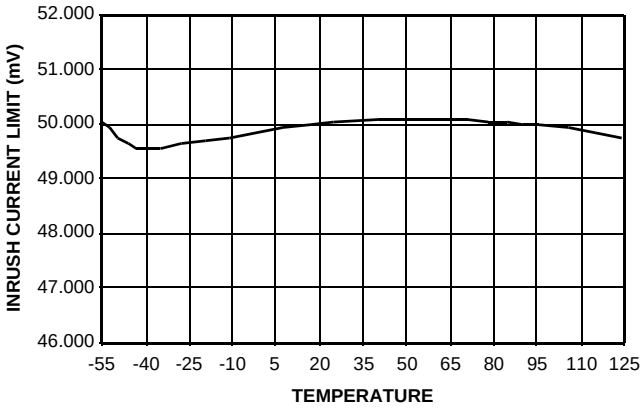


FIGURE 18. OVER CURRENT THRESHOLD vs TEMPERATURE

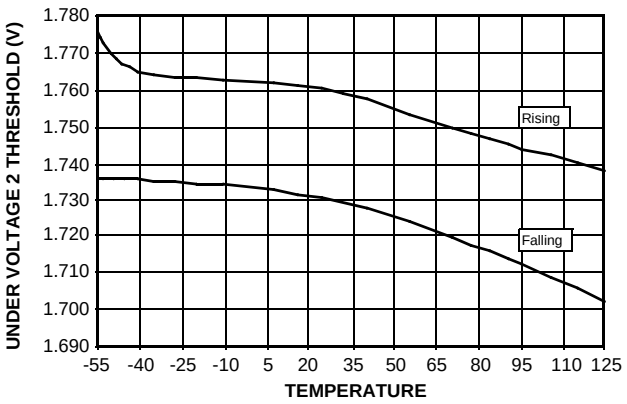


FIGURE 19. UNDERVOLTAGE 2 THRESHOLD vs TEMPERATURE

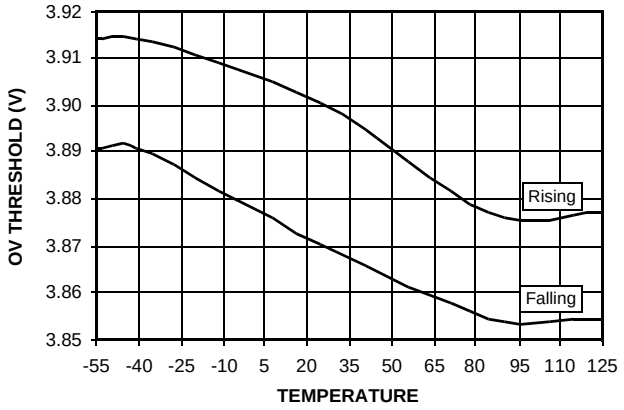


FIGURE 20. OVERVOLTAGE THRESHOLD vs TEMPERATURE

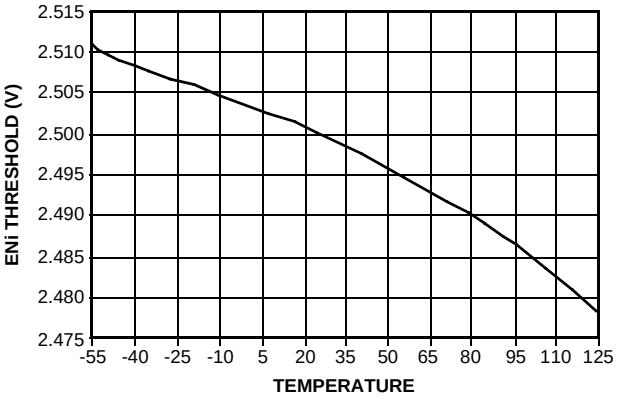


FIGURE 21. $\overline{ENi}$ THRESHOLD vs TEMPERATURE

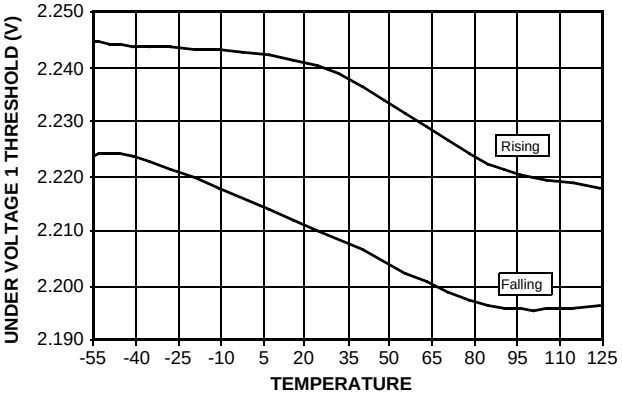


FIGURE 22. UNDERVOLTAGE 1 THRESHOLD vs TEMPERATURE

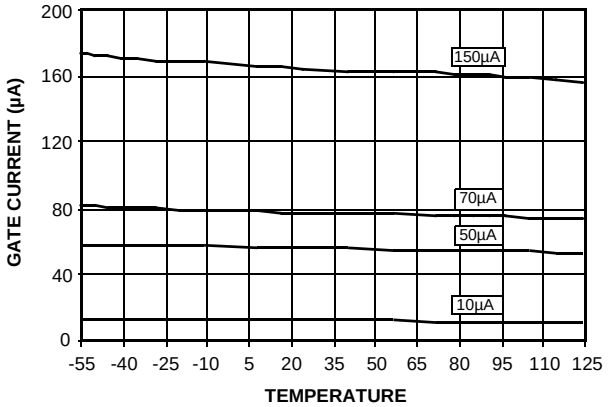


FIGURE 23. I_{GATE} (SOURCE) vs TEMPERATURE

Typical Performance Characteristics (Continued)

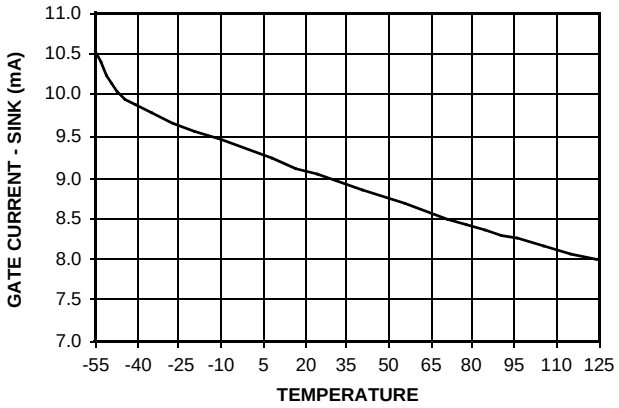


FIGURE 24. I_{GATE} (SINK) vs TEMPERATURE

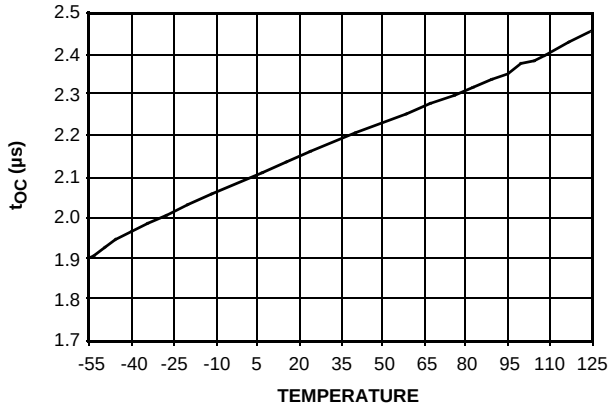


FIGURE 25. t_{FOC} vs TEMPERATURE

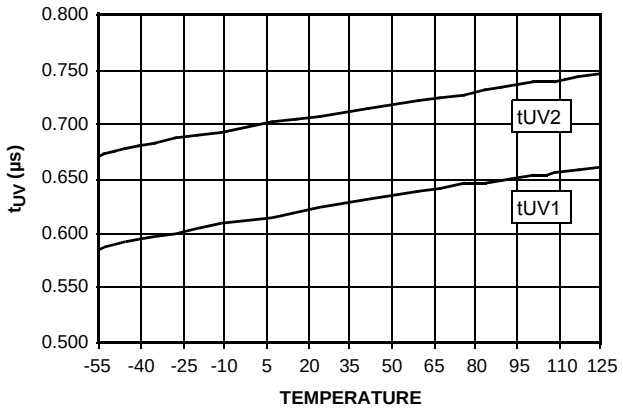


FIGURE 26. t_{FUV} vs TEMPERATURE

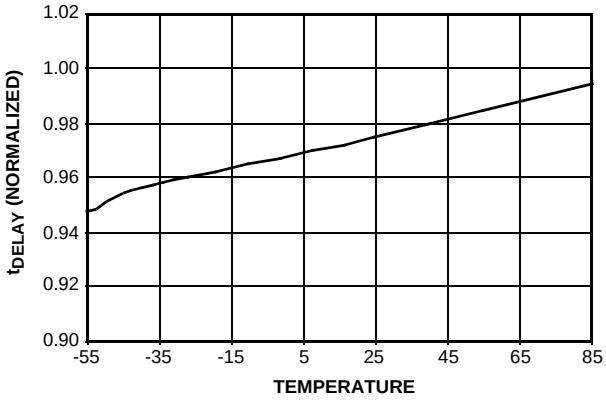


FIGURE 27. t_{DELAYi} vs TEMPERATURE

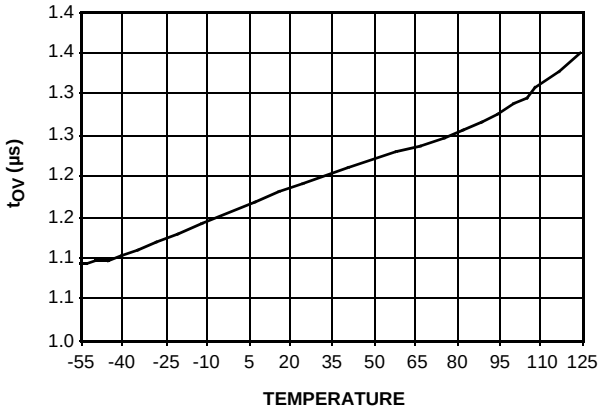


FIGURE 28. t_{FOV} vs TEMPERATURE

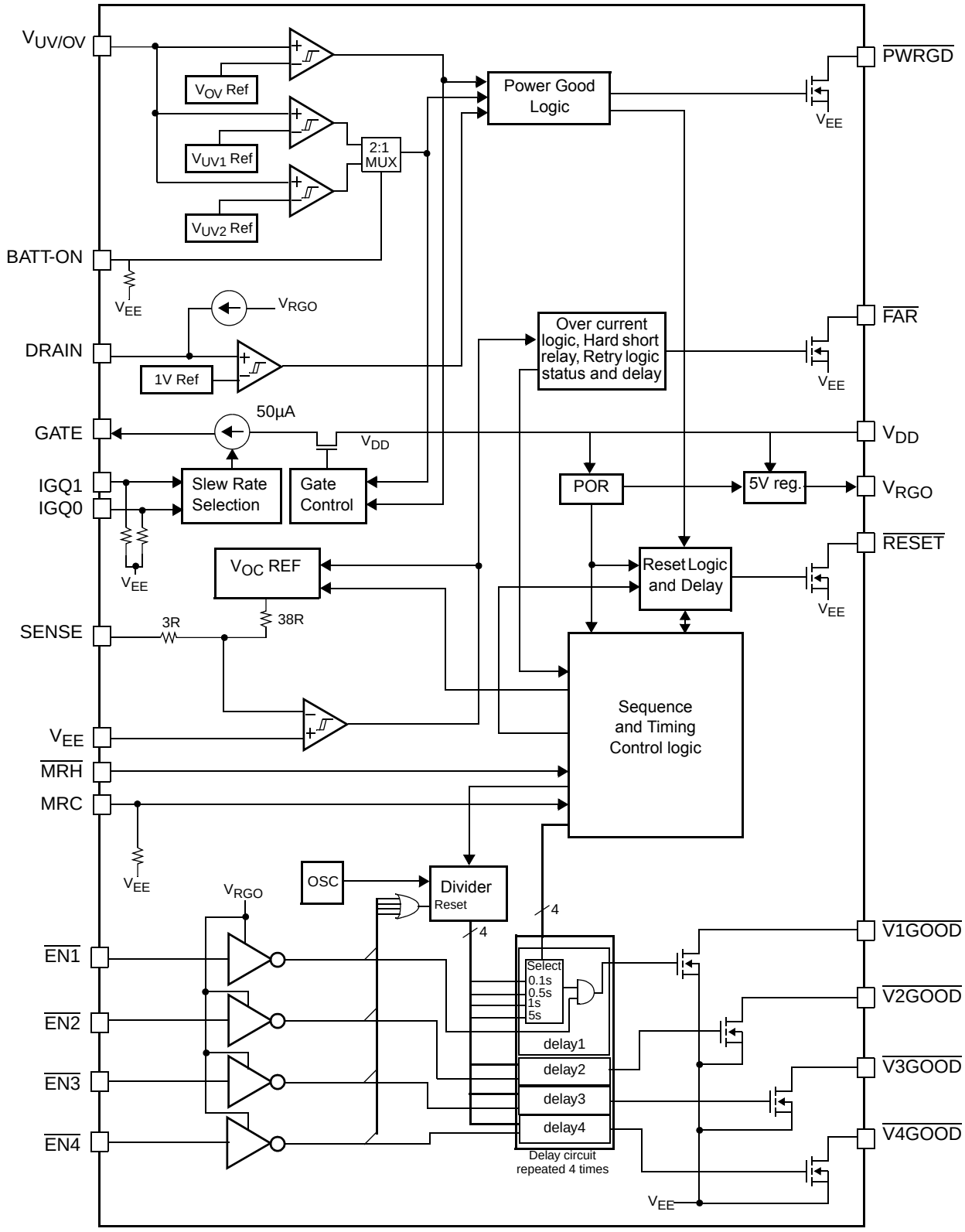
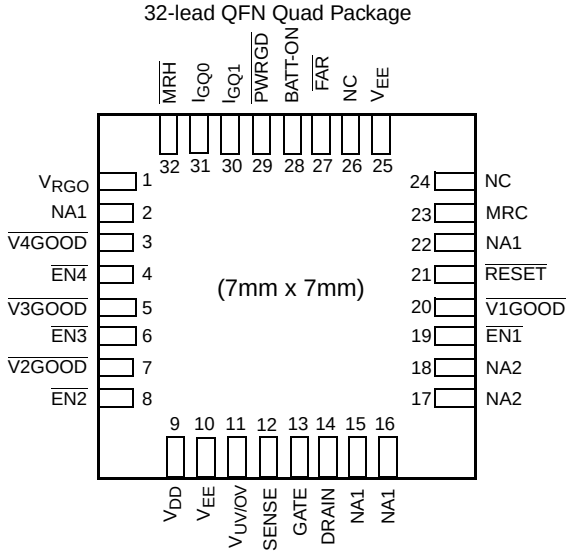


FIGURE 29. BLOCK DIAGRAM

Pin Configuration

X80010, X80011, X80012, X80013

32-lead QFN Quad Package



Pin Descriptions

PIN	NAME	DESCRIPTION
1	V_{RGO}	**Regulated 5V output.** Used to pull-up user programmable inputs IGQ0, IGQ1, BATT-ON (if needed).
2	NA1	**Not Available.** Do not connect to this pin.
3	$\overline{V4GOOD}$	**V4 Voltage Good Output.** This open drain output goes LOW when $\overline{EN4}$ is less than V_{TRIP4} and goes HIGH when $\overline{EN4}$ is greater than V_{TRIP4}. There is a user selectable delay circuitry on this pin.
4	$\overline{EN4}$	**V4 Voltage Enable Input.** Fourth voltage enable pin. If unused connect to V_{RGO}.
5	$\overline{V3GOOD}$	**V3 Voltage Good Output (Active Low).** This open drain output goes LOW when $\overline{EN3}$ is less than V_{TRIP3} and goes HIGH when $\overline{EN3}$ is greater than V_{TRIP3}. There is a user selectable delay circuitry on this pin.
6	$\overline{EN3}$	**V3 Voltage Enable Input.** Third voltage enable pin. If unused connect to V_{RGO}.
7	$\overline{V2GOOD}$	**V2 Voltage Good Output (Active Low).** This open drain output goes LOW when $\overline{EN2}$ is less than V_{TRIP2} and goes HIGH when $\overline{EN2}$ is greater than V_{TRIP2}. There is a user selectable delay circuitry on this pin.
8	$\overline{EN2}$	**V2 Voltage Enable Input.** Second voltage enable pin. If unused connect to V_{RGO}.
9	V_{DD}	Positive Supply Voltage Input.
10	V_{EE}	Negative Supply Voltage Input.
11	$V_{UV/OV}$	**Analog Undervoltage and Overvoltage Input.** Turns off the external N-channel MOSFET when there is an undervoltage or overvoltage condition.
12	SENSE	**Circuit Breaker Sense Input**. This input pin detects the overcurrent condition.
13	GATE	**Gate Drive Output.** Gate drive output for the external N-channel MOSFET.
14	DRAIN	**Drain**. Drain sense input of the external N-channel MOSFET.
15	NA1	**Not Available.** Do not connect to this pin.
16	NA1	**Not Available.** Do not connect to this pin.
17	NA2	**Not Available.** Connect to V_{RGO}.
18	NA2	**Not Available.** Connect to V_{RGO}.
19	$\overline{EN1}$	**V1 Voltage Enable Input.** First voltage enable pin. If unused connect to V_{RGO}.
20	$\overline{V1GOOD}$	**V1 Voltage Good Output (Active Low).**This open drain output goes LOW when $\overline{EN1}$ is less than V_{TRIP1} and goes HIGH when $\overline{EN1}$ is greater than V_{TRIP1}. There is a user selectable delay circuitry on this pin.

Pin Descriptions (Continued)

PIN	NAME	DESCRIPTION
21	$\overline{\text{RESET}}$	**RESET Output.** This open drain pin is an active LOW output. This pin will be active until $\overline{\text{PWRGD}}$ goes active and the power sequencing is complete. This pin will be released after a programmable delay.
22	NA1	**Not Available.** Do not connect to this pin.
23	MRC	**Manual Reset Input Cold-side.** Pulling the MRC pin HIGH initiates a system side RESET. The MRC signal must be held HIGH for 5µs. It has an internal pulldown resistor. (>10mΩ typical)
24	NC	**No Connect.** No internal connections.
25	V_{EE}	Negative Supply Voltage Input.
26	NC	**No Connect.** No internal connections.
27	$\overline{\text{FAR}}$	**Failure After Re-try ($\overline{\text{FAR}}$)** output signal. Failure After Re-try ($\overline{\text{FAR}}$) is asserted after a number of retries. Used for Overcurrent and hardshort detection.
28	BATT-ON	**Battery On Input**. This input signals that the battery backup (or secondary supply) is supplying power to the backplane. It has an internal pulldown resistor. (>10mΩ typical)
29	$\overline{\text{PWRGD}}$	**Power Good Output.** This output pin enables a power module.
30	IGQ1	**Gate Current Quick Select Bit 1 Input.** This pin is used to change the gate current drive and is intended to allow for current ramp rate control of the gate pin of an external FET. It has an internal pulldown resistor. (>10mΩ typical)
31	IGQ0	**Gate Current Quick Select Bit 0 Input.** This pin is used to change the gate current drive and is intended to allow for current ramp rate control of the gate pin of an external FET. It has an internal pulldown resistor. (>10mΩ typical)
32	$\overline{\text{MRH}}$	**Manual Reset Input Hot-side.** Pulling the $\overline{\text{MRH}}$ pin LOW initiates a GATE pin reset (GATE pin pulled LOW). The $\overline{\text{MRH}}$ signal must be held LOW for 5µs (minimum).

Functional Description

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the bypass capacitors at the input of the board's power module or DC/DC converter can draw huge transient currents as they charge up (See Figure 30). This transient current can cause permanent damage to the board's components and cause transients on the system power supply.

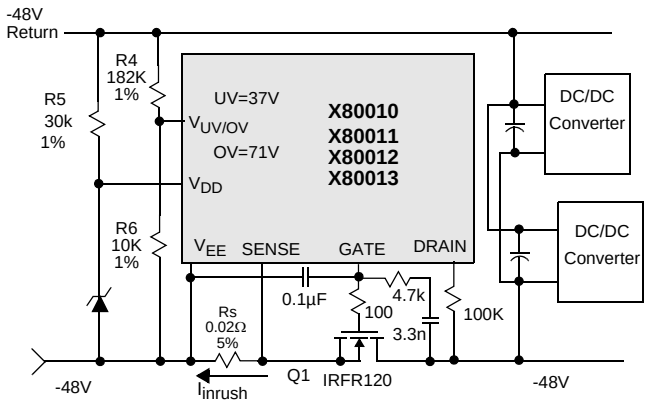


FIGURE 30. TYPICAL -48V HOTSWAP APPLICATION CIRCUIT

The X80010 is designed to turn on a board's supply voltage in a controlled manner (see Figure 31), allowing the board to be safely inserted or removed from a live backplane. The device also provides undervoltage, overvoltage and overcurrent protection while keeping the power module (DC/DC converter) off until the backplane input voltage is stable and within tolerance.

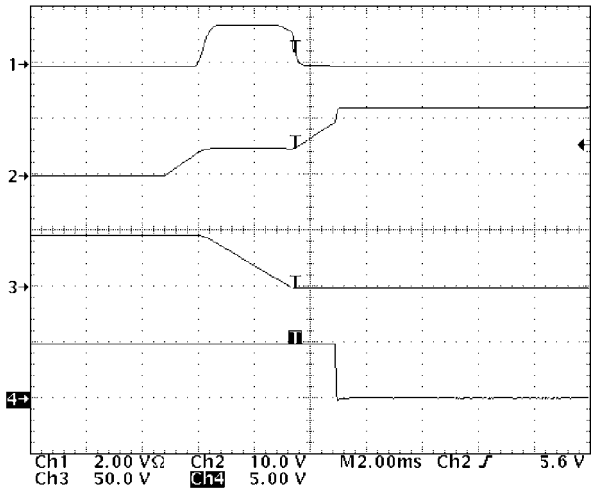


FIGURE 31. TYPICAL INRUSH WITH GATE SLEW RATE CONTROL

Overvoltage and Undervoltage Shutdown

The X80010 provides overvoltage and undervoltage protection circuits. When an overvoltage (V_{OV}) or undervoltage (V_{UV1} and V_{UV2}) condition is detected, the GATE pin immediately pulls low. The undervoltage threshold V_{UV1} applies to the normal operation with a mains supply. The undervoltage threshold V_{UV2} assumes the system is powered by a battery. When using a battery backup, the

BATT-ON pin is pulled to V_{RGO}. The default thresholds have been set so the external resistance values in Figure 30 provide an overvoltage threshold of 74.9V (X80010/X80012) or 68V (X80011/X80013), a main undervoltage threshold of 43V and a battery undervoltage threshold of 33.8V.

As shown in Figure 34, this circuit block contains comparators and voltage references to monitor for a single overvoltage and dual undervoltage trip points. The overvoltage and undervoltage trip points as shown in Table 1.

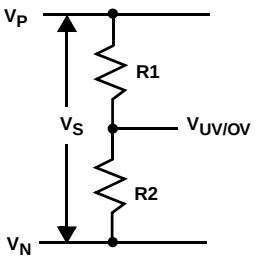
TABLE 1. OVERVOLTAGE/UNDERVOLTAGE DEFAULT THRESHOLDS

SYMBOL	DESCRIPTION	THRESHOLD FALLING	THRESHOLD RISING	MAX/MIN VOLTAGE[1]	LOCKOUT VOLTAGE[2]
V_{OV}	Overvoltage (X80010/12)	3.87V	3.9V	74.3	74.9
V_{OV}	Overvoltage (X80011/13)	3.51V	3.54V	67.4	68
V_{UV1}	Undervoltage 1	2.21V	2.24V	43.0	42.4
V_{UV2}	Undervoltage 2	1.73V	1.76V	33.8	33.2

Notes: 1: Max/Min Voltage is the maximum and minimum operating voltage assuming the recommended $V_{UV/OV}$ resistor divider.

2: Lockout voltage is the voltage where the X8001x turns off the FET.

A resistor divider connected between the plus and minus input voltages and the $V_{UV/OV}$ pin (see Figure 32) determines the overvoltage and undervoltage shutdown voltages and the operating voltage range. Using the thresholds in Table and the equations of Figure 32 the desired operating voltage can be determined. Figure 33 shows the resistance values for various operating voltages (X80010 and X80012).



Voltage divider:

$$V_{UV/OV} = V_S\left(\frac{R2}{R1 + R2}\right)$$

or:

$$V_S = V_{UV/OV}\left(\frac{R1 + R2}{R2}\right)$$

FIGURE 32. OVERVOLTAGE UNDERVOLTAGE DIVIDER

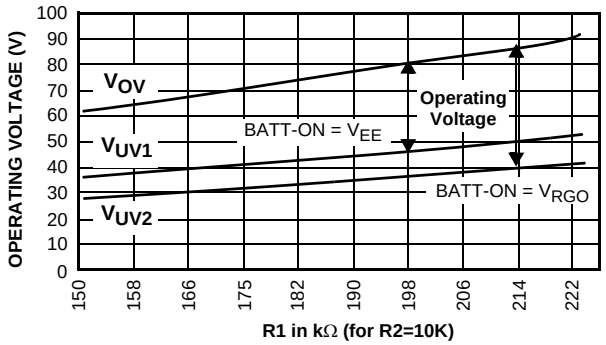


FIGURE 33. OPERATING VOLTAGe vs RESISTOR RATIO

Battery Back Up Operations

An external signal, BATT_ON is provided to switch the undervoltage trip point. The BATT_ON signal is a LOGIC HIGH if $V_{IHB} > V_{EE} + 4V$ and is a LOGIC LOW if $V_{ILB} < V_{EE} + 2V$. The time from a BATT_ON input change to a valid new undervoltage threshold is 100ns. See Electrical Specifications for more details.

Note: The $V_{UV/OV}$ pin must be limited to less than V_{EE} + 5.5V in worst case conditions. Values for R1 and R2 must be chosen such that this condition is met. Intersil recommends R1 = 182kΩ and R2 = 10kΩ to conform to factory settings.

TABLE 2. SELECTING BETWEEN UNDERVOLTAGE TRIP POINTS

PIN	DESCRIPTION	TRIP POINT SELECTION
BATT_ON	Undervoltage Trip Point Selection Pin	If BATT_ON = 0, V_{UV1} trip point is selected; If BATT_ON = 1, V_{UV2} trip point is selected.

V_{UV1} and V_{UV2} are undervoltage thresholds.

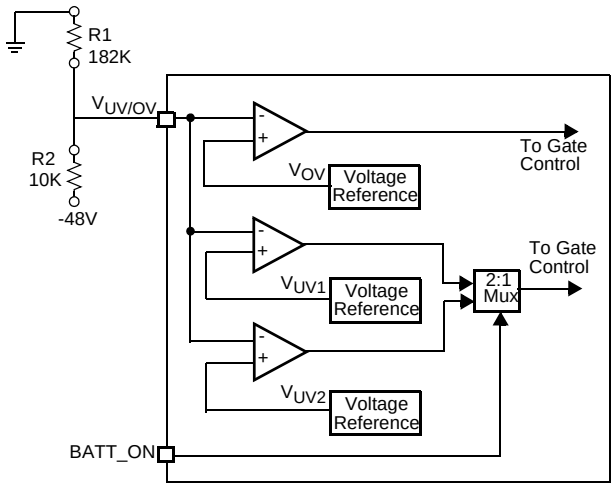


FIGURE 34. OVERVOLTAGE UNDERVOLTAGE FOR PRIMARY AND BATTERY BACKUP

Overcurrent Protection (Circuit Breaker Function)

The X80010 over-current circuit provides the following functions:

- Over-current shut-down of the power FET and external power good indicators.
- Noise filtering of the current monitor input.
- Relaxed over-current limits for initial board insertion.
- Over-current recovery retry operation.

A sense resistor, placed in the supply path between V_{EE} and SENSE (see Figure 30) generates a voltage internal to the X80010. When this voltage exceeds 50mV an over current condition exists and an internal “circuit breaker” trips, turning off the gate drive to the external FET. The actual over-current level is dependent on the value of the current sense resistor. For example a 20mΩ sense resistor sets the over-current level to 2.5A.

Intersil’s X80010 provides a safety mechanism during insertion of the board into the back plane. During insertion of the board into the backplane large currents may be induced. In order to prevent premature shut down, the overcurrent detect circuit of the X80010 allows up to 3 times the standard overcurrent setting during insertion.

After the $\overline{\text{PWRGD}}$ signal is asserted, the X80010 switches back to the normal overcurrent setting. The over-current threshold voltage during insertion is 150mV.

After the Power FET turns off due to an over-current condition, a retry circuit turns the FET back on after a delay of 100ms. If the over-current condition remains, the FET again turns off. For the X80010 and X80012, this sequence repeats indefinitely until the over-current condition is released. For the X80011 and X80013, the X80010 retries five times, then, sets an output signal, $\overline{\text{FAR}}$, to indicate a failure after retry.

Over-current shut-down

As shown in Figure 35, this circuit block contains a resistor divider, a comparator, a noise filter and a voltage reference to monitor for over-current conditions.

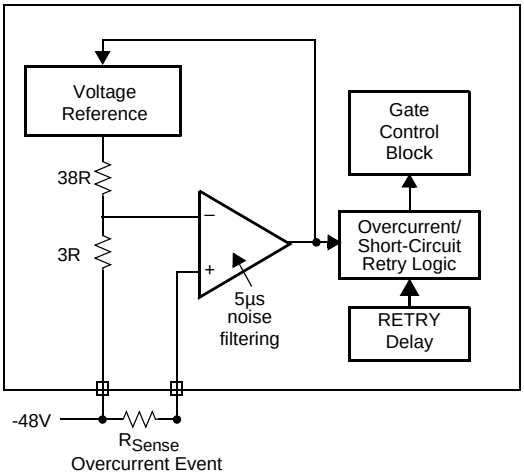


FIGURE 35. OVERCURRENT DETECTION/SHORT CIRCUIT PROTECTION

The overcurrent voltage threshold (V_{OC}) is 50mV. This can be factory set, by special order, to any setting between 30mV and 100mV. V_{OC} is the voltage between the SENSE and V_{EE} pins and across the R_{SENSE} resistor. If the selected sense resistor is 20mW, then 50mV corresponds to an overcurrent of 2.5A.

If an over-current condition is detected, the GATE is turned off and all power good indicators go inactive.

Overcurrent Noise Filter

The X80010 has a noise (low pass) filter built into the over-current comparator. The comparator will thus require the current spikes to exceed the overcurrent limit for more than 5µs.

Overcurrent During Insertion

Insertion is defined as the first plug-in of the board to the backplane. In this case, the X80010 is initially fully powered off prior to the hot plug connection to the mains supply. This condition is different from a situation where the mains supply has temporarily failed resulting in a partial recycle of the power. This second condition will be referred to as a power cycle.

During insertion, the board can experience high levels of current for short periods of time as power supply capacitors charge up on the power bus. To prevent the over-current sensor from turning off the FET inadvertently, the X80010 has the ability to allow more current to flow through the powerFET and the sense resistor for a short period of time until the FET turns on and the $\overline{\text{PWRGD}}$ signal goes active. In the X80010, 150mV is allowed across sense resistor the during insertion (10A assuming a 20mΩ resistor). This provides a mechanism to reduce insertion issues associated with huge current surges.

Hardshort Protection - FET Turn-on Retry

In the event on an over-current or hard short condition, the X80010 includes a retry circuit. This circuit waits for 100ms, then attempts to again turn on the FET. If the fault condition still exists, the FET turns off and the sequence repeats. For the X80010 and X80012, this process continues indefinitely until the overcurrent condition does not exist. For the X80011 and X80013, this process repeats five times, only then will keep the FET off and set the $\overline{FAR}$ pin active. After $\overline{FAR}$ is asserted, it can be cleared using the master reset pin, $\overline{MRH}$ (upon $\overline{MRH}$ assertion the $\overline{FAR}$ output is cleared) or cycling the power on V_{DD}.

If an overcurrent condition does not occur on any retry, the gate pin proceeds to open at the user defined slew rate.

Gate Drive Output Slew Rate (Inrush Current) Control

The gate output drives an external N-Channel FET. The GATE pin goes high when no overcurrent, undervoltage or overvoltage conditions exist.

The X80010 provides an I_{GATE} current of 50µA to provide on-chip slew rate control to minimize inrush current. This I_{GATE} current limits the inrush current and provides the best charge time for a given load, while avoiding overcurrent conditions.

For applications that require different ramp rates during insertion and start-up and operations modes, the X80010 provides two external pins, IGQ1 and IGQ0, that allow the user to switch to different GATE currents on-the-fly by selecting one of four pre-selected I_{GATE} currents. When IGQ0 and IGQ1 are left unconnected, the gate current is 50µA. The other three settings are 10µA, 70µA and 150µA (See Figure 36). Typically, the delay from IGQ1 and IGQ0 selection to a change in the GATE pin current is less than 1µs.

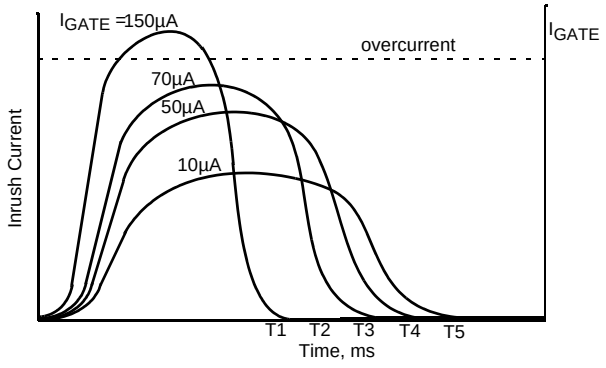


FIGURE 36. SELECTING I_{GATE} CURRENT FOR SLEW RATE CONTROL ON THE GATE PIN

Slew Rate (Gate) Control

As shown in Figure 37, this circuit block contains a current source (I_{GATE}) that drives the 50µA current into the GATE pin. This current provides a controlled slew rate for the FET.

For applications that require different ramp rates during insertion and operation or for applications where a different gate current is desired, the X80010 provides two external pins, IGQ1 and IGQ0, that allow the system to switch to a different GATE current with pre-selected options.

The IGQ1 and IGQ0 pins can be used to select from one of four set values.

IGQ1 PIN	IGQ0 PIN	CONTENTS
0	0	Defaults to gate current 50µA
0	1	Gate Current is 10µA
1	0	Gate Current is 70µA
1	1	Gate Current is 150µA

Typically, the delay from IGQ1 and IGQ0 selection to a change in the GATE pin current is less than 1µs.

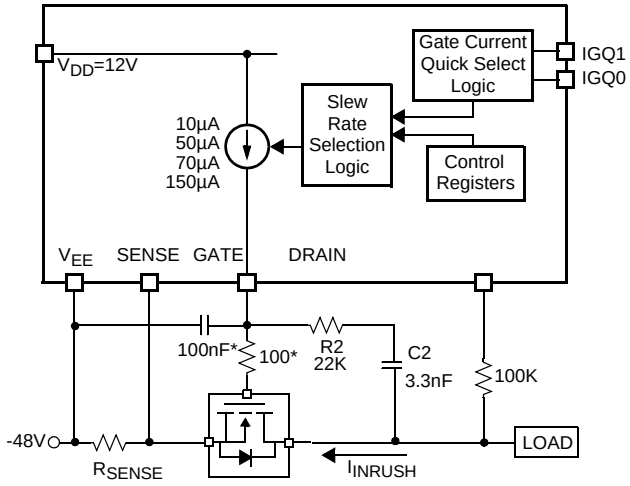


FIGURE 37. SLEW RATE (INRUSH CURRENT) CONTROL

Gate Capacitor, Filtering and Feedback

In Figure 37, the FET control circuit includes an FET feedback capacitor C_2, which provides compensation for the FET during turn on. The capacitor value depends on the load, the FET gate current, and the maximum desired inrush current.

The value of C2 can be selected with the following formula.

$$C2 = \frac{I_{GATE} \times C_{LOAD}}{I_{INRUSH}}$$

Where:

I_{GATE} = FET Gate current

I_{INRUSH} = Maximum desired inrush current

C_{LOAD} = DC/DC bulk capacitance

With the X80010, there is some control of the gate current with the IGQ pins, so one selection of C2 can cover a wide range of possible loading conditions. Typical values for C2 range from 2.2 to 4.7nF.

When power is applied to the system, the FET tries to turn on due to its internal gate to drain capacitance (Cgd) and the feedback capacitor C2 (see Figure 37.) The X80010 device, when powered, pulls the gate output low to prevent the gate voltage from rising and keep the FET from turning on. However, unless V_{DD} powers up very quickly, there will be a brief period of time during initial application of power when the X80010 circuits cannot hold the gate low. The use of an external capacitor (C1) prevents this. Capacitors C1 and C2 form a voltage divider to prevent the gate voltage from rising above the FET turn on threshold before the X80010 can hold the gate low. Use the following formula for choosing C1.

$$C1 = \frac{V1 - V2}{V2} C2$$

Where:

V1 = Maximum input voltage,

V2 = FET threshold voltage,

C1 = Gate capacitor,

C2 = Feedback capacitor.

In a system where V_{DD} rises very fast, a smaller value of C1 may suffice as the X80010 will control voltage at the gate before the voltage can rise to the FET turn on threshold. The circuit of Figure 37 assumes that the input voltage can rise to 80V before the X80010 sees operational voltage on V_{DD}. If C1 is used then the series resistor R1 will be required to prevent high frequency oscillations.

Drain Sense and Power Good Indicator

The X80010 provides a drain sense and power good indicator circuit. The $\overline{PWRGD}$ signal asserts LOW when there is no overvoltage, no undervoltage, and no overcurrent condition, the Gate voltage exceeds VDD-1V, and the voltage at the DRAIN pin is less $V_{EE}+V_{DRAIN}$.

As shown in Figure 38, this circuit block contains a drain sense voltage trip point (ΔV_{DRAIN}) and a gate voltage trip point (ΔV_{GATE}), two comparators, and internal voltage references. These provide both a drain sense and a gate sense circuit to determine the whether the FET has turned on as requested. If so, the power good indicator ($\overline{PWRGD}$) goes active.

The drain sense circuit checks the DRAIN pin. If the voltage on this pin is greater that 1V above V_{EE}, then a fault condition exists.

The gate sense circuit checks the GATE pin. If the voltage on this pin is less than V_{EE} - 1V, then a fault condition exists.

The $\overline{PWRGD}$ signal asserts (Logic LOW) only when all of the below conditions are true:

- there is no overvoltage or no undervoltage condition, (i.e. undervoltage < V_{EE} < overvoltage.)
- There is no overcurrent condition (i.e. V_{EE} - V_{SENSE} < V_{OC}.)
- The FET is turned on (i.e. V_{DRAIN} < V_{EE} + 1V and V_{GATE} > V_{DD} - 1V).

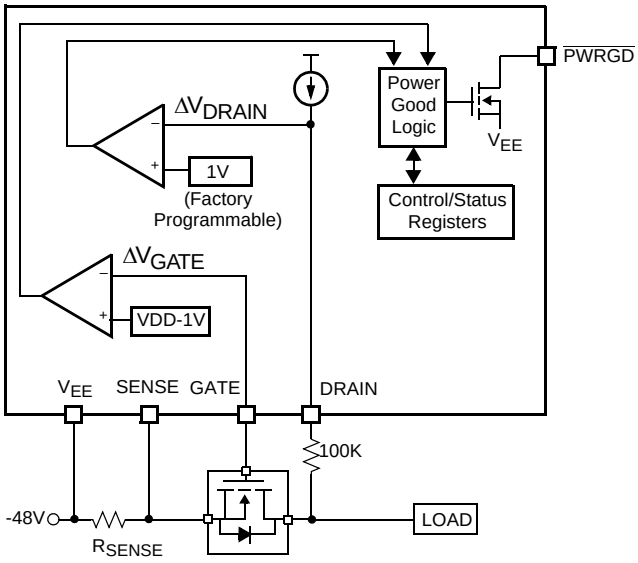


FIGURE 38. DRAIN SENSE AND POWER GOOD INDICATOR

Power On/System Reset and Delay

Application of power to the X80010 activates a Power On Reset circuit that pulls the $\overline{RESET}$ pin active. This signal, if used, provides several benefits.

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It allows time for an FPGA to download its configuration prior to initialization of the circuit.

The POR/RESET circuit is activated when all voltages are within specified ranges and the following time-out conditions are met: $\overline{PWRGD}$ and $\overline{V1GOOD}$, $\overline{V2GOOD}$, $\overline{V3GOOD}$, and $\overline{V4GOOD}$. The POR/RESET circuit will then wait 100ms and assert the $\overline{RESET}$ pin.

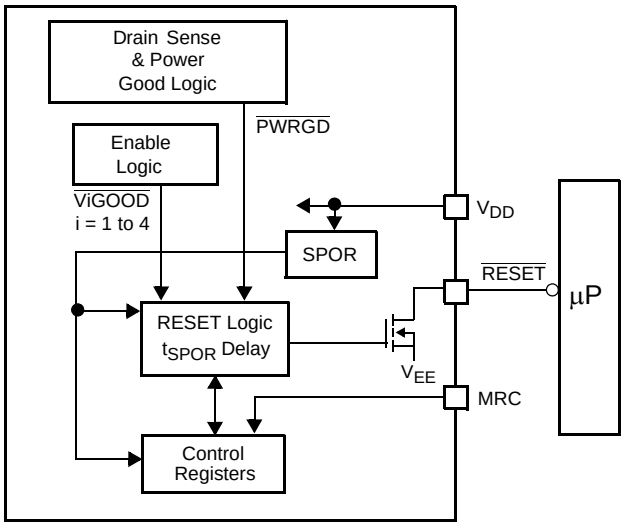


FIGURE 39. POWER ON/SYSTEM RESET AND DELAY

Once the $\overline{PWRGD}$ signal is asserted, the power sequencing of the DC/DC modules can commence. $\overline{RESET}$ goes active 100ms after all $\overline{ViGOOD}$ (i=1 to 4) outputs are asserted (See Figure 39).

As shown in Figure 40, this circuit block contains four separate voltage enable pins, a time delay circuit, and an output driver.

Quad Voltage Monitoring

X80010 monitors 4 voltage enable inputs. When the $\overline{ENi}$ (i=1-4) input is detected to be below the input threshold, the output $\overline{ViGOOD}$ (i = 1 to 4) goes active LOW. The $\overline{ViGOOD}$ signal is asserted after a delay of 100ms. The $\overline{ViGOOD}$ signal remains active until $\overline{ENi}$ rises above threshold.

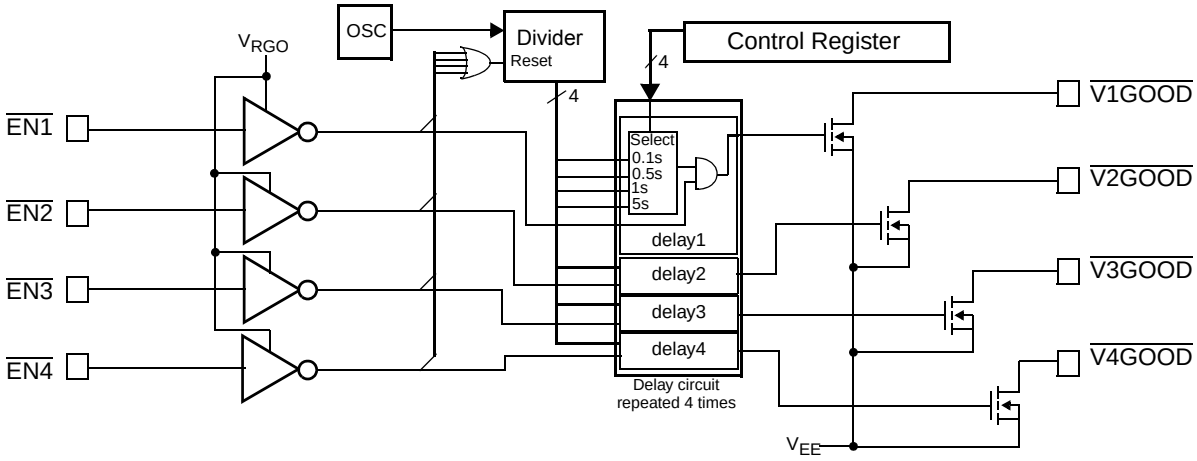


FIGURE 40. VOLTAGE MONITORS AND VGOOD OUTPUTS

Manual Reset (Hot Side and Cold Side)

The manual reset option allows a hardware reset of either the Gate control or the $\overline{PWRGD}$ indicator. These can be used to recover the system in the event of an abnormal operating condition.The X80010 has two manual reset pins: $\overline{MRH}$ (manual reset hot side) and MRC (manual reset cold side). The $\overline{MRH}$ signal is used as a manual reset for the GATE pin. This pin is used to initiate Soft Reinsert. When $\overline{MRH}$ is pulled LOW the GATE pin will be pulled LOW. It also clears the $\overline{FAR}$ signal. When the $\overline{MRH}$ pin goes HIGH, it removes the override signal and the gate will turn on based on the selected gate control mechanism.

TABLE 3. MANUAL RESET OF THE HOT SIDE (GATE SIGNAL)

MRH	GATE PIN	REQUIREMENTS
1	Operational	When $\overline{MRH}$ is HIGH the Manual Reset (Hot) function is disabled
0	OFF	$\overline{MRH}$ must be held LOW minimum of 5µs

The MRC signal is used as a manual reset for the $\overline{PWRGD}$ signal. This pin is used to initiate a Soft Restart. When the MRC is pulled HIGH, the $\overline{PWRGD}$ signal is pulled HIGH. When MRC pin goes LOW, the $\overline{PWRGD}$ pin goes operational. It will go LOW if all constraints on the GATE are within limits.

TABLE 4. MANUAL RESET OF THE COLD SIDE ($\overline{PWRGD}$ SIGNAL)

MRC	PWRGD	REQUIREMENTS
1	HIGH	MRC must be held HIGH minimum of 5µs
0	Operational	When MRC is LOW the MRC function is disabled

Flexible Power Sequencing of Multiple Power Supplies

The X80010 provides several circuits such as multiple voltage enable pins, programmable delays, and a power good signals can be used to set up flexible power sequencing schemes for downstream DC/DC supplies. Below are examples of parallel and relay sequencing.

1. Power Up of DC/DC Supplies In Parallel Sequencing Using Programmable Delays on Power Good (See Figure 41 and Figure 42).

   Several DC/DC power supplies and their respective power up start times can be controlled using the X80010 such that each of the DC/DC power supplies will start up following the issue of the $\overline{PWRGD}$ signal. The $\overline{PWRGD}$ signal is fed into the $\overline{ENi}$ inputs to the X80010. When $\overline{PWRGD}$ is valid, the internal voltage enable circuits issue $\overline{ViGOOD}$ signals after a time delay. The $\overline{ViGOOD}$ signals control the ON/OFF pins of the DC/DC supplies. Each DC/DC converter is instructed to turn on 100ms after the $\overline{PWRGD}$ goes active. However, each $\overline{ViGOOD}$ delay can be increased with the use of external R-C circuits.

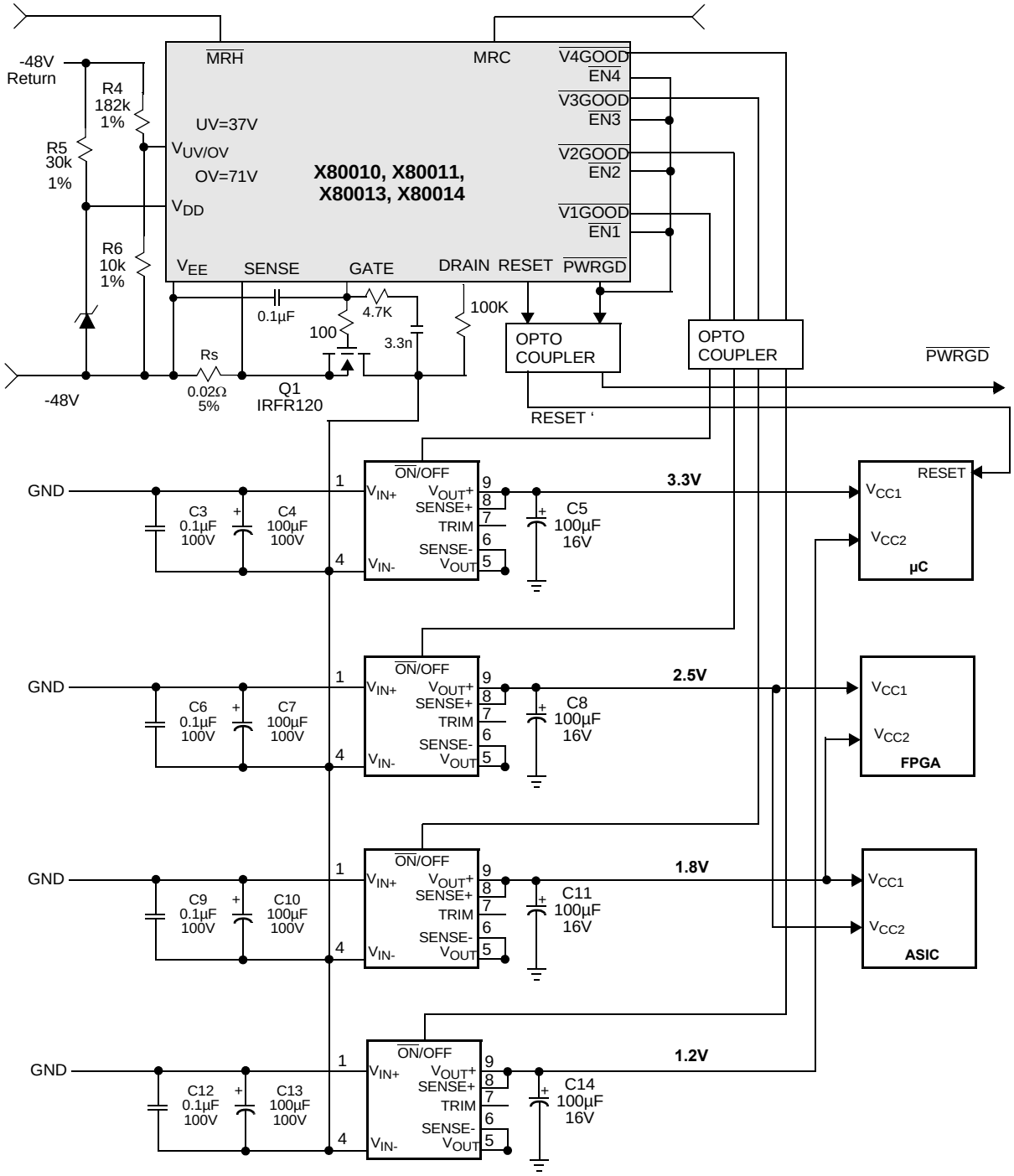


FIGURE 41. TYPICAL APPLICATION OF HOTSWAP AND DC/DC PARALLEL POWER SEQUENCING

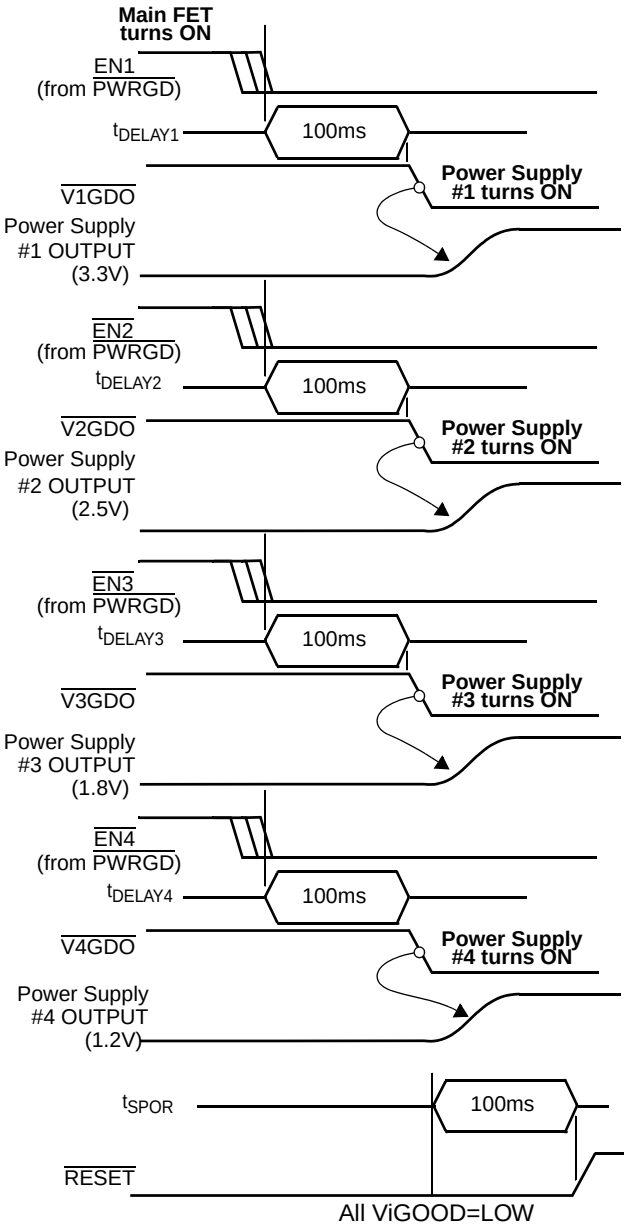


FIGURE 42. PARALLEL SEQUENCING OF DC/DC SUPPLIES. (TIMING)

1. Power Up of DC/DC Supplies Via Relay Sequencing Using Power Good and Voltage Monitors (see Figure 43 and Figure 44).

   Several DC/DC power supplies and their respective power up start times can be controlled using the X80010 such that each of the DC/DC power supplies will start in a relay sequencing fashion. The 1st DC/DC supply will power up when $\overline{PWRGD}$ is LOW after a 100ms delay. Subsequent DC/DC supplies will power up after the prior supply has reached its operating voltage. One way to do this is by using an external CPU Supervisor (for example the Intersil X40430) to monitor the DC/DC output. When the DC/DC voltage is good, the supervisor output signals the X80010 $\overline{EN1}$ input to sequence the next supply. An opto-coupler is recommended in this connection for isolation. This configuration ensures that each subsequent DC/DC supply will power up after the preceding DC/DC supply voltage output is valid.

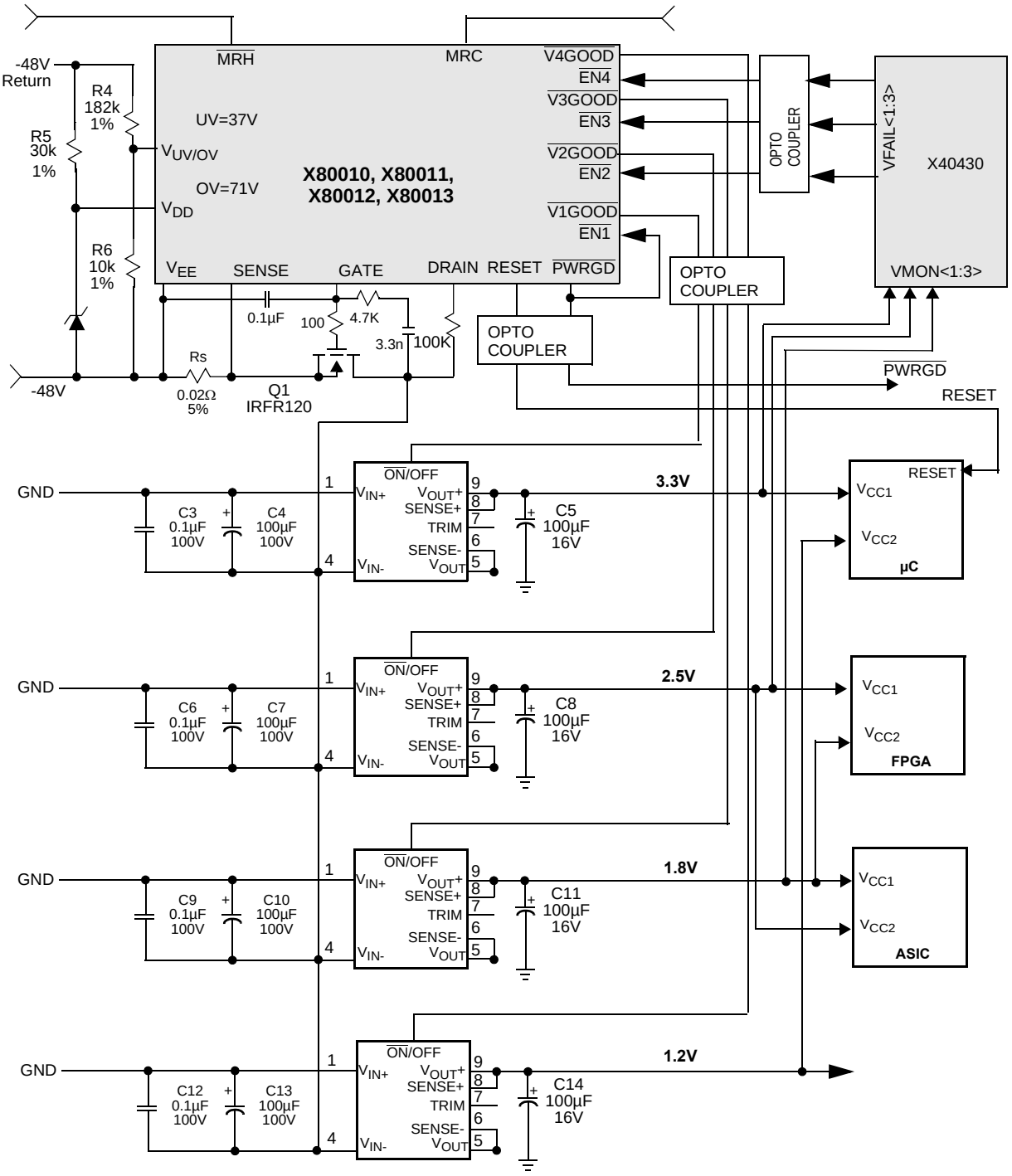


FIGURE 43. TYPICAL APPLICATION OF HOTSWAP AND DC/DC RELAY SEQUENCING

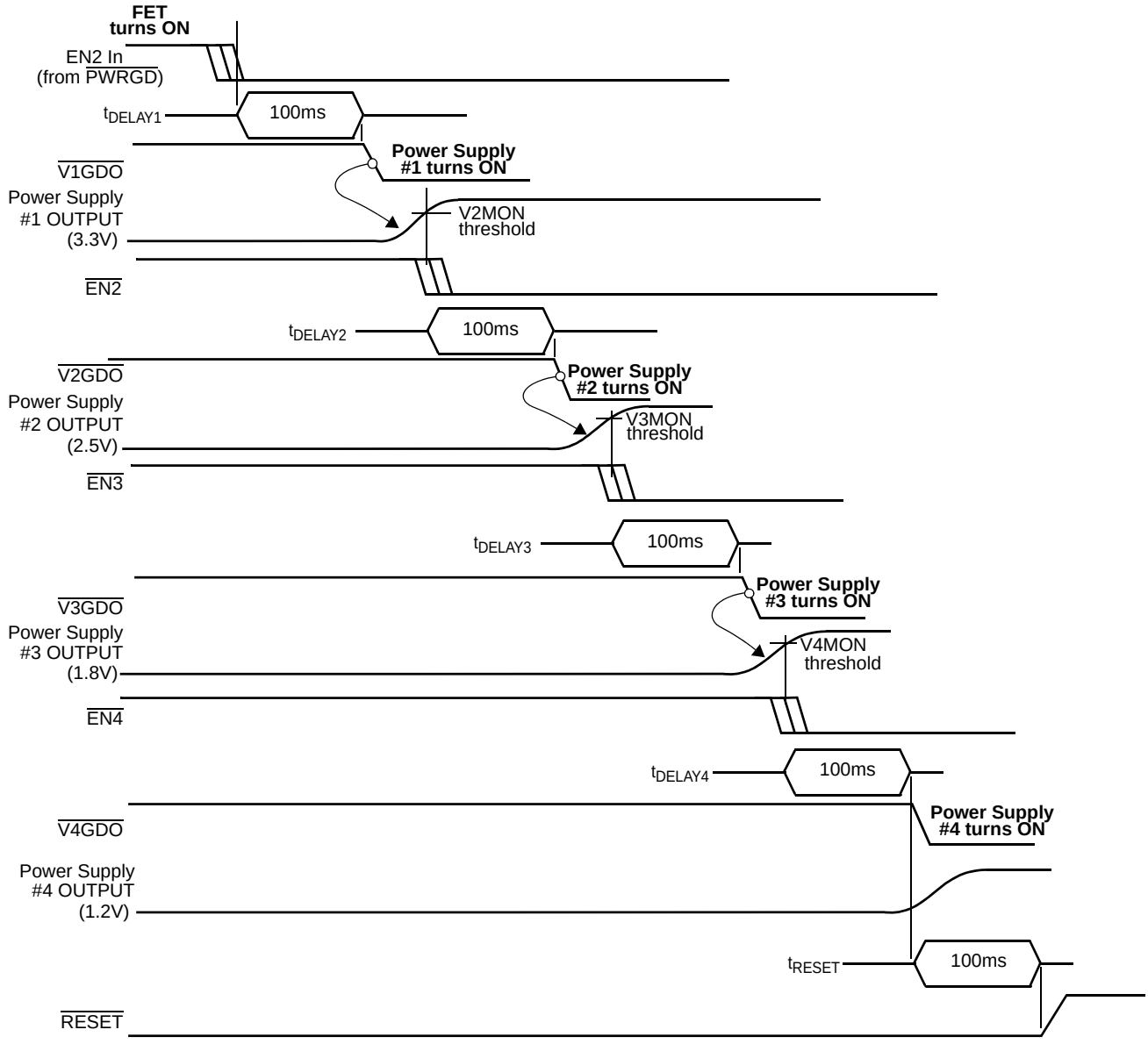


FIGURE 44. RELAY SEQUENCING OF DC/DC SUPPLIES. (TIMING)

Packaging Information

32-Lead Very Very Thin Quad Flat No Lead Package
7mm x 7mm Body with 0.65mm Lead Pitch