MAS9270

IC FOR 10.00 – 30.00 MHz VCTCXO

- **Wide Supply Voltage Range**
- **True Sine Wave Output**
- **Very High Level of Integration**
- **Electrically Trimmable**
- **Very Low Phase Noise**
- **Low Cost**
- **Minimum Operating Temperature –40 °C**

DESCRIPTION

The MAS9270 is an integrated circuit well suited to build VCTCXO for mobile communication. Temperature calibration is achieved in three calibration temperatures only. The trimming is done through a serial bus and the calibration information is stored in an internal PROM. This means no rework for trimming is needed.

To build a VCTCXO additionally only crystal is required. The compensation method is fully analog, working continuously without generating any steps or other interference.

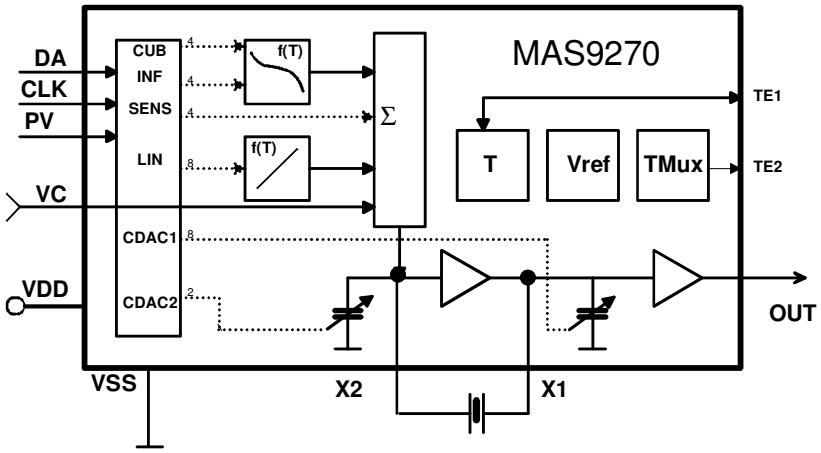
FEATURES

- Very small size
- Minor current draw
- Wide operating temperature range
- Phase noise <-120 dBc/Hz at 100Hz offset
- Programmable VC-sensitivity
- Minimum Operating Temperature –40 °C for MAS9270Cxx3

APPLICATIONS

- VCTCXO for mobile phones
- VCTCXO for other telecommunications systems

BLOCK DIAGRAM



PIN DESCRIPTION

Pin Description	Symbol	x-coordinate	y-coordinate
Power Supply Voltage	VDD	166	1430
Programming Input	PV	420	1435
Serial Bus Clock Input	CLK	979	1441
Serial Bus Data Input	DA	1234	1441
Temperature Output	TE1	1488	1441
Test Multiplexer Output	TE2	1742	1441
Voltage Control Input	VC	185	153
Crystal Oscillator Output	X1	439	149
Crystal/Varactor Oscillator Input	X2	1357	149
Power Supply Ground	VSS	1790	166
Buffer Output	OUT	2046	153

Note: Because the substrate of the die is internally connected to GND, the die has to be connected to GND or left floating. Make sure that GND is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.
Note: Pad coordinates are measured from the left bottom corner of the chip to the center of the pads. The coordinates may vary depending on sawing width and location, however, distances between pads are accurate.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD} - V_{SS}	-0.3	6.0	V	
Input Pin Voltage		V_{SS} -0.3	V_{DD} + 0.3	V	1)
Power Dissipation	P_{MAX}		20	mW	
Storage Temperature	T_{ST}	-55	150	°C	

Note 1: Not valid for programming pin PV

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}		2.7	2.8	5.5	V	1)
Supply Current	I_{CC}	Vdd = 2.8 Volt			1.8	mA	
Operating Temperature	T_{OP}		-30		+85	°C	2)
Storage Temperature	T_S	Relative humidity = 15%…70%	-45		+40	°C	
Crystal Pulling Sensitivity	S			30		ppm/pF	
Crystal Load Capacitance	C_L			10		pF	

Note 1: Minimum Supply Voltage 2.6 V for MAS9270Cxx2 version.
Note 2: Minimum Operating Temperature –40 °C for MAS9270Cxx3 version.

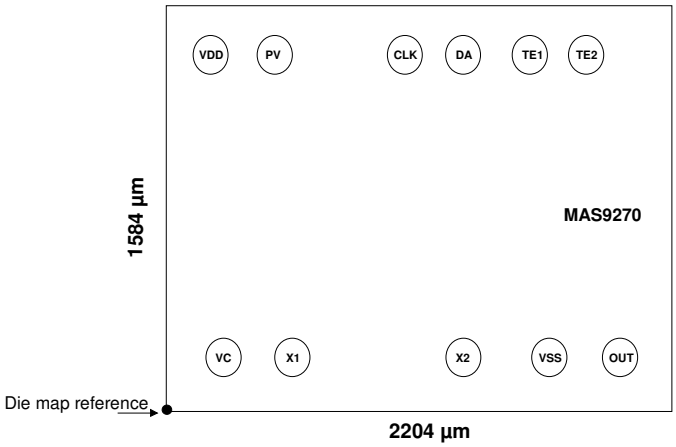
ELECTRICAL CHARACTERISTICS

(recommended operation conditions)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Frequency Range	f_o	10.00		30.00	MHz	
Voltage Control Range	V_C	0		Vdd	V	
Voltage Control Sensitivity (VCR = 0)	V_{CSENS}	9		15	ppm/V	1)
Voltage Control Sensitivity (VCR = 1)	V_{CSENS}	4		8	ppm/V	
Frequency vs. Supply Voltage	df_o			±0.2	ppm	2)
Frequency vs. Load Change	df_o			±0.2	ppm	3)
Output Voltage (10kΩ // 10 pF)	V_{out}		1.0		Vpp	
Compensation Range ± 2.5 ppm	T_C	-30		85	°C	
Compensation Range ± 2.0 ppm	T_C	-25		75	°C	
Compensation Range ± 2.5 ppm	T_C	-40		85	°C	4)
Compensation Range Linear Part	a1	-0.7		0.0	ppm/K	
Compensation Inflection Point	INF	25		31	°C	
Compensation Range Cubic Part	a3		95		ppm^2/K^3	
Compensation CDAC1 (7 Bit)	C_{X1}	C10		C10 + 18	pF	5)
Compensation CDAC2 (2 Bit)	C_{X2}	C20		C20 + 4	pF	6)
Start up Time	T_{START}		2		ms	

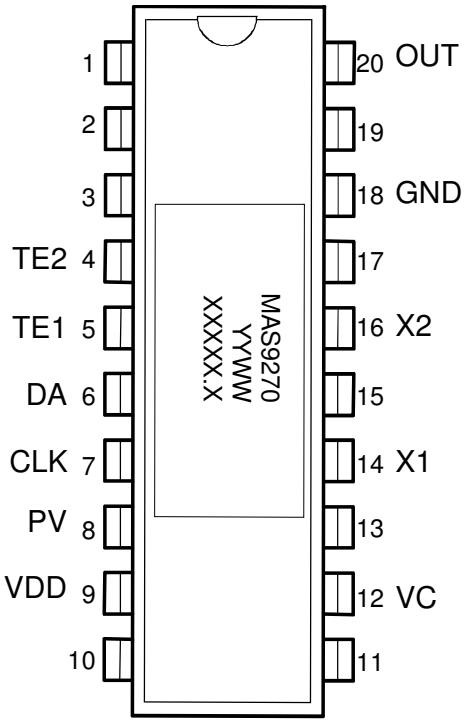
Note 1: default
Note 2: VDD +/- 5%
Note 3: R=10 kohm +/- 10%, C=10 pF +/- 10%
Note 4: MAS9270Cxx3
Note 5: typ C10 = 13 pF
Note 6: typ C20 = 6 pF (varactor capacitance at 1.8 V 12 pF)

IC OUTLINES



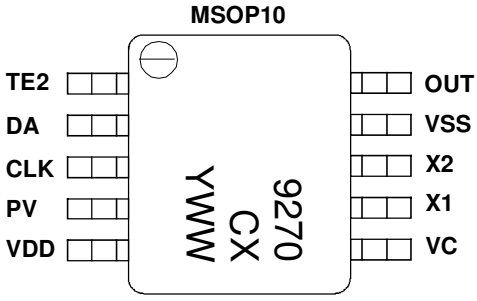
Note 1: MAS9270 pads are round with 80 µm diameter at opening.
Note 2: Pins CLK and DA can either be connected to VSS or left floating, pin PV can either be connected to VDD or left floating and pin TE1 must be left floating in VCTCXO module end-user application.
Note 3: Die map reference is the actual left bottom corner of the sawn chip.

SAMPLES IN SB20 DIL PACKAGE



Top marking:
YYWW = Year, Week
XXXXX.X = Lot number

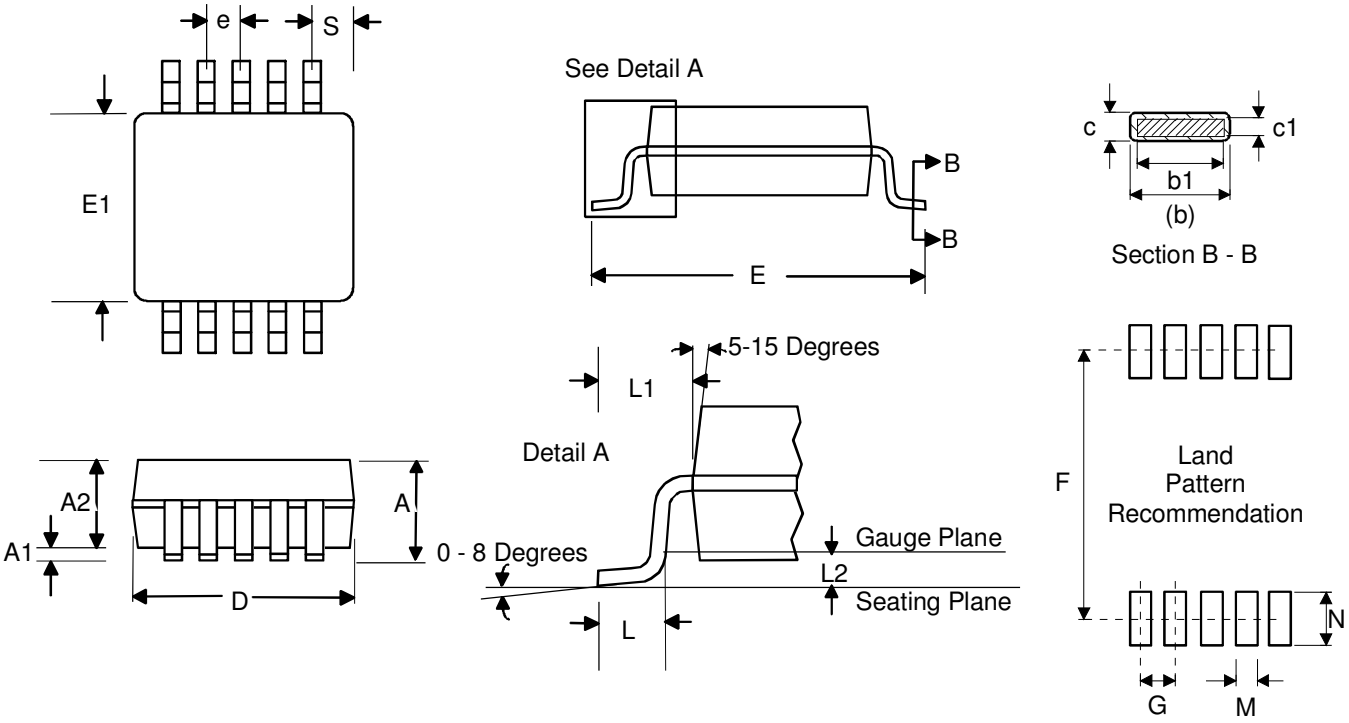
DEVICE OUTLINE CONFIGURATION



Top View

C = product version
X = voltage version
Y = year
WW= week

PACKAGE (MSOP-10) OUTLINE



Symbol	Min	Nom	Max	Unit
A	--	--	1.10	mm
A1	0.00	--	0.15	mm
A2	0.75	0.85	0.95	mm
b	0.15	--	0.30	mm
b1	0.15	---	0.25	mm
c	0.08		0.23	mm
c1	0.08		0.18	mm
D		3.00 BSC		mm
E		4.90 BSC		mm
E1		3.00 BSC		mm
e		0.50 BSC		mm
F		4.8		mm
G		0.50		mm
L (Terminal length for soldering)	0.40	0.60	0.80	mm
L1		0.95 REF		
L2		0.25 BSC		mm
M		0.41		mm
N		1.02		mm
S		0.50		Mm

Dimensions do not include mold or interlead flash, protrusions or gate burrs.
Reference Standard : JEDEC MO-187 BA.

SOLDERING INFORMATION

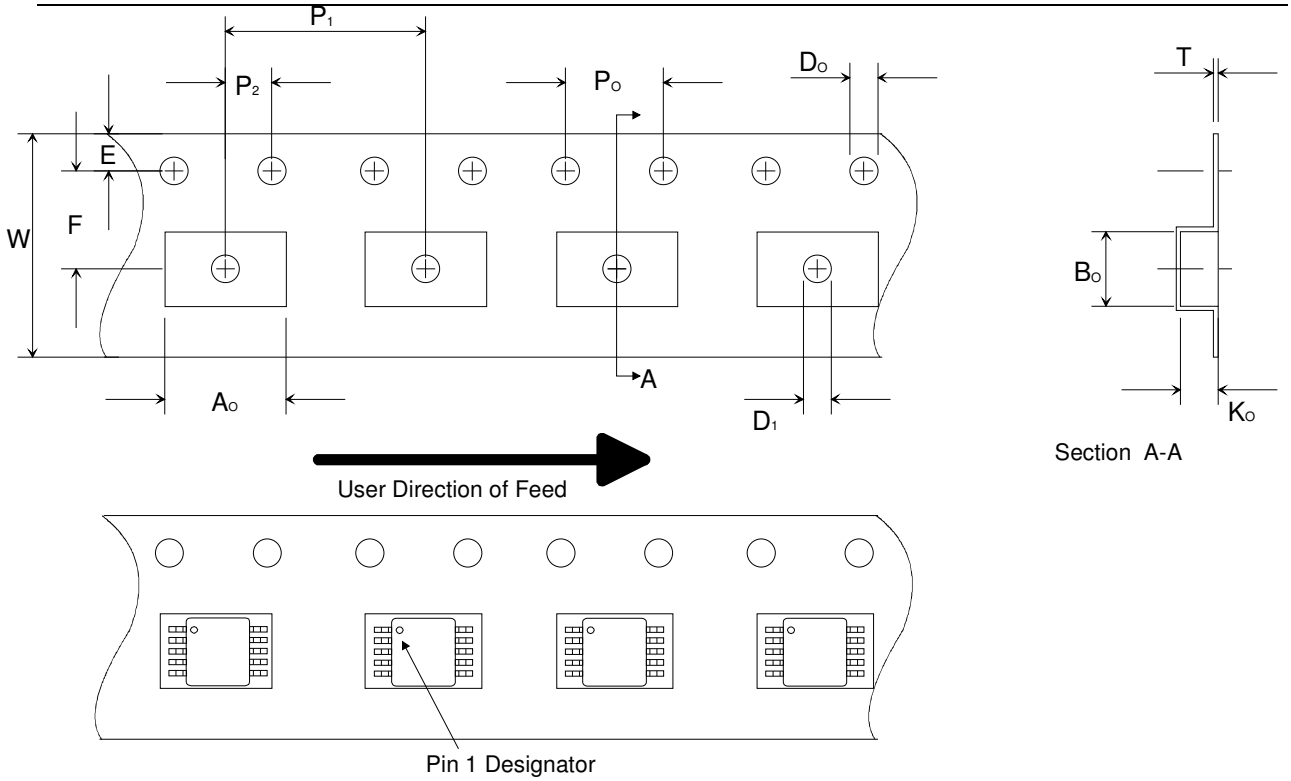
◆ **For Sn/Pb MSOP-10**

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20 2*220°C
Maximum Temperature	240°C
Maximum Number of Reflow Cycles	2
Reflow profile	Thermal profile parameters stated in JESD22-A113 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Sn 85% Pb 15%

◆ **For Pb Free, RoHS Compliant MSOP-10**

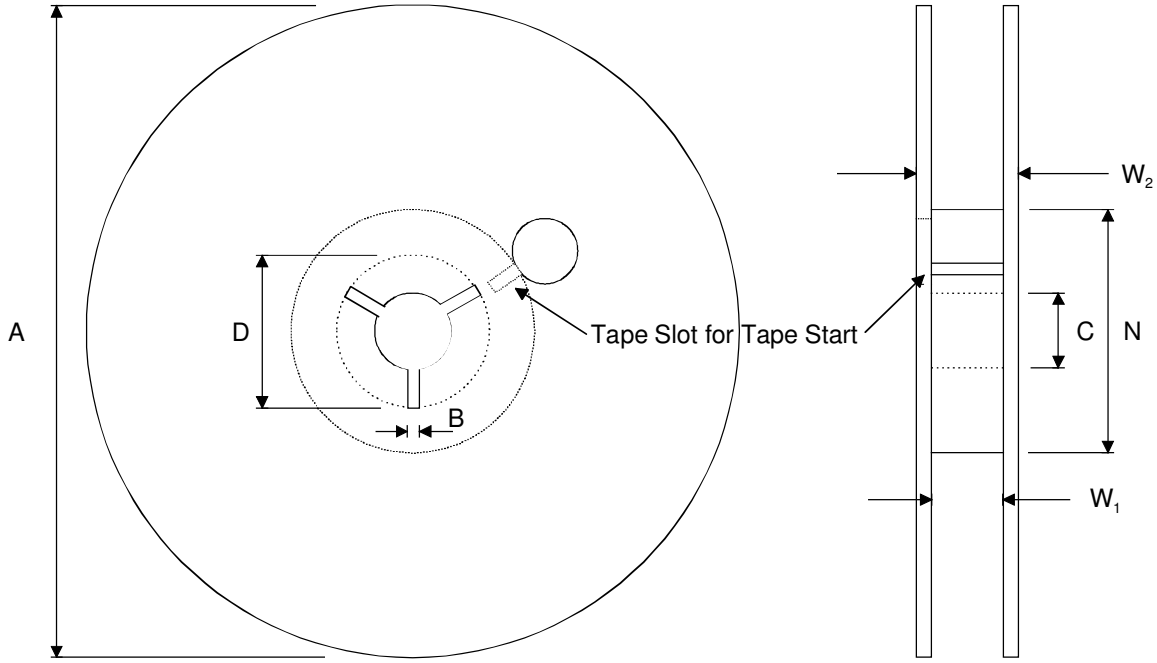
Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

EMBOSSED TAPE SPECIFICATIONS

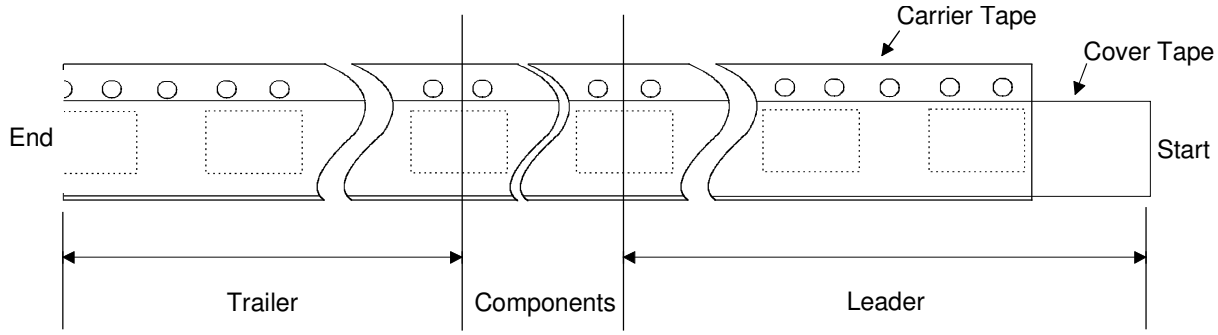


Dimension	Min/Max	Unit
Ao	5.00 ±0.10	mm
Bo	3.20 ±0.10	mm
Do	1.50 +0.1/-0.0	mm
D1	1.50 min	mm
E	1.75	mm
F	5.50 ±0.05	mm
Ko	1.45 ±0.10	mm
Po	4.0	mm
P1	8.0 ±0.10	mm
P2	2.0 ±0.05	mm
T	0.3 ±0.05	mm
W	12.00 +0.30/-0.10	mm

REEL SPECIFICATIONS



5000 Components on Each Reel
Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS9270CTB1	VCTCXO IC 2.7 V	EWS Tested wafers 480 µm	Die Size 2.204 x 1.584 mm
MAS9270CTG1	VCTCXO IC 2.7 V	EWS Tested wafers 215 µm	Die Size 2.204 x 1.584 mm
MAS9270CASN06	VCTCXO IC 2.7 V	Green MSOP-10, Pb Free, RoHS Compliant/Top Marking CA	Tape & Reel, 5.000 pcs/reel
MAS9270CTB2	VCTCXO IC 2.6 V	EWS Tested wafers 480 µm	Die Size 2.204 x 1.584 mm
MAS9270CTG2	VCTCXO IC 2.6 V	EWS Tested wafers 215 µm	Die Size 2.204 x 1.584 mm
MAS9270C2SN06	VCTCXO IC 2.6 V	Green MSOP-10, Pb Free, RoHS Compliant /Top Marking C2	Tape & Reel, 5.000 pcs/reel
MAS9270CTB3	VCTCXO IC –40 °C	EWS Tested wafers 480 µm	Die Size 2.204 x 1.584 mm
MAS9270CTG3	VCTCXO IC –40 °C	EWS Tested wafers 215 µm	Die Size 2.204 x 1.584 mm
MAS9270C3SN06	VCTCXO IC –40 °C	Green MSOP-10, Pb Free, RoHS Compliant /Top Marking C3	Tape & Reel, 5.000 pcs/reel

Please contact Micro Analog Systems Oy for other wafer thickness options.

LOCAL DISTRIBUTOR

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