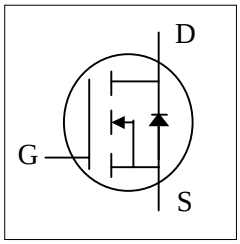
AP94T07GMT-HF

Halogen-Free Product

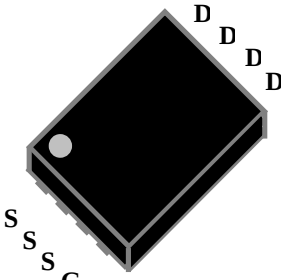
Advanced Power Electronics Corp.

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **Simple Drive Requirement**
- ▼ **SO-8 Compatible with Heatsink**
- ▼ **Low On-resistance**
- ▼ **RoHS Compliant & Halogen-Free**



BV_{DSS}	75V
$R_{DS(ON)}$	7.5mΩ
I_D	65A



PMPAK® 5x6

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The PMPAK® 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	75	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current (Chip)	65	A
I_D@T_A=25℃	Continuous Drain Current[3]	18.4	A
I_D@T_A=70℃	Continuous Drain Current[3]	14.7	A
I_{DM}	Pulsed Drain Current[1]	200	A
P_D@T_C=25℃	Total Power Dissipation	62.5	W
P_D@T_A=25℃	Total Power Dissipation	5	W
E_{AS}	Single Pulse Avalanche Energy[4]	28.8	mJ
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	2.0	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	25	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	75	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=30A	-	-	7.5	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2	-	5	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=30A	-	55	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=60V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=30A	-	54	86	nC
Q_{gs}	Gate-Source Charge	V_{DS}=40V	-	14.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=10V	-	25	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=40V	-	16	-	ns
t_r	Rise Time	I_D=1A	-	14	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=10V	-	40	-	ns
t_f	Fall Time	R_D=40Ω	-	37	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	2350	3760	pF
C_{oss}	Output Capacitance	V_{DS}=25V	-	390	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	245	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1.3	-	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=30A, V_{GS}=0V	-	-	1.3	V
t_{rr}	Reverse Recovery Time[2]	I_S=10A, V_{GS}=0V,	-	46	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	86	-	nC

Notes:

1.Pulse width limited by Max. junction temperature

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec, 60°C/W at steady state.

4.Starting T_j=25°C , V_{DD}=30V , L=0.1mH , R_G=25Ω , I_{AS}=24A.

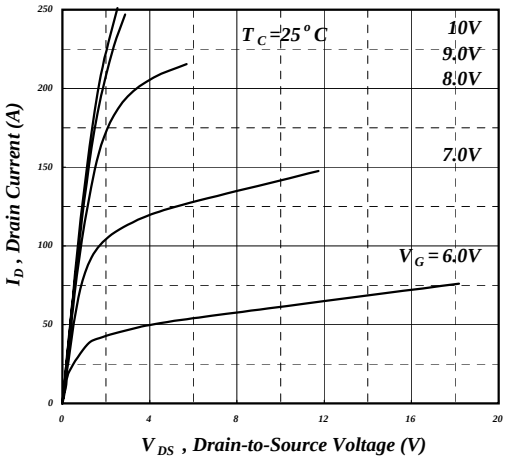


Fig 1. Typical Output Characteristics

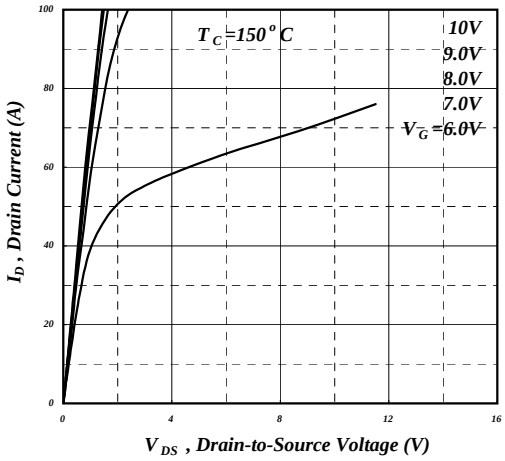


Fig 2. Typical Output Characteristics

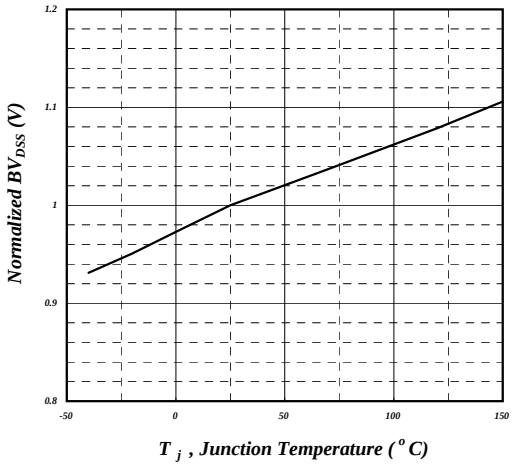


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

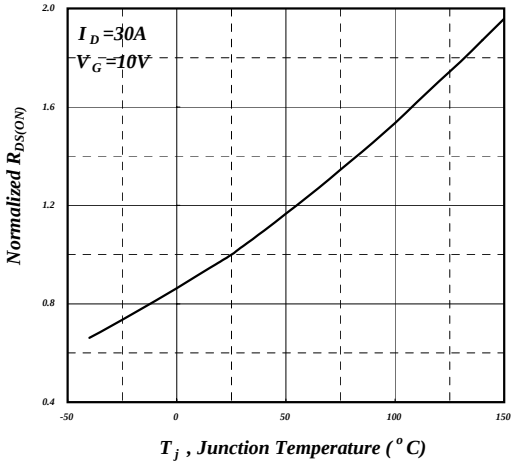


Fig 4. Normalized On-Resistance v.s. Junction Temperature

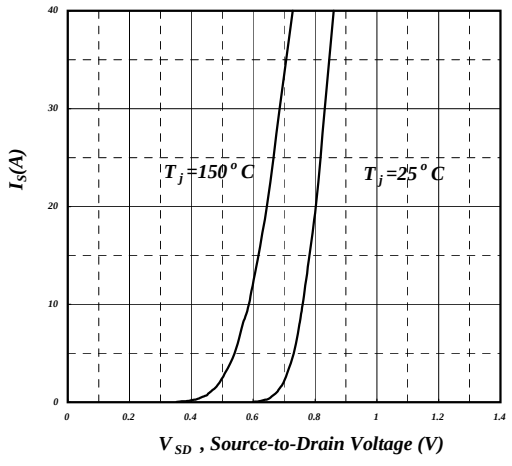


Fig 5. Forward Characteristic of Reverse Diode

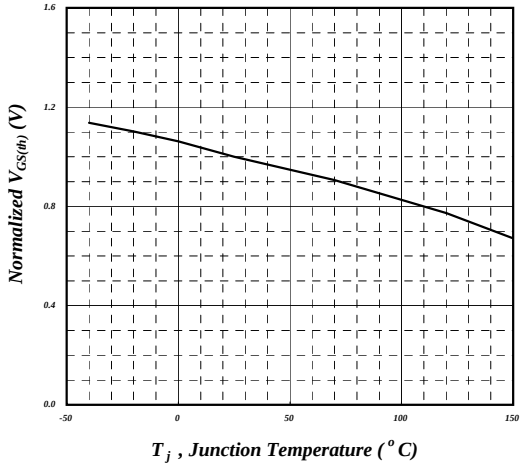


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

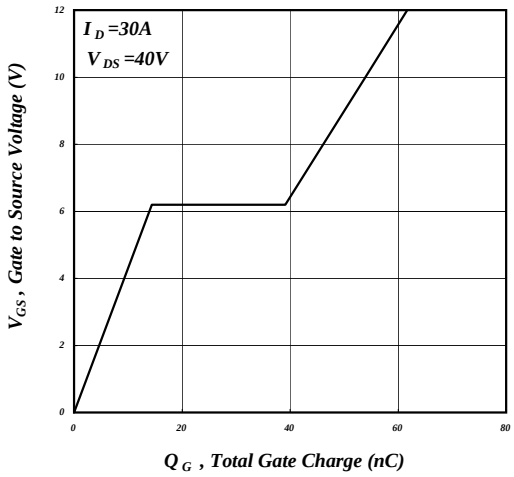


Fig 7. Gate Charge Characteristics

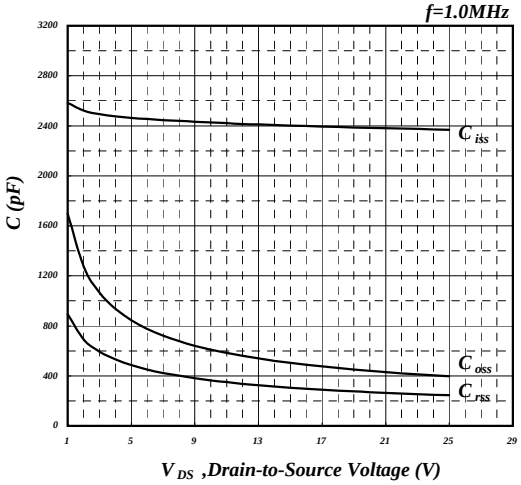


Fig 8. Typical Capacitance Characteristics

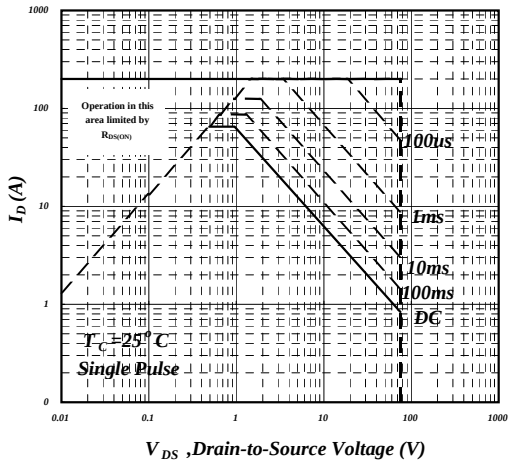


Fig 9. Maximum Safe Operating Area

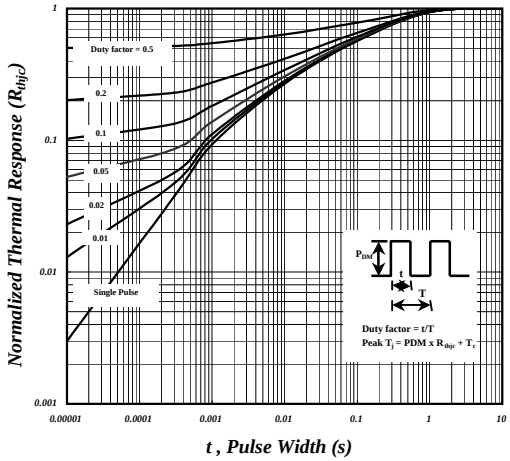


Fig 10. Effective Transient Thermal Impedance

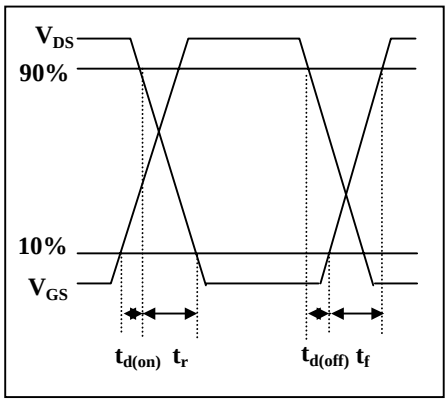


Fig 11. Switching Time Waveform

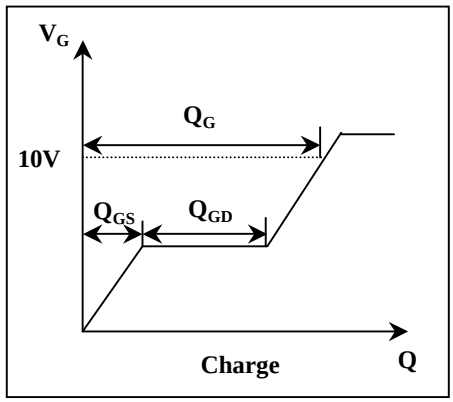


Fig 12. Gate Charge Waveform