

REC/PB Amplifier

Description

CX20034/CXA1234AR is a bipolar IC containing the peripheral functions of a VTR head on a single chip. It has following functions.

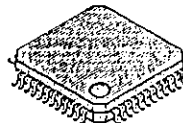
- Recording
 - REC AMP (2 channels)
 - Gain controlled amplifier for each of the 4 REC signal inputs (Y, Chroma, PCM, AFT (Automatic Track Finding)).
 - Signal MIX, switch.
- Playback
 - Low noise head amplifier (2 channels).
 - Playback signal output switch.
- Control/Logic
 - Logic control circuits of each mode.

Features

- Single power supply 5V
- Low power consumption (about 80 mW in REC mode, 85 mW in PB mode) power saving mode.
- Audio PCM (after recording is possible) and ATF are provided.

48pin QFP(Plastic)

48pin VQFP(Plastic)

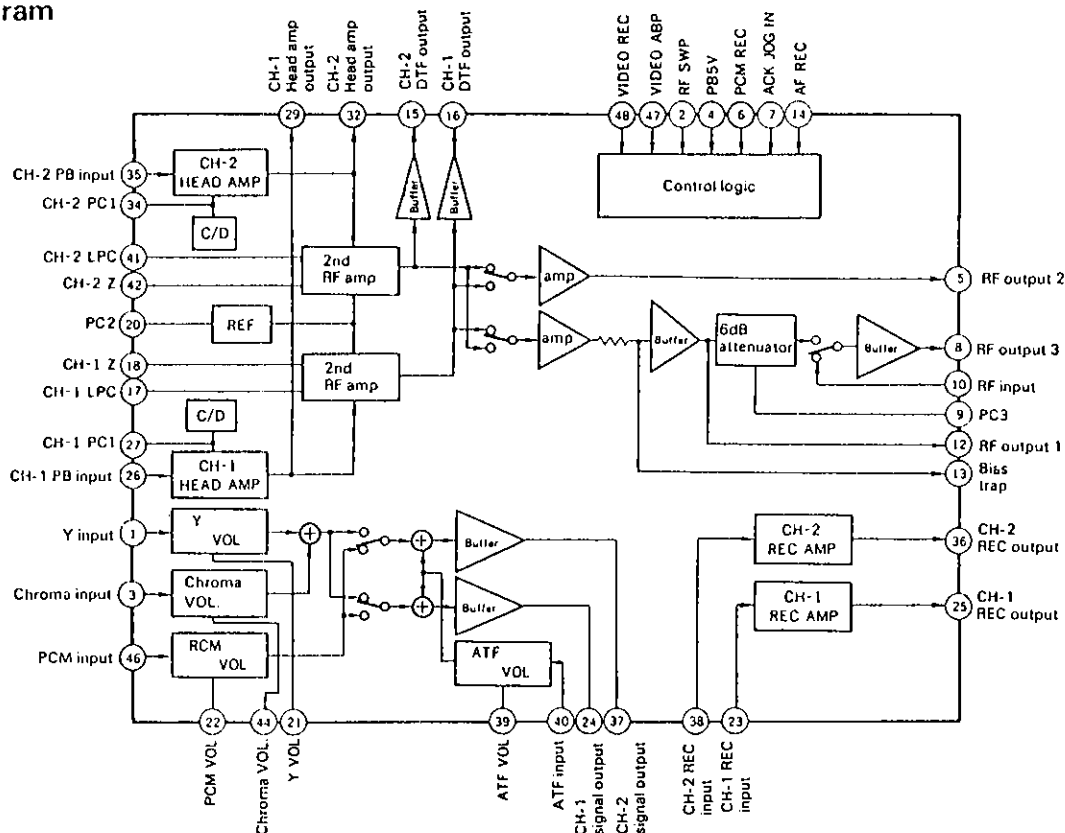


- DC REC signal (Y, Chroma, PCM and ATF) level control.
- Logic circuit is incorporated to control signal switching and save power in the REC, PB and after recording mode.

Structure

Bipolar silicon monolithic IC

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	10	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	Pd (CX20034)	920	mW
	Pd (CXA1234AR)	1100	mW

(CXA1232AR; Substrate surface 40 × 25 mm, t = 0.635 mm when ceramic substrate mounted.)

Recommended Operating Condition

• Supply voltage	Vcc	5.0 ± 0.25	V
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Pin Description

E. F; Emitter Follower

No.	Name	Voltage (Typ.) (V)	Input/Output resistance (Typ.)	Operation/Description
1	Y input	3.3V in REC	20k Ω	Input pin for recording Y signal.
2	RF SWP	— (Open; L)	40k Ω	Input pin of RF switching pulse to switch CH. H: over 3V L: under 1V
3	Chroma input	2.3V in REC	20k Ω	Input pin for recording chroma signal.
4	PB 5V	— (Open; L)	40k Ω	Logic control pin switching PB ON or OFF. H: over 3V. L: under 1V.
5	RF output 2	3.4V in PB	(E.F)	Output pin for playback PCM signal.
6	PCM REC	— (Open; L)	40k Ω	Logic control pin to record PCM. Priority over VIDEO REC. H; over 3V, L; under 1V.
7	ACK JOG IN	— (Open; L)	3k Ω +PN junction	Switching between VIDEO signal (L) and RF signal (H) for RF output 3 in PB mode. H; over 25 μ A, L; under 5 μ A.
8	RF output 3	3.4V in PB	(E.F)	Playback output pin to be controlled by ACK JOG IN.
9	PC3	2.5V in PB		Attenuator bypass capacitor pin.
10	RF input	2.5V in PB	20k Ω	VIDEO signal input pin.
11	PB Vcc	5V	—	Power supply pin for PB and control logic.
12	RF output 1	2.5V in PB	(E.F)	Playback Video output pin.
13	Bias trap	3.3V in PB	500 Ω	Pin to connect a filter in the fixed head audio mode. Open when not in use.
14	AF REC	— (Open; L)	40k Ω	Logic control pin to set in after recording mode. H; over 3V, L; under 1V.
15	CH-2 DTF output	2.5V in PB	(E.F)	CH-2 signal output pin when DTF is in use. Open when not in use.
16	CH-1 DTF output	2.5V in PB	(E.F)	CH-1 signal output pin when DTF is in use. Open when not in use.
17	CH-1 LPC	1.7V in PB		Bypass capacitor pin for 2nd RF AMP.
18	CH-1Z	About 3.9V in PB		Connect a resonance circuit to Vcc. About 1.5k Ω of DC resistance from Vcc is desirable.
19	PB GND	—	—	GND for PB and control logic.
20	PC2	2.5V in PB		Bypass capacitor pin.

No.	Name	Voltage (Typ.) (V)	Input/Output resistance (Typ.)	Operation/Description
21	Y VOL	—	$\geq 100k\Omega$	Gain control DC voltage (2 to 3V) application pin for recording Y signal. Not open allowable.
22	PCM VOL	—	$\geq 100k\Omega$	Gain control DC voltage (2 to 3V) application pin for recording chroma signal. Not open allowable.
23	CH-1 REC input	0.7V in REC	$\approx 0\Omega$	Input pin for CH-1 REC AMP
24	CH-1 signal output	3.3V in REC	(E.F)	CH-1 signal output pin for recording VOL + SW.
25	CH-1 REC output	—	(Open collector)	CH-1 REC AMP output pin.
26	CH-1 PB input	2.3V in PB	1.7k Ω	CH-1 HEAD AMP input pin.
27	CH-1 PC1	1.7V in PB		Bypass capacitor pin for CH-1 HEAD AMP. (About 0.2 μ)
28	HEAD AMP Vcc	5V	—	Power supply pin for HEAD AMP.
29	CH-1 HEAD AMP output	3.1V in PB	(E.F)	CH-1 HEAD AMP output.
30	HEAD AMP GND	—	—	GND for HEAD AMP.
31	REC AMP GND	—	—	GND for REC AMP.
32	CH-2 HEAD AMP output	3.1V in PB	(E.F)	CH-2 HEAD AMP output pin
33	REC AMP Vcc	—	—	Power supply pin for REC AMP.
34	CH-2 PC1	1.7V in PB	—	Bypass capacitor pin for CH-2 HEAD AMP.
35	CH-2 PB input	2.3V in PB	1.7k Ω	Input pin for CH-2 HEAD AMP.
36	CH-2 REC output	—	(Open collector)	Output pin for CH-2 REC AMP.
37	CH-2 signal output	3.3V in REC	(E.F)	CH-2 signal output pin for recording VOL + SW.
38	CH-2 REC input	0.7V in REC	$\approx 0\Omega$	Input pin for CH-2 REC AMP.
39	ATF VOL		$\geq 100k\Omega$	Gain control DC voltage (2 to 3V) supply pin for recording ATF signal. Not open allowable.
40	ATF IN	2.3V in REC	20k Ω	Input pin for recording ATF signal.

No.	Name	Voltage (Typ.) (V)	Input/Output resistance (Typ.)	Operation/Description
41	CH-2 LPC	1.7V in PB	—	Bypass capacitor pin for 2nd RF AMP.
42	CH-2 Z	About 3.9V in PB	—	Connect a resonance circuit to Vcc. About 1.5k Ω DC resistance from Vcc is desirable.
43	REC GND	—	—	GND for REC except REC AMP.
44	Chroma VOL		$\geq 100k\Omega$	Gain control DC voltage (2 to 3V) supply pin for recording chroma signal. Not open allowable.
45	REC Vcc	5V		Power supply pin for REC except for REC AMP.
46	PCM input	3.3V in REC	20k Ω	Input pin for recording PCM signal.
47	VIDEO ABP	— (Open; L)	40k Ω	Logic mode control pin to record overlap by activating REC AMP for both channels. H; over 3V, L; under 1V.
48	VIDEO REC	— (Open; L)	40k Ω	Logic control pin to record VIDEO signal. H; over 3V, L; under 1V.

Control Logic Truth Table

		(Input)						(Output)									
Control logic input		Control input condition						Operation of each section						Operation	Mode		
		AF REC ⑩	PB 5V ⑪	VIDEO REC ⑫	PCM REC ⑬	RF SWP ⑭	VIDEO ABP ⑮	VOLUME-SW	REC output		PB output						
Control logic condition																	
SW 1		X	L	L	L	X	X	○	X	X	X	X	X	REC PAUSE	REC		
SW 2		X	L	H	L	L	L	○	X	V	X	X	X	VIDEO REC			
SW 3		X	L	H	L	H	L	○	V	X	X	X	X				
SW 4		X	L	H	L	X	H	○	V	V	X	X	X	PCM REC			
SW 5		X	L	L	H	L	X	○	P	X	X	X	X				
SW 6		X	L	L	H	H	X	○	X	P	X	X	X	VIDEO PCM REC			
SW 7		X	L	H	H	L	X	○	P	V	X	X	X				
SW 8		X	L	H	H	H	X	○	V	P	X	X	X				
SW 9		L	H	L	L	L	X	X	X	X	○	CH ₋₂	CH ₋₁	PB	PB		
SW10		L	H	L	L	H	X	X	X	X	○	CH ₋₁	CH ₋₂				
SW11		H	H	L	L	L	X	○	X	X	○	CH ₋₂	CH ₋₁	PB in dubbing	Dubbing		
SW12		H	H	L	L	H	X	○	X	X	○	CH ₋₁	CH ₋₂	PCM REC in dubbing			
SW13		H	H	L	H	L	X	○	P	X	X	Z	△				
SW14		H	H	L	H	H	X	○	X	P	X	Z	△				
SW9-SW12		ACKJOGIN ⑩ --- H						RFOUT3 outputs signal from FRIN in each mode of SW9-12.									
		ACKJOGIN ⑩ --- L						RFOUT3 outputs signal with the same channel for RFOUT1 in each mode of SW9-12.									

Description of input condition

X Independent of H, L.

H Control logic input, over 3V.

L Control logic input, under 1V.

Only for ACKJOGIN

H Input current over 25μA.

L Input current under 5μA.

Description of operation mode

○ Operating

X Not operating. Power saving.

When VOLUME output is input to REC AMP (in REC mode)

V VIDEO signal is output.

P PCM signal is output.

In PB mode

CH-1 ... CH-1 signal is output.

CH-2 ... CH-2 signal is output.

Z DC level is held in place.

Δ Current flows but no normal output is obtained.

Electrical Characteristics *1 See the Control Logic Truth Table for control logic conditions. *2 See the Description of Circuit.
 $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$

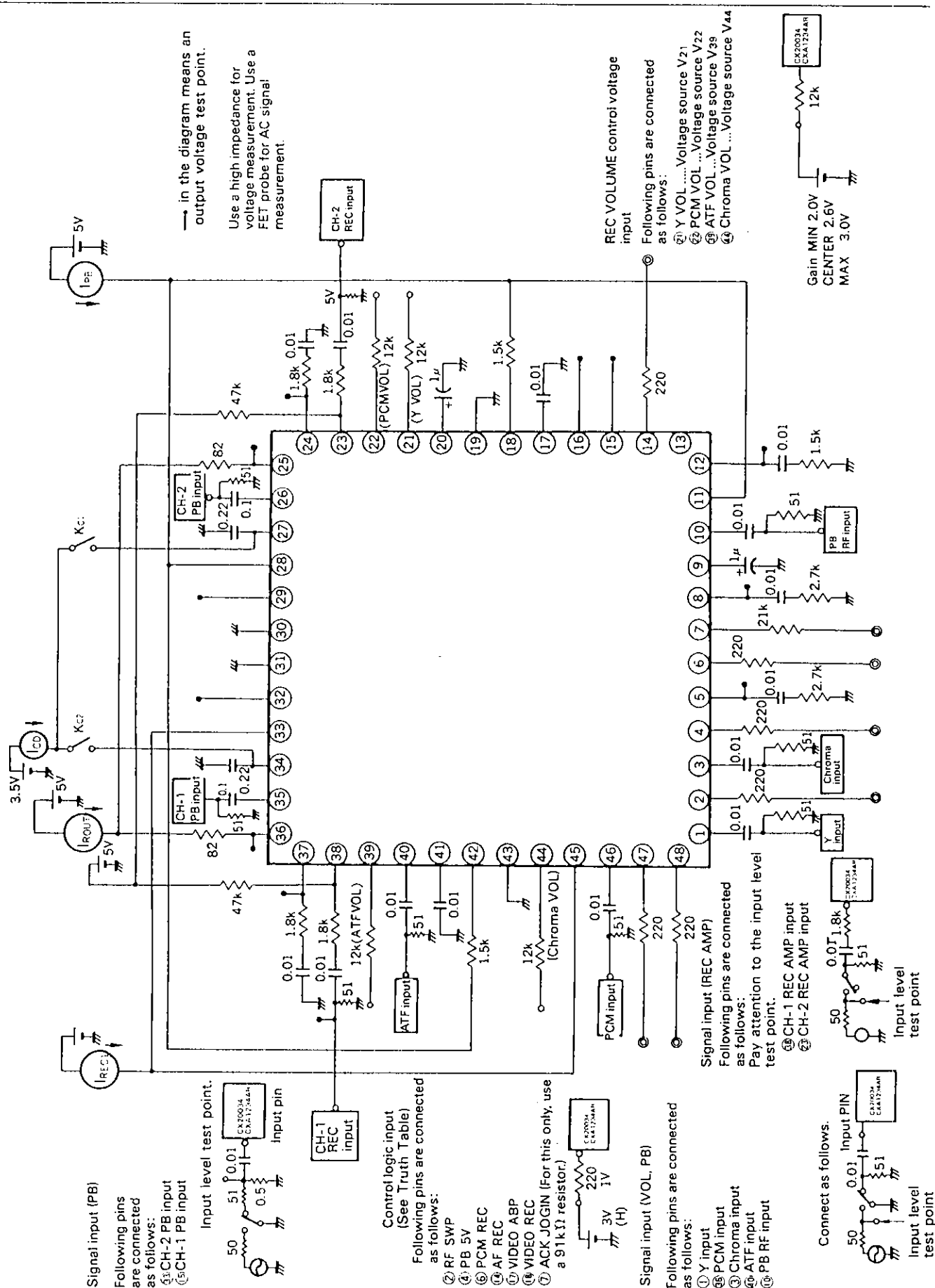
No.	Item	Symbol	Input condition *2 Input pin level · frequency	SW condition	Bias voltage				Output pin	Test content	Min.	Typ.	Max.	Unit
					*1 Control logic condition	Other SW ON	V ₂₁ Y vol	V ₂₂ PCH vol	V ₄₄ Chroma vol	V ₃₉ ATF vol				
1	REC mode total current (in both CH REC)	I _{REC}		SW4			2.6V	2.6V	2.6V	2.6V	13.5	17.0	21.5	mA
2	PB mode total current	I _{PB}		SW9			↓	↓	↓	↓	14.0	17.5	22.5	mA
3	REC output bias current (CH1) (CH2)	I _{OUT1}		SW3			↓	↓	↓	↓	12.0	14.0	16.0	mA
		I _{OUT2}		SW2			↓	↓	↓	↓				
4	PC1 CHARGE current (CH1) (CH2)	I _{CC1}		SW5	Kc1		↓	↓	↓	↓	-29.0	-22.0	-14.0	mA
		I _{CC2}		SW6	Kc2		↓	↓	↓	↓				
5	PC1 DISCHARGE current (CH1) (CH2)	I _{DC1}		SW10	Kc1		↓	↓	↓	↓	28.0	34.0	40.0	mA
		I _{DC2}		SW9	Kc2		↓	↓	↓	↓				
6	RF output 1 DC voltage difference in switching inputs (CH-1, CH-2)	ΔV _{V12}		SW11 — SW12			↓	↓	↓	↓			40	mA
7	RF output 2 DC voltage difference in switching PB output in place (Setting CH-1, CH-2)	ΔV _{VW}		SW11-SW13 SW12-SW13			↓	↓	↓	↓			90	mV
8	RF output 2 DC voltage difference in switching inputs (CH1 — CH2)	ΔV _{P12}		SW11 — SW12			↓	↓	↓	↓			30	mV
<AC in REC system>														
9	Y VOL output level (MIN) (CH2)	Y _{1MIN}	1; — 2dBm	SW3			2.0V	2.6V	2.6V	2.6V	24			
		Y _{2MIN}	↓	SW2			↓	↓	↓	↓	37			
10	Y VOL output level (TYP) (CH2)	Y _{1TYP}	↓	SW3			2.6V	↓	↓	↓	24			
		Y _{2TYP}	↓	SW2			↓	↓	↓	↓	37			

No.	Item	Symbol	Input condition * 2 Input pin level · frequency	SW condition	Bias voltage					Output pin	Test content	Min.	Typ.	Max.	Unit	
				* 1Control logic condition	Other SW ON	V21 Y vol	V22 PCH vol	V44 Chroma vol	V39 ATF vol	Ammeter name						
11	Y VOL output level (MAX)	Y1MAX (CH1)	1; - 2dBm 1MHz	SW3		3.0V	2.6V	2.6V	2.6V	24	Output level in Y VOL GAIN MAX (Standard input level, 1 MHz)	-4.5	- 1.8	+1.0	dBm	
		Y2MAX (CH2)	1; 1	SW2		1	1	1	1	37						
12	Y VOL frequency response (TYP)	ΔY1TYP (CH1)	1; 1MHz	SW3		2.6V	1	1	1	24	Output level drops during 1 - 10 MHz in Y VOL GAIN TYP			1.0	dB	
		ΔY2TYP (CH2)	1; 10MHz	SW2		1	1	1	1	37						
13	Y VOL 2nd harmonic (TYP)	DY1 (CH1)	1; 4MHz	SW3		1	1	1	1	24	2nd harmonic in Y VOL GAIN TYP (Standard input level, 4MHz)			-44	dB	
		DY2 (CH2)	1; 4MHz	SW2		1	1	1	1	37						
14	PCM VOL output level (MIN)	P2MIN (CH2)	46; - 2dBm 1MHz	SW6		1	2.0V	1	1	37	Output level in PCM VOL GAIN MIN (Standard input level, 1MHz)	- 17.5	- 16.3	- 15.5	dBm	
15	PCM VOL output level (TYP)	P2TYP (CH2)	1; 1	SW6		1	2.6V	1	1	37	Output level in PCM VOL GAIN TYP (Standard input level, 1MHz)	- 11.5	- 10.5	- 9.5	dBm	
16	PCM VOL output level (MAX)	P2MAX (CH2)	1; 1	SW6		1	3.0V	1	1	37	Output level in PCM VOL GAIN MAX (Standard input level, 1MHz)	- 4.5	- 1.8	+1.0	dBm	
17	PCM VOL frequency response (TYP)	ΔP1TYP (CH1)	1; 1MHz, 10MHz,	SW5		1	2.6V	1	1	24	Output level drops during 1 to 10MHz in PCM VOL GAIN TYP.			1.0	dB	
		ΔP2TYP (CH2)	1; 1MHz, 10MHz,	SW6		1	1	1	1	37						
18	PCM VOL 2nd harmonic (TYP)	DP1 (CH1)	1; 4MHz	SW5		1	1	1	1	24	2nd harmonic in PCM VOL GAIN TYP. (Standard input level, 4MHz).			-42	dB	
		DP2 (CH2)	1; 4MHz	SW6		1	1	1	1	37						
19	Chroma VOL output level (MIN)	C2MIN (CH2)	3; -12 dBm, 750 kHz	SW2		1	1	2.0V	1	37	Output level in chroma VOL GAIN MIN (Standard input level, 750kHz)	-29.7	-28.9	-28.2	dBm	
20	Chroma VOL output level (TYP)	C1TYP (CH1)	1; 1	SW3		1	1	2.6V	1	24	Output level in chroma VOL GAIN TYP (Standard input level, 750kHz)	-24.6	-23.8	-23.0	dBm	
21	Chroma VOL output level (MAX)	C2MAX (CH2)	1; 1	SW2		1	1	3.0V	1	37	Output level in chroma VOL GAIN MAX (Standard input level, 750kHz)	-19.0	-17.5	-15.8	dBm	
22	Chroma VOL 2nd harmonic (TYP)	DC1 (CH1)	1; 1	SW3		1	1	2.6V	1	24	2nd harmonic of chroma VOL GAIN TYP. (Standard input level, 750kHz).			-44	dB	
		DC2 (CH2)	1; 1	SW2		1	1	2.6V	1	37						
23	ATF VOL output level (MIN)	A1MIN (CH1)	40; -2 dBm, 100 kHz	SW3		1	1	1	2.0V	24	Output level in ATF VOL GAIN MIN (Standard input level, 100kHz)	-44.0	-43.2	-42.0	dBm	
		A2MIN (CH2)	1; 1	SW2		1	1	1	1	37						

No.	Item	Symbol	Input condition *2 Input pin level · frequency	SW condition	Bias voltage				Output pin	Test content	Min.	Typ.	Max.	Unit
					Control logic condition	Other SW ON	V21 Y vol	V22 PCH vol	V44 Chroma vol	V39 ATF vol				
24	ATF VOL output level (MIN)	A1MAX	40; -2dBm 100kHz	SW3			2.6V	2.6V	2.6V	3.0V	24			
		A2MAX	↓; ↓	SW2			↓	↓	↓	↓	37			
25	ATF VOL 2nd harmonic (MAX)	DA1	↓; ↓	SW3			↓	↓	↓	↓	24			
		DA2	↓; ↓	SW2			↓	↓	↓	↓	37			
26	REC AMP output level	R1	23; -10 dBm 1MHz	SW3			↓	↓	↓	2.6V	25			
		R2	38; ↓	SW2			↓	↓	↓	↓	36			
27	REC AMP frequency response	ΔR1	23; ↓ 1MHz 10MHz	SW3			↓	↓	↓	↓	25			
		ΔR2	38; ↓ 1MHz 10MHz	SW3			↓	↓	↓	↓	36			
28	REC AMP (CH1)	DR1	23; ↓ 4MHz	SW3			↓	↓	↓	↓	25			
	(CH2)	DR2	38; ↓	SW2			↓	↓	↓	↓	36		-48	-38
29	REC AMP channel balance	ΔR12	23; ↓ 1MHz	SW3			↓	↓	↓	↓	25			
	38; ↓		SW2			↓	↓	↓	↓	↓	36			
< AC in PB system >														
30	RF output 1 output level	PB12	35; -69.5 dBm 1MHz	SW9			2.6V	2.6V	2.6V	2.6V	12			
31	RF output 2 output level	PB21	26; ↓	SW9			↓	↓	↓	↓	5			
	(CH2)	PB22	35; ↓	SW10			↓	↓	↓	↓	5			

No.	Item	Symbol	Input condition *2 Input pin level · frequency	SW condition	Bias voltage				Output pin	Test content	Min.	Typ.	Max.	Unit
					*1Control logic condition	Other SW ON	V21 Y vol	V22 PCH vol	V44 Chroma vol	V39 ATF vol	Ammeter name			
32	RF output 2 frequency response	ΔP_{B21} (CH1) ΔP_{B22} (CH2)	26; -69.5dBm 1MHz 35; ↓	SW9		2.6V	2.6V	2.6V	2.6V	5	Output level drops during 1 to 10MHz in RF output 2 output.		2.7	dB
33	RF output 3 output level	P_{B31} (CH1) ΔP_{B32} (CH2)	26; ↓ 35; ↓	SW10 7pin-L SW9 7pin-L		↓	↓	↓	↓	8	RF output 3 output level (-69.5dBm input, 1MHz)	-14.5 - 12.0 - 10.5	dBm	
34	RF output 3 frequency response	ΔP_{B31} (CH1) ΔP_{B32} (CH2)	26; ↓ 35; ↓	SW10 7pin-L SW9 7pin-L		↓	↓	↓	↓	8	Output level drops during 1 to 10MHz in RF output 3 output.		3.2	dB
35	RF output 3 output level of RFIN input	P_{B3AJ}	10; -12 dBm	SW10 7pin-H		↓	↓	↓	↓	8	1MHz output level in RFIN — RF output 3 modes.	-12.9 - 12.1	-11.6	dBm
36	RF output 3 output frequency response of RFIN input	ΔP_{B3AJ}	10; ↓ 1MHz, 10MHz	SW10 7pin-H		↓	↓	↓	↓	8	Output level drops during 1 to 10MHz in RFIN — RF output 3 modes.		22	dB

Electrical Characteristics Test Circuit



Description of Operations

The CX20034/CXA1234AR has following functional blocks.

1. REC, VOL + SW section.
2. REC AMP section.
3. PB HEAD AMP section.
4. PB 2nd RF AMP + SW section.
5. CONTROL LOGIC section.

The CX20034/CXA1234AR has 4 power supply and GND pairs for above systems, 1, 2, 3, and 4, 5 (common). The following is a description for each block.

<REC VOL + SW>

Here, each of the Y, Chroma, PCM and ATF signals are input and the VIDEO + ATF and PCM + ATF signals are generated with the level matched in the head to the correct current and they are output with the correct timing to the CH-1 and CH-2 signal output pins.

In the VOL section, the DC voltage (0.4VCC to 0.6VCC, Open not allowable) is applied to each VOL terminal and controls the gain of the 4 inputs independently. In SW, the signal is output to the CH-1 and CH-2 signal output pins in the REC and after recording modes under control of the control logic section.

<REC AMP>

The REC VOL + SW output is input after it is converted into a suitable current by an external resistor, to drive the head. Adjustment of the external resistor makes it possible to set a gain and DC bias current to match that of the head. (Refer to the Example of Application Circuit).

Take care that capacitance coupling will not occur across the input and output.

<PB HEAD AMP>

The playback signal from the head is amplified with low-noise and high gain. For example, the equivalent input noise level at 1MHz is $696\text{pV}/\sqrt{\text{Hz}}$ (Typ). The C/D (Charge/Discharge) circuit is a circuit used to rapidly charge or discharge the head amp bypass condenser.

In switching from PB to REC, it serves to shorten the switching time by rapidly injection current to the bypass condenser for PC1 PIN, and intake current in switching from REC to PB. The switching time is determined by bypass condenser for PC1 and LPC. Selection of values $0.22\mu\text{F}$ for the PC1 and $0.01\mu\text{F}$ for LPC, makes it possible to switch within 1 H ($\approx 64\mu\text{s}$).

In PB, the total input capacitance will be about 82pF. (Fig.3 example of Application Circuit). However, this capacitance will increase when there is a capacitance coupling across the head input and output. Be careful about the relations between the later stages (RF outputs 1, 2, 3 etc.) and input or between the other channel outputs and inputs.

- Connect a bypass condenser for CH-1 PC1 and CH-2 PC1 between them and the rotary transformer Vcc.

<PB 2nd RF AMP + SW>

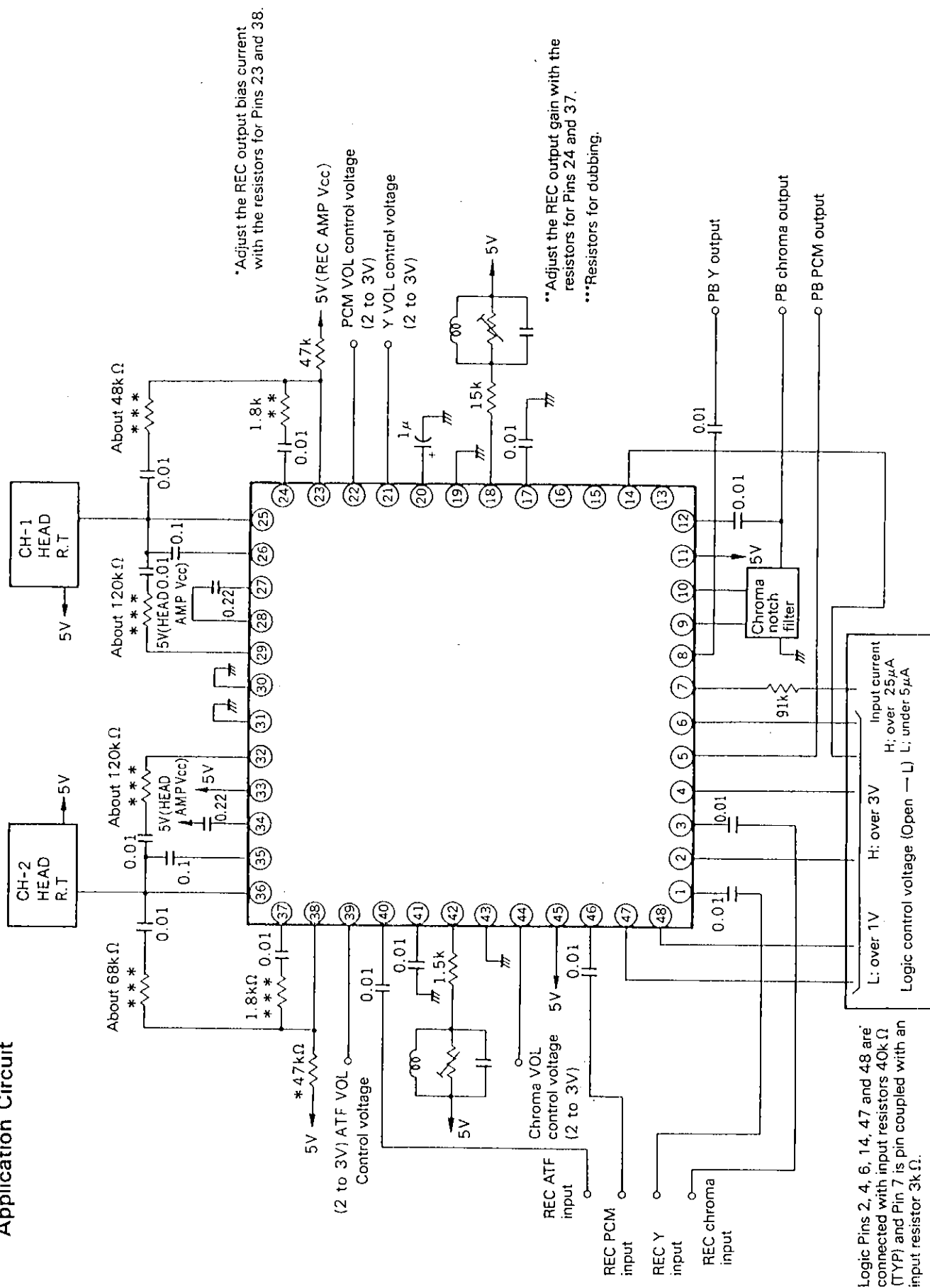
The playback signal from the head amp is further amplified here and the playback signal is output with the correct timing to the RF outputs 1, 2 and 3 under the control logic section.

<CONTROL LOGIC>

The IC is controlled from this section so it will save power when circuit blocks are not in use. Therefore, power saving is automatically executed when all the power supplies are switched on. Many SWs are also available to switch inputs or outputs with complicated timings; internal logic circuits to control them are provided.

With the 14 modes shown in the control logic condition table, all input and output combinations required for basic operations are satisfied. L is set when the control logic pin is open.

Application Circuit

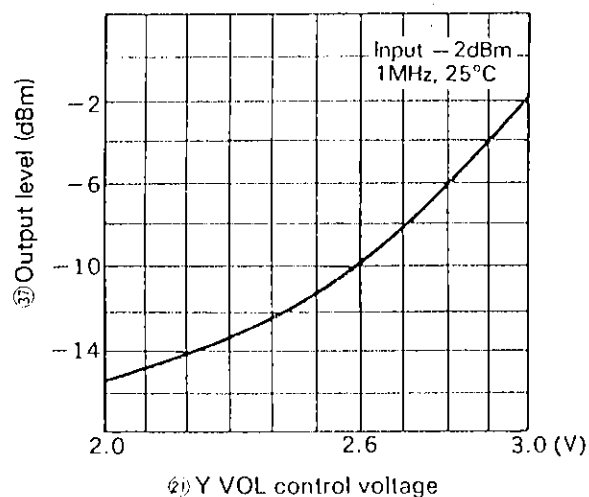


Y VOL + SW Typical Performance Curves

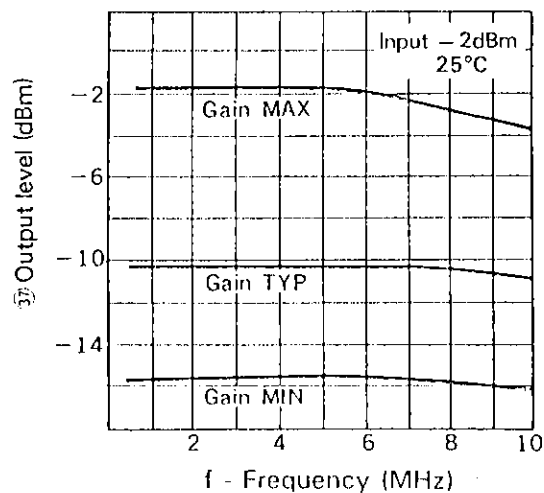
(Pin ①) input → Pin ③ output,
with Pin 21 controlling gain.

Control voltage 2.0V → Minimum gain.
2.6V → Typical gain.
3.0V → Maximum gain.

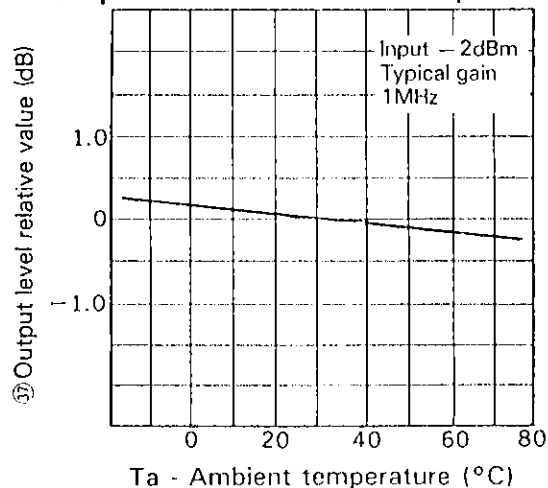
Output level vs. Y VOL control voltage



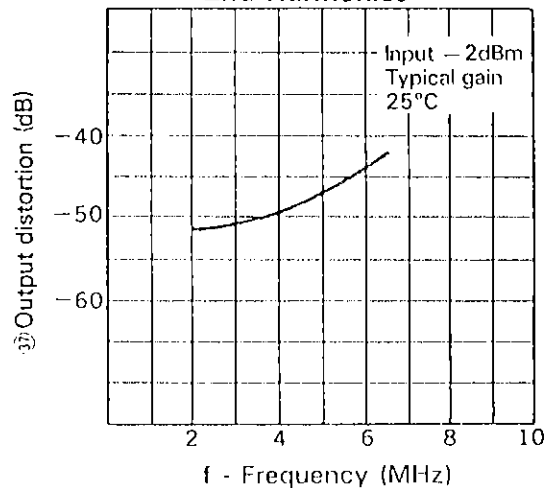
Output level vs. Frequency



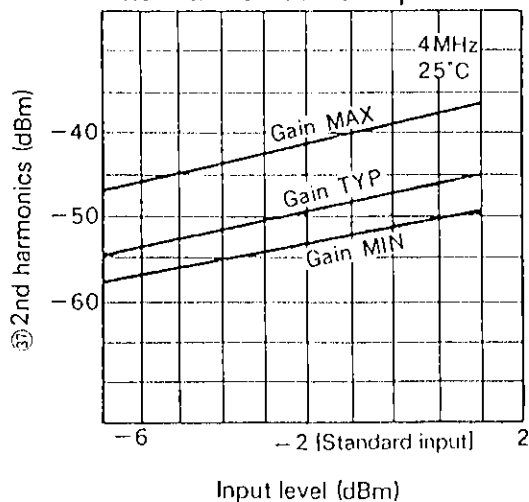
Output level vs. Ambient temperature



2nd Harmonics



2nd Harmonics vs. Input level



Chroma VOL + SW Typical Performance Curves

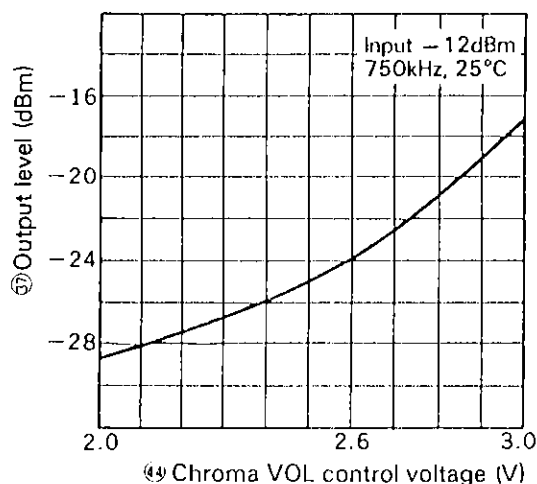
(Pin ③ input → Pin ⑦ output,
with Pin 44 controlling gain.

Control voltage 2.0V → Minimum gain.

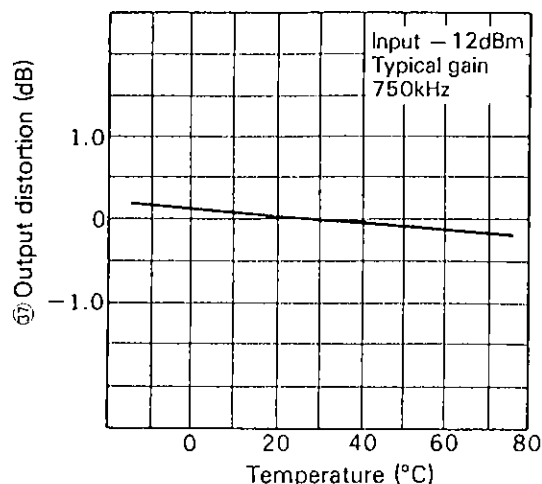
2.6V → Typical gain.

3.0V → Maximum gain.

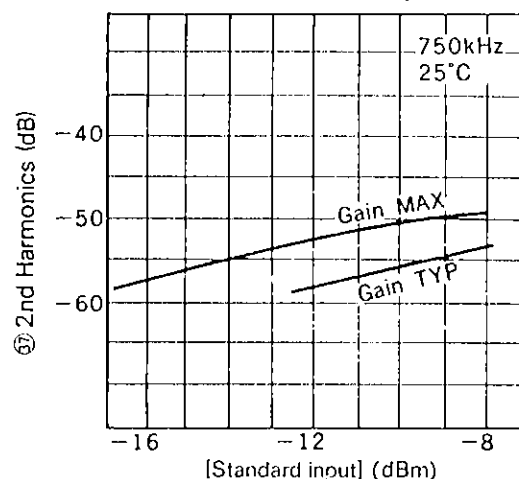
Output level vs. Chroma VOL control voltage



Output level vs. Temperature



2nd Harmonics vs. Input level



PCM VOL + SW Typical Performance Curves

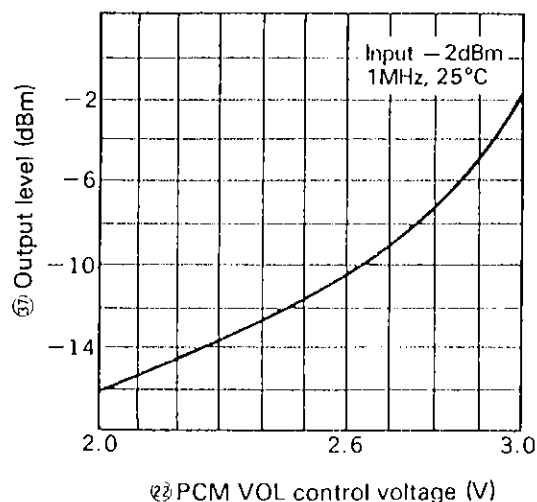
(Pin 46 input → Pin 37 output,
with Pin 22 controlling gain.

Control voltage 2.0V → Minimum gain.

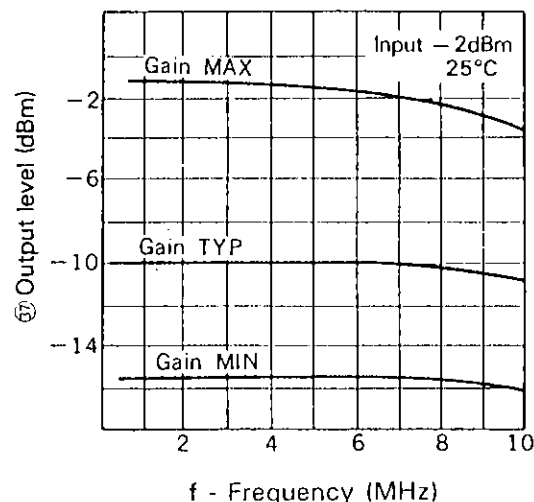
2.6V → Typical gain.

3.0V → Maximum gain.

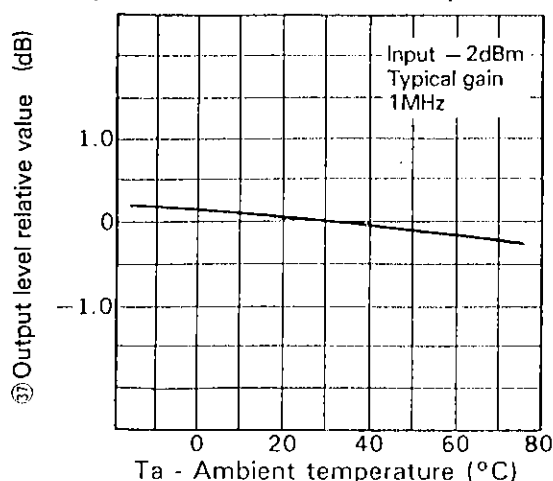
Output level vs. PCM VOL control voltage



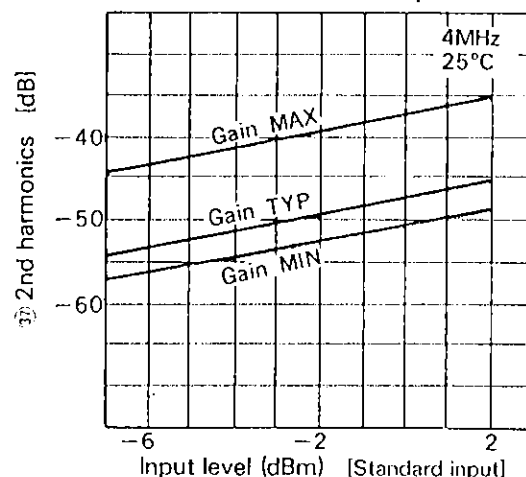
Output level vs. Frequency



Output level vs. Ambient temperature



2nd Harmonics vs. Input level

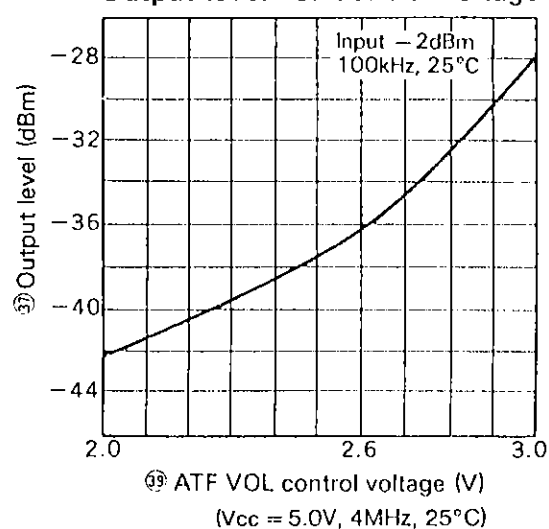


ATF VOL + SW Typical Performance Curves

(Pin 40 input → Pin 37 output,
with Pin 39 controlling gain.)

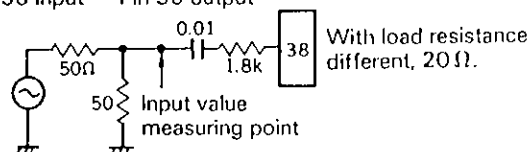
Control voltage 2.0V → Minimum gain.
2.6V → Typical gain.
3.0V → Maximum gain.

Output level vs. Control voltage

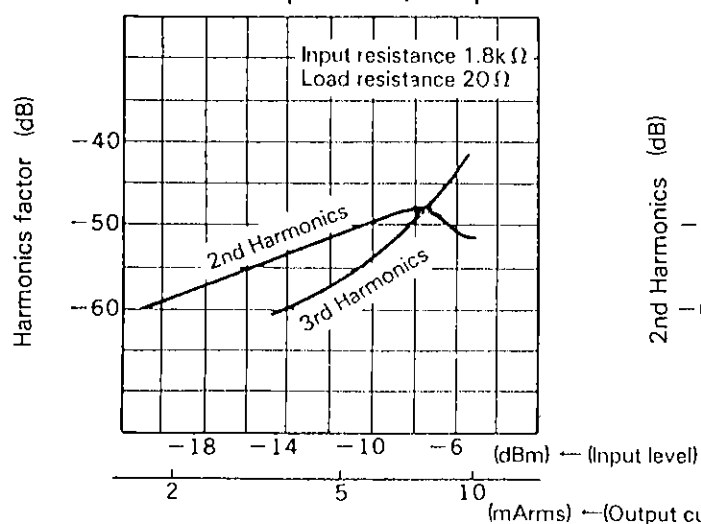


REC AMP Reference Characteristics

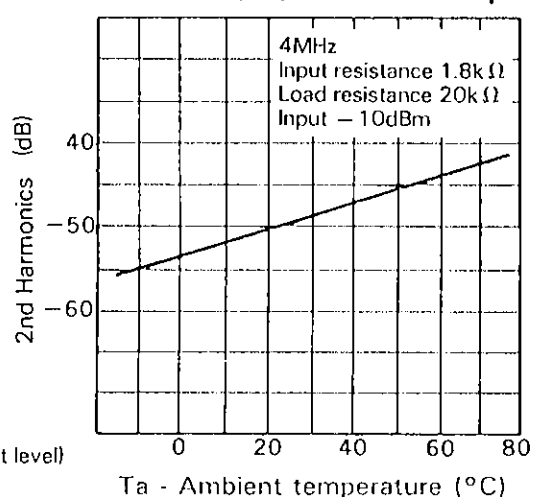
Pin 38 input → Pin 36 output



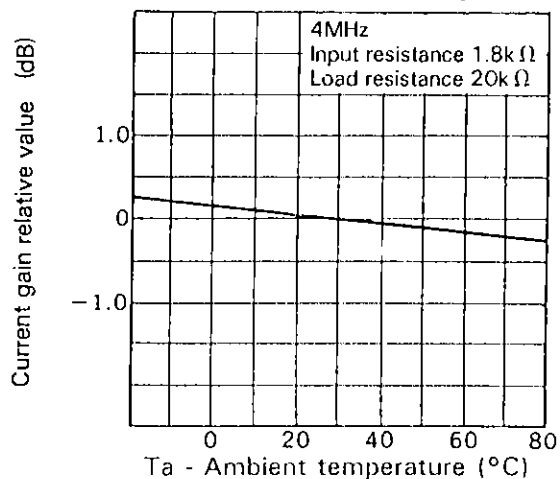
Distortion factor vs. Input level, Output current



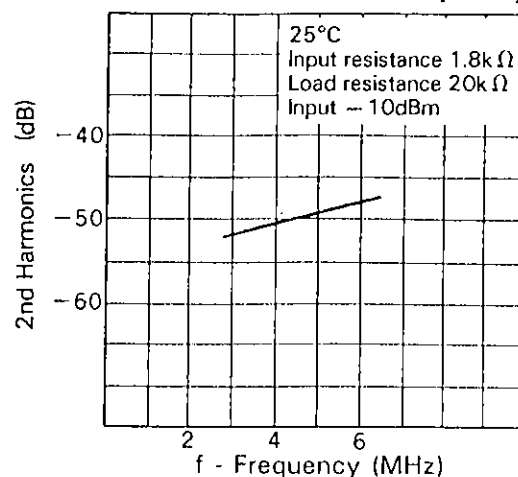
2nd Harmonics vs. Ambient temperature



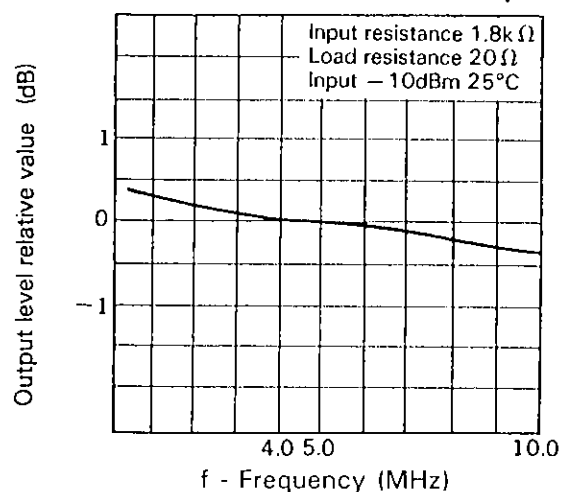
Current gain vs. Ambient temperature



2nd Harmonics vs. Frequency



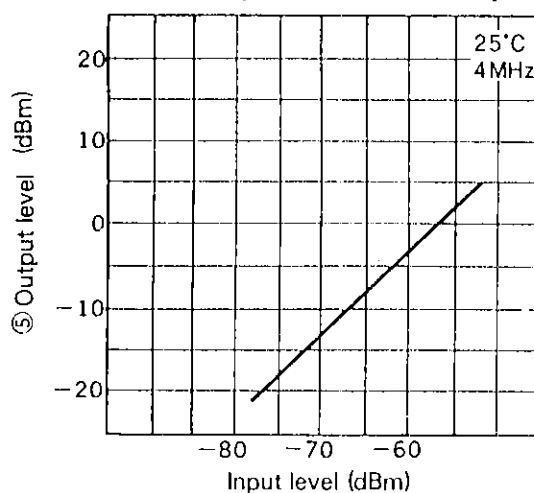
Output level relative value vs. Frequency



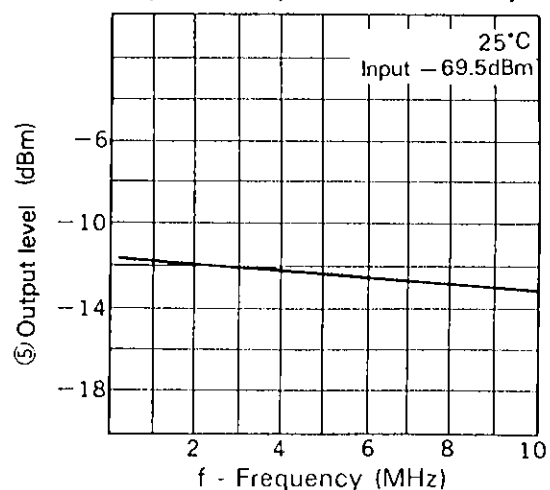
PB Typical Performance Curves

With $V_{CC} = 5.0\text{V}$ in the Electrical Characteristics measuring Circuit, Pin 35 input $\rightarrow$ Pin 5 output.

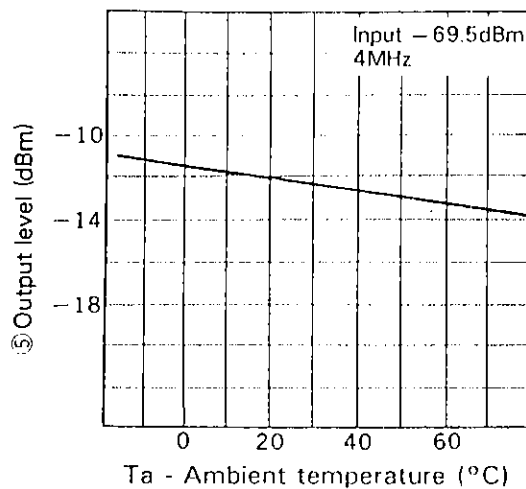
RF output 2 output level vs. PB input level



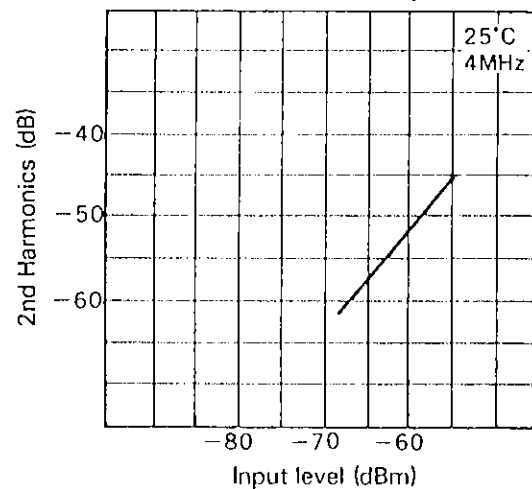
RF output 2 output level vs. Frequency



RF output 2 output level vs. Ambient temperature

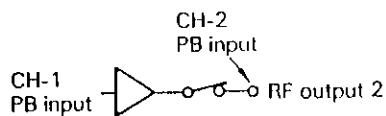
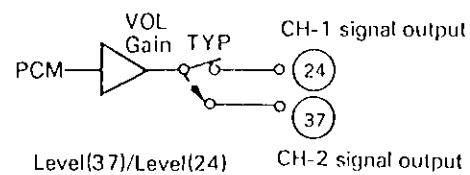
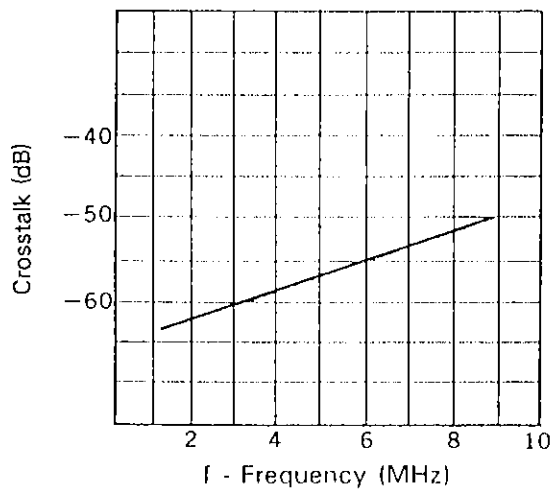


2nd Harmonics vs. Input level

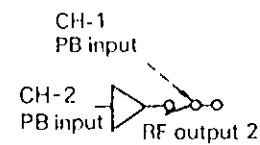
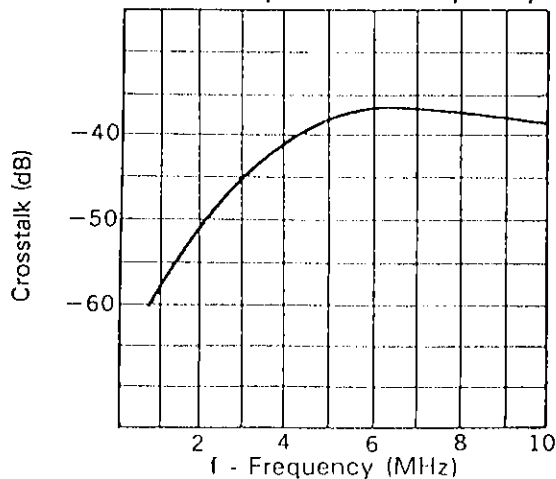


Crosstalk Typical Performance Curves

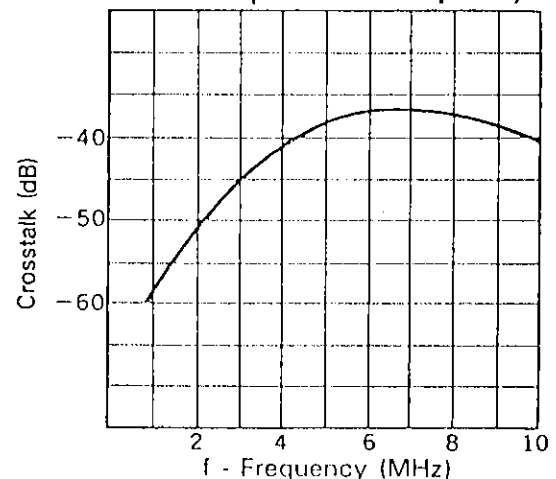
REC PCM VOL + SW crosstalk vs. Frequency



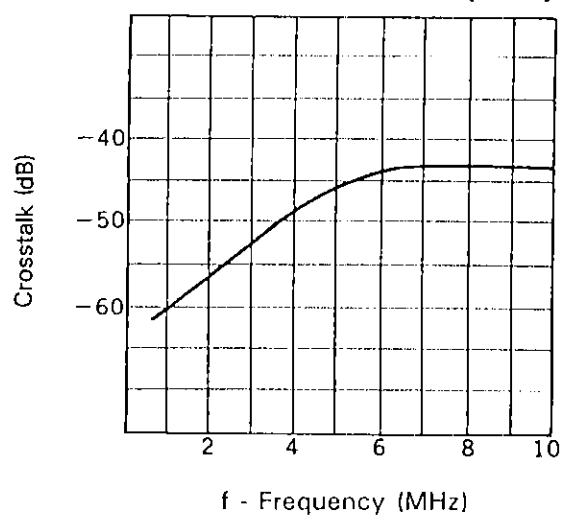
CH-2 → CH-1 crosstalk with PB RF output 2 vs. Frequency



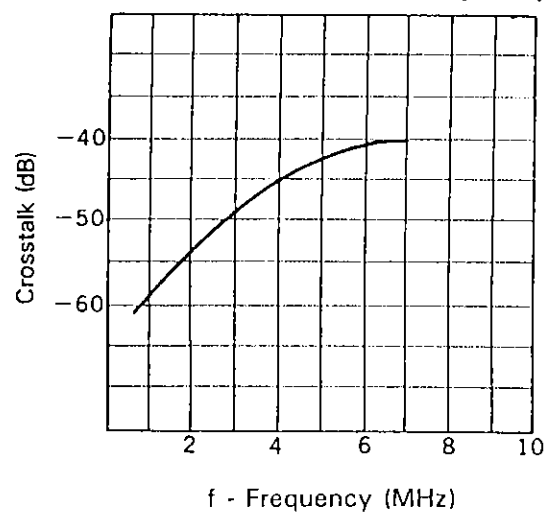
CH-1 → CH-2 crosstalk with PB RF output 2 vs. Frequency



CH-2 → CH-1 crosstalk with
PB RF OUTPUT 3 vs. Frequency

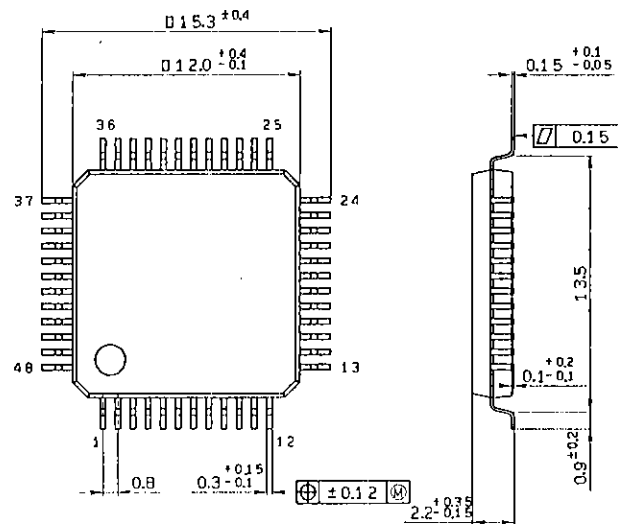


CH-1 → CH-2 crosstalk with
PB RF OUTPUT 3 vs. Frequency



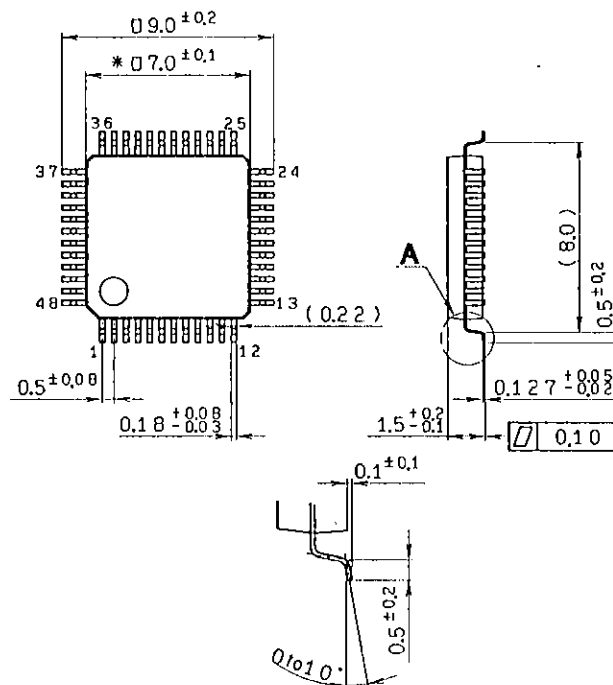
Package Outline Unit : mm

CX20034 48pin QFP(Plastic) 0.6g



QFP-48P-L04

CXA1234AR 48pin VQFP(Plastic) 0.2g



VQFP-48P-L01