Analog Front-End for Power Monitoring, Control, and Protection

Check for Samples: ADS131E04, ADS131E06 , ADS131E08

FEATURES

- **Eight Differential Current and Voltage Inputs**
- **Outstanding Performance:**
  - **Exceeds Class 0.1 Performance**
  - **Dynamic Range at 1 kSPS: 118 dB**
  - **Crosstalk: –110 dB**
  - **THD: –90 dB at 50 Hz and 60 Hz**
- **Supply Range:**
  - **Analog:**
    - **+3 V to +5 V (Unipolar)**
    - **±2.5 V (Bipolar, allows dc coupling)**
  - **Digital: +1.8 V to +3.6 V**
- **Low Power: 2 mW per Channel**
- **Data Rates: 1, 2, 4, 8, 16, 32, and 64 kSPS**
- **Programmable Gains (1, 2, 4, 8, and 12)**
- **Fault Detection and Device Testing Capability**
- **SPI™ Data Interface and Four GPIOs**
- **Package: TQFP-64 (PAG)**
- **Operating Temperature Range: –40°C to +105°C**

APPLICATIONS

- **Industrial Power Applications:**
  - **Energy Metering**
  - **Monitoring, Control, and Protection**

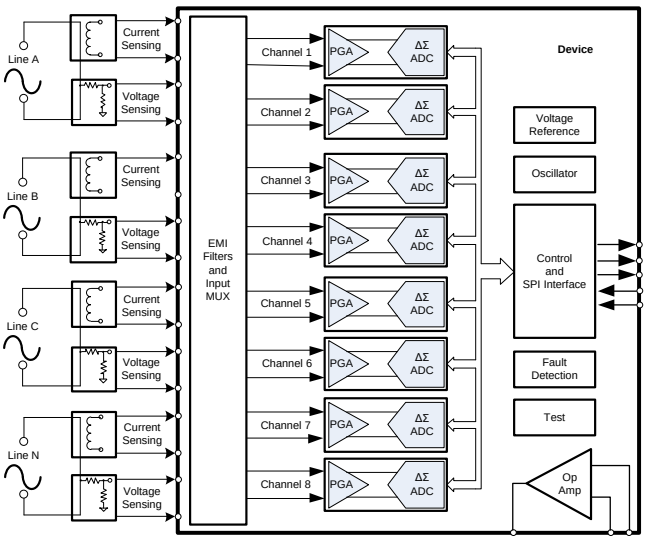
DESCRIPTION

The ADS131E0x are a family of multichannel, simultaneous sampling, 24- and 16-bit, delta-sigma (ΔΣ), analog-to-digital converters (ADCs) with a built-in programmable gain amplifier (PGA), internal reference, and an onboard oscillator.

The ADS131E0x incorporate features commonly required in industrial power monitoring, control, and protection applications. The ADS131E0x inputs can be independently and directly interfaced with a resistor-divider network or a transformer to measure voltage. The inputs can also be interfaced to a current transformer or Rogowski coil to measure current. With high integration levels and exceptional performance, the ADS131E0x family enables the creation of scalable industrial power systems at significantly reduced size, power, and low overall cost.

The ADS131E0x have a flexible input multiplexer per channel that can be independently connected to the internally-generated signals for test, temperature, and fault detection. Fault detection can be implemented internal to the device, using the integrated comparators with digital-to-analog converter (DAC)-controlled trigger levels. The ADS131E0x can operate at data rates as high as 64 kSPS.

These complete analog front-end (AFE) solutions are packaged in a TQFP-64 package and are specified over the industrial temperature range of –40°C to +105°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FAMILY AND ORDERING INFORMATION(1)

PRODUCT	PACKAGE OPTION	NUMBER OF CHANNELS	ACCURACY	MAXIMUM SAMPLE RATE (kSPS)	OPERATING TEMPERATURE RANGE
ADS130E08	TQFP-64	8	Class 1.0	8	–40°C to +105°C
ADS131E04	TQFP-64	4	Class 0.1	64	–40°C to +105°C
ADS131E06	TQFP-64	6	Class 0.1	64	–40°C to +105°C
ADS131E08	TQFP-64	8	Class 0.1	64	–40°C to +105°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
AVDD to AVSS		–0.3 to +5.5	V
DVDD to DGND		–0.3 to +3.9	V
AGND to DGND		–0.3 to +0.3	V
Analog input to AVSS		AVSS – 0.3 to AVDD + 0.3	V
Digital input to DVDD		DVSS – 0.3 to DVDD + 0.3	V
Input current to any pin except supply pins(2)		±10	mA
Input current	Momentary	±100	mA
	Continuous	±10	mA
Temperature	Operating, industrial-grade devices only	–40 to +85	°C
	Storage	–60 to +150	°C
	Maximum junction, T_J	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±1000	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing beyond the supply rails must be current limited to 10 mA or less.

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ELECTRICAL CHARACTERISTICS

Minimum and maximum specifications apply from –40°C to +105°C. Typical specifications are at +25°C. All specifications are at DVDD = 1.8 V, AVDD = 3 V, AVSS = 0 V, V_{REF} = 2.4 V, external f_{CLK} = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS131E0x MIN	ADS131E0x TYP	ADS131E0x MAX	UNIT
ANALOG INPUTS						
	Full-scale differential input voltage (AINP – AINN)			±V_{REF} / gain		V
	Input common-mode range			See the *Input Common-Mode Range* subsection of the *PGA Settings and Input Range* section		
C_i	Input capacitance			20		pF
I_{IB}	Input bias current	PGA output in normal range		5		nA
	DC input impedance			200		MΩ
PGA PERFORMANCE						
	Gain settings			1, 2, 4, 8, 12		
BW	Bandwidth			See Table 3		
ADC PERFORMANCE						
	Resolution	Data rates up to 16 kSPS	24			Bits
		32- and 64-kSPS data rate	16			Bits
DR	Data rate	f_{CLK} = 2.048 MHz	1		64	kSPS
CHANNEL PERFORMANCE (DC Performance)						
INL	Integral nonlinearity	Full-scale, best fit		10		ppm
	Dynamic range	G = 1	105			dB
		Gain settings other than 1		See *Noise Measurements* section		
E_O	Offset error			350		µV
	Offset error drift			0.65		µV/°C
E_G	Gain error	Excluding voltage reference error		0.1		%
	Gain drift	Excluding voltage reference drift		3		ppm/°C
	Gain match between channels			0.2		% of FS
CHANNEL PERFORMANCE (AC Performance)						
CMRR	Common-mode rejection ratio	f_{CM} = 50 Hz and 60 Hz (1)		–110		dB
PSRR	Power-supply rejection ratio	f_{PS} = 50 Hz and 60 Hz		–80		dB
	Crosstalk	f_{IN} = 50 Hz and 60 Hz		–110		dB
	Accuracy	1:3000 dynamic range with a 1-second measurement (V_{RMS} / I_{RMS})		0.1		%
SNR	Signal-to-noise ratio	f_{IN} = 50 Hz and 60 Hz, gain = 1		107		dB
THD	Total harmonic distortion	10 Hz, –0.5 dBFs		–93		dB
FAULT DETECT AND ALARM						
	Comparator threshold accuracy			±30		mV
EXTERNAL REFERENCE						
	Reference input voltage	AVDD = 3 V, V_{REF} = (VREFP – VREFN)		2.5		V
		AVDD = 5 V, V_{REF} = (VREFP – VREFN)		4		V
VREFN	Negative input			AVSS		V
VREFP	Positive input			AVSS + 2.5		V
	Input impedance			6		kΩ

(1) CMRR is measured with a common-mode signal of (AVSS + 0.3 V) to (AVDD – 0.3 V). The values indicated are the minimum of the eight channels.

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ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications apply from –40°C to +105°C. Typical specifications are at +25°C. All specifications are at DVDD = 1.8 V, AVDD = 3 V, AVSS = 0 V, V_{REF} = 2.4 V, external f_{CLK} = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

PARAMETER			TEST CONDITIONS	ADS131E0x MIN	ADS131E0x TYP	ADS131E0x MAX	UNIT
OPERATIONAL AMPLIFIER							
	Integrated noise		0.1 Hz to 250 Hz		9		μV_{RMS}
	Noise density		2 kHz		120		nV/√Hz
GBP	Gain bandwidth product		50 kΩ || 10-pF load		100		kHz
SR	Slew rate		50 kΩ || 10-pF load		0.25		V/µs
	Load current				50		µA
THD	Total harmonic distortion		f_{IN} = 100 Hz		70		dB
CMIR	Common-mode input range			AVSS + 0.7		AVDD – 0.3	V
	Quiescent power consumption				20		µA
INTERNAL REFERENCE							
V_O	Output voltage		CONFIG2.VREF_4V = 0		2.4		V
			CONFIG2.VREF_4V = 1		4		V
	V_{REF} accuracy				±0.2		%
	Temperature drift		0°C ≤ T_A ≤ +70°C		30		ppm/°C
			–40°C ≤ T_A ≤ +105°C		40		ppm/°C
	Start-up time		Settled to 0.2%		150		ms
SYSTEM MONITORS							
	Supply reading error	Analog			2		%
		Digital			2		%
	Device wake up		From power-up to $\overline{DRDY}$ low		150		ms
			STANDBY mode		31.25		µs
	Temperature sensor reading	Voltage	T_A = +25°C		145		mV
		Coefficient			490		µV/°C
SELF-TEST SIGNAL							
	Signal frequency		See *Register Map* section for settings		f_{CLK} / 2^{21}		Hz
					f_{CLK} / 2^{20}		Hz
	Signal voltage		See *Register Map* section for settings		±1		mV
					±2		mV
	Accuracy				±2		%
CLOCK							
	Internal oscillator clock frequency		Nominal frequency		2.048		MHz
			T_A = +25°C			±0.5	%
			–40°C ≤ T_A ≤ +105°C			2.5	%
	Internal oscillator start-up time				20		µs
	Internal oscillator power consumption				120		µW
	External clock input frequency		CLKSEL pin = 0, AVDD = 3 V	1.7	2.048	2.25	MHz
			CLKSEL pin = 0, AVDD = 5 V	0.7	2.048	2.25	MHz
DIGITAL INPUT AND OUTPUT (DVDD = 1.8 V to 3.6 V)							
V_{IH}	Logic level, input voltage	High		0.8 DVDD		DVDD + 0.1	V
V_{IL}		Low		–0.1		0.2 DVDD	V
V_{OH}	Logic level, output voltage	High	I_{OH} = –500 µA	0.9 DVDD			V
V_{OL}		Low	I_{OL} = +500 µA			0.1 DVDD	V
I_{IN}	Input current		0 V < $V_{DigitalInput}$ < DVDD	–10		+10	µA
POWER-SUPPLY REQUIREMENTS							
AVDD	Analog supply	AVDD – AVSS		2.7	3	5.25	V
DVDD	Digital supply			1.8	1.8	3.6	V
	AVDD – DVDD			–2.1		3.6	V

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ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications apply from –40°C to +105°C. Typical specifications are at +25°C. All specifications are at DVDD = 1.8 V, AVDD = 3 V, AVSS = 0 V, V_{REF} = 2.4 V, external f_{CLK} = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

PARAMETER			TEST CONDITIONS	ADS131E0x MIN	ADS131E0x TYP	ADS131E0x MAX	UNIT
SUPPLY CURRENT (Operational Amplifier Turned Off)							
I_{AVDD}	Normal mode		AVDD – AVSS = 3 V		5.1		mA
			AVDD – AVSS = 5 V		5.8		mA
I_{DVDD}			DVDD = 3.3 V		1		mA
			DVDD = 1.8 V		0.4		mA
POWER DISSIPATION (Analog Supply = 3 V)							
Quiescent power dissipation		ADS131E04	Normal mode		9.3	10.2	mW
			Power-down mode		10		µW
			Standby mode		2		mW
		ADS131E06	Normal mode		12.7	13.5	mW
			Power-down mode		10		µW
			Standby mode		2		mW
		ADS131E08	Normal mode		16	17.6	mW
			Power-down mode		10		µW
			Standby mode		2		mW
POWER DISSIPATION (Analog Supply = 5 V)							
Quiescent power dissipation		ADS131E04	Normal mode		18		mW
			Power-down mode		20		µW
			Standby mode		4.2		mW
		ADS131E06	Normal mode		24.3		mW
			Power-down mode		20		µW
			Standby mode		4.2		mW
		ADS131E08	Normal mode		29.7		mW
			Power-down mode		20		µW
			Standby mode		4.2		mW
TEMPERATURE							
T_A	Temperature range	Specified		–40		+105	°C
T_J		Operating		–40		+105	°C
T_{stg}		Storage		–60		+150	°C

THERMAL INFORMATION

THERMAL METRIC(1)		ADS131E0x PAG (TQFP) 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	35	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	31	
θ_{JB}	Junction-to-board thermal resistance	26	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	NA	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	NA	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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PARAMETER MEASUREMENT INFORMATION

NOISE MEASUREMENTS

The ADS131E0x noise performance can be optimized by adjusting the data rate and PGA setting. As the averaging is increased by reducing the data rate, the noise drops correspondingly. Increasing the PGA value reduces the input-referred noise, which is particularly useful when measuring low-level signals. Table 1 summarizes the ADS131E0x noise performance with a 3-V analog power supply. Table 2 summarizes the ADS131E0x noise performance with a 5-V analog power supply. The data are representative of typical noise performance at T_A = +25°C. The data shown are the result of averaging the readings from multiple devices and are measured with the inputs shorted together. A minimum of 1000 consecutive readings are used to calculate the RMS and peak-to-peak noise for each reading. For the two highest data rates, the noise is limited by ADC quantization noise and does not have a Gaussian distribution. Table 1 and Table 2 show measurements taken with an internal reference. The data are also representative of the ADS131E0x noise performance when using a low-noise external reference, such as the REF5025.

Table 1. Input-Referred Noise, 3-V Analog Supply, and 2.4-V Reference(1)

DR BITS (CONFIG1 Register)	OUTPUT DATA RATE (kSPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN									
			x1		x2		x4		x8		x12	
			DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB
000	64	16768	74.1	12.31	74.1	12.30	74.0	12.29	74.0	12.29	73.9	12.27
001	32	8384	89.6	14.89	89.6	14.88	89.4	14.85	88.6	14.71	87.6	14.55
010	16	4192	102.8	17.07	102.3	16.99	100.6	16.72	97.1	16.12	94.2	15.65
011	8	2096	108.2	18.0	107.4	17.9	105.2	17.5	101.6	16.9	98.9	16.5
100	4	1048	111.4	18.6	109.4	18.4	107.4	18.1	103.5	17.4	100.5	17.0
101	2	524	114.6	19.1	113.7	19.0	111.4	18.6	107.7	18.0	104.9	17.5
110	1	262	117.7	19.6	116.8	19.5	114.5	19.1	110.7	18.5	108.0	18.0

(1) At least 1000 consecutive readings were used to calculate the peak-to-peak noise values in this table.

Table 2. Input-Referred Noise, 5-V Analog Supply, and 4-V Reference

DR BITS (CONFIG1 Register)	OUTPUT DATA RATE (kSPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN									
			x1		x2		x4		x8		x12	
			DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB
000	64	16768	74.7	12.41	74.7	12.41	74.7	12.41	74.7	12.41	74.6	12.39
001	32	8384	90.3	15.01	90.3	15.00	90.2	14.99	89.9	14.93	89.4	14.85
010	16	4192	104.3	17.33	104.0	17.28	103.1	17.12	100.5	16.70	98.1	16.30
011	8	2096	112.3	18.7	111.6	18.6	109.7	18.3	106.3	17.7	103.8	17.3
100	4	1048	116.0	19.3	115.2	19.2	113.1	18.8	109.5	18.3	106.9	17.8
101	2	524	119.1	19.8	118.2	19.7	116.2	19.4	112.6	18.8	109.9	18.3
110	1	262	122.1	20.4	121.3	20.2	119.1	19.9	115.6	19.3	112.9	18.8

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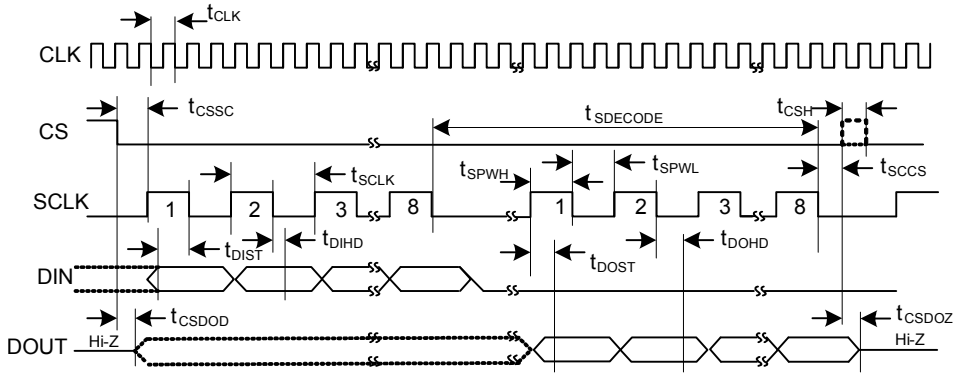
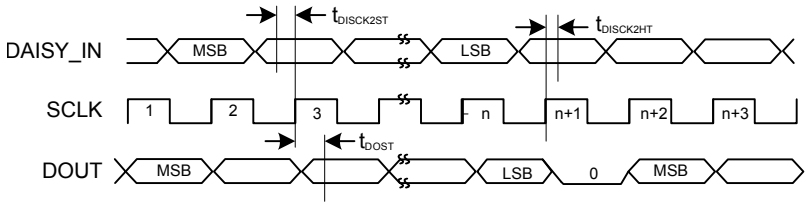
TIMING CHARACTERISTICS



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 1. Serial Interface Timing



(1) n = Number of channels × resolution + 24 bits. Number of channels is 4, 6, or 8; resolution is 16-bit or 24-bit.

Figure 2. Daisy-Chain Interface Timing

Timing Requirements For Figure 1 and Figure 2(1)

PARAMETER	DESCRIPTION	2.7 V ≤ DVDD ≤ 3.6 V		1.7 V ≤ DVDD ≤ 2.0 V		UNIT
		MIN	MAX	MIN	MAX	
t_{CLK}	Master clock period	444	588	444	588	ns
t_{CSSC}	$\overline{CS}$ low to first SCLK: setup time	6		17		ns
t_{SCLK}	SCLK period	50		66.6		ns
$t_{SPWH, L}$	SCLK pulse width, high and low	15		25		ns
t_{DIST}	DIN valid to SCLK falling edge: setup time	10		10		ns
t_{DIHD}	Valid DIN after SCLK falling edge: hold time	10		11		ns
t_{DOHD}	SCLK falling edge to invalid DOUT: hold time	10		10		ns
t_{DOST}	SCLK rising edge to DOUT valid: setup time		17		32	ns
t_{CSH}	$\overline{CS}$ high pulse	2		2		t_{CLKs}
t_{CSDOD}	$\overline{CS}$ low to DOUT driven	10		20		ns
t_{SCCS}	Eighth SCLK falling edge to $\overline{CS}$ high	4		4		t_{CLKs}
$t_{SDECODE}$	Command decode time	4		4		t_{CLKs}
t_{CSDOZ}	$\overline{CS}$ high to DOUT Hi-Z		10		20	ns
$t_{DISCK2ST}$	Valid DAISY_IN to SCLK rising edge: setup time	10		10		ns
$t_{DISCK2HT}$	Valid DAISY_IN after SCLK rising edge: hold time	10		10		ns

(1) Specifications apply from –40°C to +105°C, unless otherwise noted. Load on DOUT = 20 pF || 100 kΩ.

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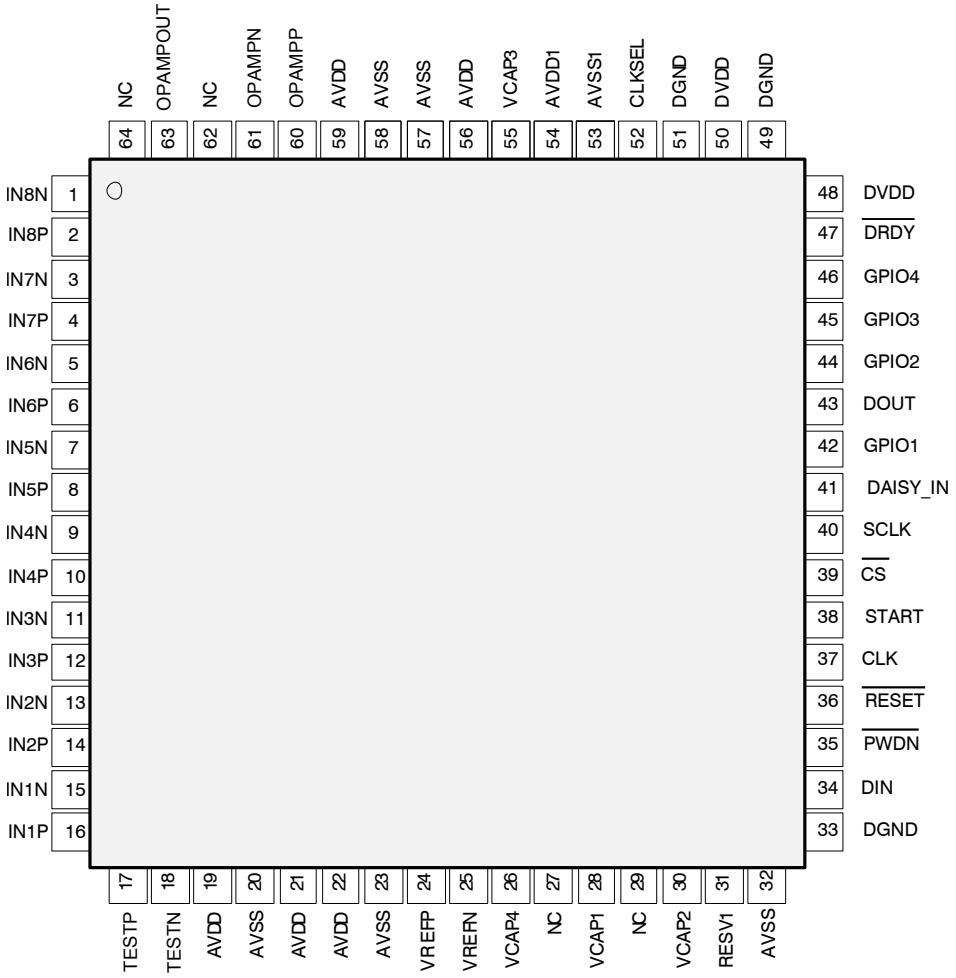
PIN CONFIGURATIONS

PAG PACKAGE
TQFP-32
(TOP VIEW)



PIN ASSIGNMENTS

NAME	TERMINAL	FUNCTION	DESCRIPTION
AVDD	19, 21, 22, 56, 59	Supply	Analog supply
AVDD1	54	Supply	Charge pump analog supply
AVSS	20, 23, 32, 57, 58	Supply	Analog ground
AVSS1	53	Supply	Charge pump analog ground
$\overline{CS}$	39	Digital input	SPI chip select; active low
CLK	37	Digital input	Master clock input
CLKSEL	52	Digital input	Master clock select
DAISY_IN	41	Digital input	Daisy-chain input
DGND	33, 49, 51	Supply	Digital ground
DIN	34	Digital input	SPI data in
DOUT	43	Digital output	SPI data out
$\overline{DRDY}$	47	Digital output	Data ready; active low
DVDD	48, 50	Supply	Digital power supply

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PIN ASSIGNMENTS (continued)

NAME	TERMINAL	FUNCTION	DESCRIPTION
GPIO1	42	Digital input/output	General-purpose input/output pin
GPIO2	44	Digital input/output	General-purpose input/output pin
GPIO3	45	Digital input/output	General-purpose input/output pin
GPIO4	46	Digital input/output	General-purpose input/output pin
IN1N(1)	15	Analog input	Differential analog negative input 1
IN1P(1)	16	Analog input	Differential analog positive input 1
IN2N(1)	13	Analog input	Differential analog negative input 2
IN2P(1)	14	Analog input	Differential analog positive input 2
IN3N(1)	11	Analog input	Differential analog negative input 3
IN3P(1)	12	Analog input	Differential analog positive input 3
IN4N(1)	9	Analog input	Differential analog negative input 4
IN4P(1)	10	Analog input	Differential analog positive input 4
IN5N(1)	7	Analog input	Differential analog negative input 5 (ADS131E06 and ADS131E08 only)
IN5P(1)	8	Analog input	Differential analog positive input 5 (ADS131E06 and ADS131E08 only)
IN6N(1)	5	Analog input	Differential analog negative input 6 (ADS131E06 and ADS131E08 only)
IN6P(1)	6	Analog input	Differential analog positive input 6 (ADS131E06 and ADS131E08 only)
IN7N(1)	3	Analog input	Differential analog negative input 7 (ADS131E08 only)
IN7P(1)	4	Analog input	Differential analog positive input 7 (ADS131E08 only)
IN8N(1)	1	Analog input	Differential analog negative input 8 (ADS131E08 only)
IN8P(1)	2	Analog input	Differential analog positive input 8 (ADS131E08 only)
NC	27, 29, 62, 64	—	No connection, leave floating
OPAMPN	61	Analog	Op amp inverting input
OPAMPP	60	—	Op amp noninverting input
OPAMPOUT	63	Analog	Op amp output
$\overline{\text{PWDN}}$	35	Digital input	Power-down; active low
$\overline{\text{RESET}}$	36	Digital input	System reset; active low
RESV1	31	Digital input	Reserved for future use; must tie to logic low (DGND)
SCLK	40	Digital input	SPI clock
START	38	Digital input	Start conversion
TESTN(1)	18	Analog input/output	Internal test signal, negative signal
TESTP(1)	17	Analog input/output	Internal test signal, positive signal
VCAP1	28	Analog input/output	Analog bypass capacitor
VCAP2	30	—	Analog bypass capacitor
VCAP3	55	—	Analog bypass capacitor
VCAP4	26	Analog output	Analog bypass capacitor
VREFN	25	Analog input	Negative reference voltage
VREFP	24	Analog input/output	Positive reference voltage

(1) Connect unused terminals to AVDD.

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TYPICAL CHARACTERISTICS

All plots are at T_A = +25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.4 V, VREFN = AVSS, external clock = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

INPUT-REFERRED NOISE

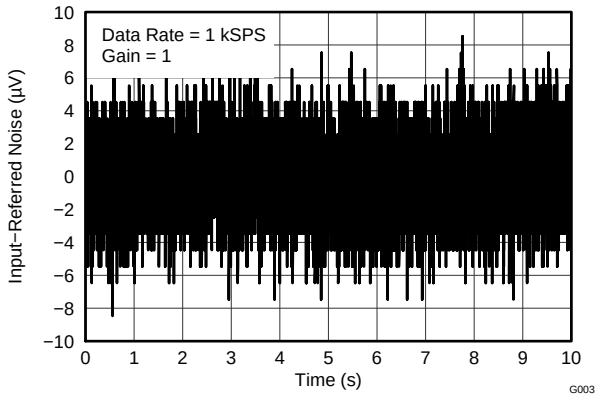

Figure 3.

NOISE HISTOGRAM

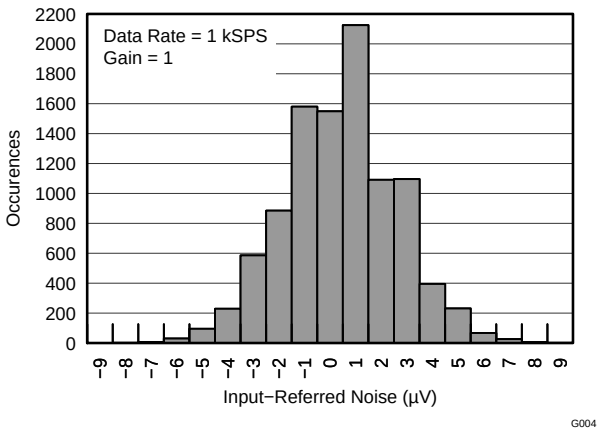

Figure 4.

CMRR vs FREQUENCY

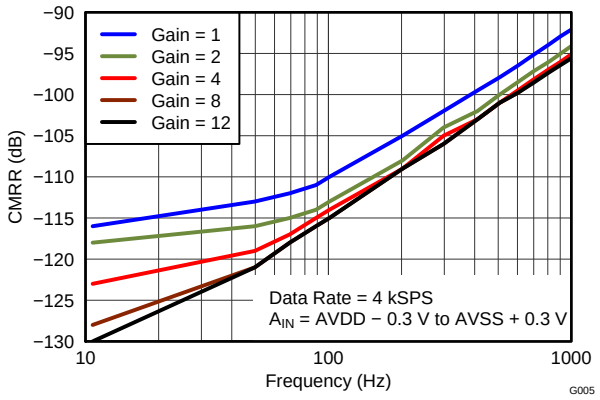

Figure 5.

THD vs FREQUENCY

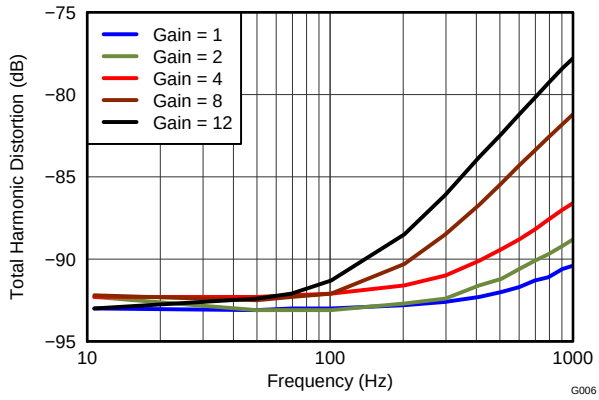

Figure 6.

PSRR vs FREQUENCY

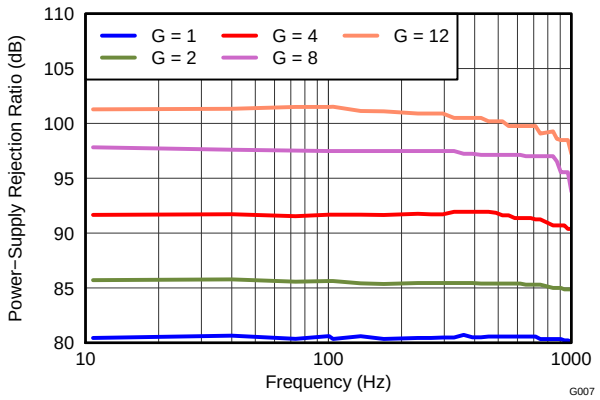

Figure 7.

INL vs PGA GAIN

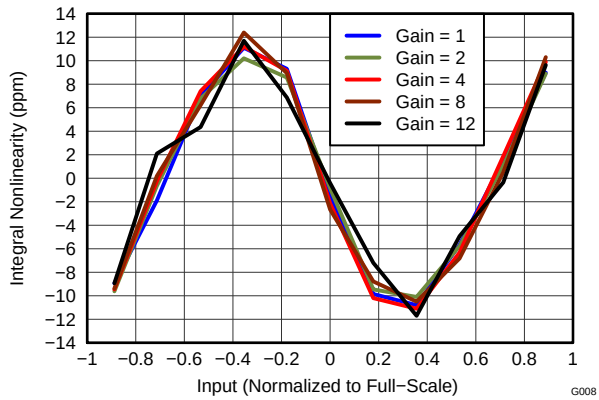

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

All plots are at T_A = +25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.4 V, VREFN = AVSS, external clock = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

INL vs TEMPERATURE

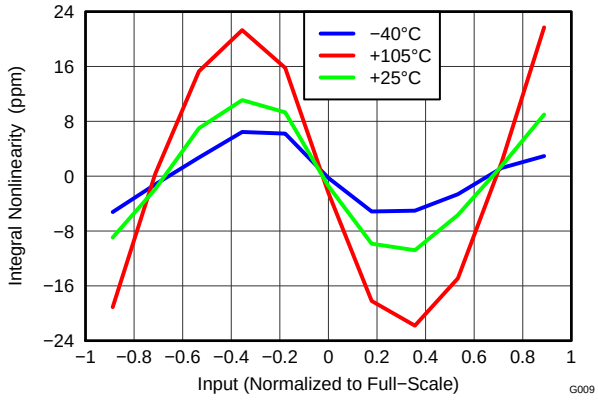

Figure 9.

THD FFT PLOT

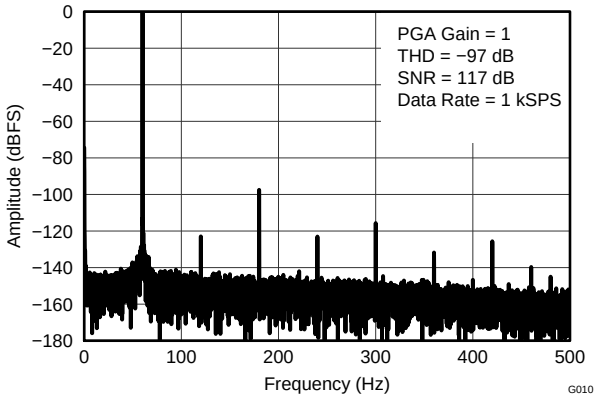

Figure 10.

FFT PLOT

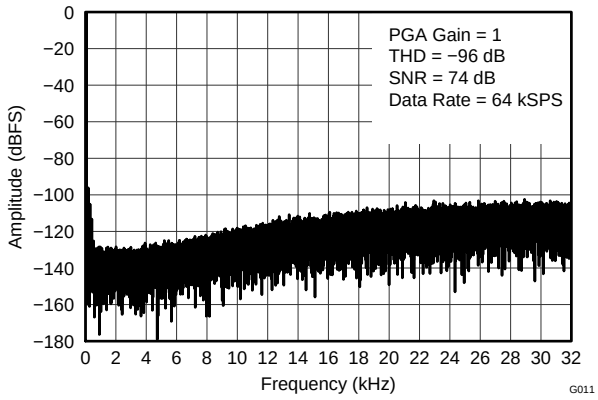

Figure 11.

OFFSET vs PGA GAIN (Absolute Value)

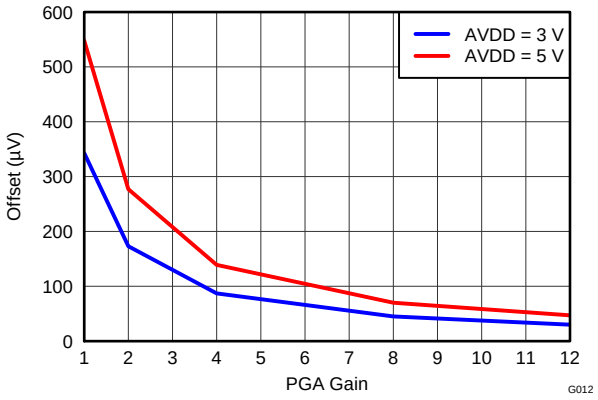

Figure 12.

OFFSET DRIFT vs PGA GAIN

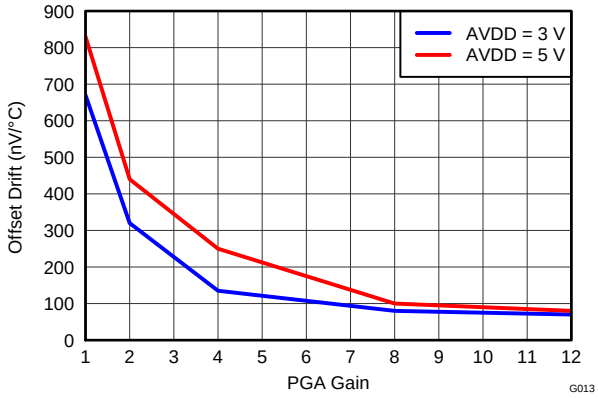

Figure 13.

ADS131E08 CHANNEL POWER

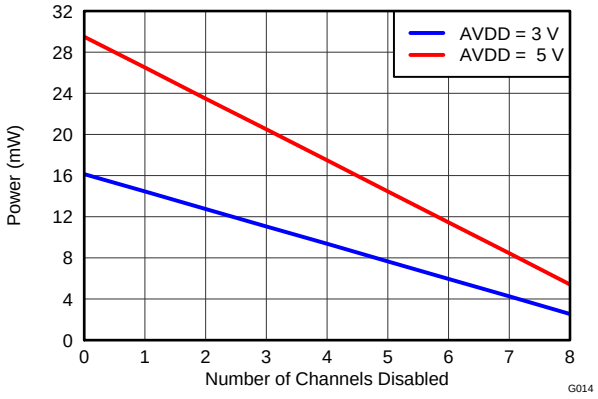

Figure 14.

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OVERVIEW

The ADS131E0x are low-power, multichannel, simultaneously-sampling, 24- and 16-bit delta-sigma (ΔΣ), analog-to-digital converters (ADCs) with an integrated programmable gain amplifier (PGA). This functionality makes these devices well-suited for smart-grid and other industrial power monitor, control, and protection applications.

The ADS131E0x have a highly-programmable multiplexer that allows for temperature, supply, and input short measurements. The PGA gain can be chosen from one of five settings (1, 2, 4, 8, and 12). The ADCs in the device offer data rates of 1, 2, 4, 8, 16, 32, and 64 kSPS. Device communication is accomplished using an SPI-compatible interface. The device provides four general-purpose I/O (GPIO) pins for general use. Multiple devices can be synchronized using the START pin.

The internal reference can be programmed to either 2.4 V or 4 V. The internal oscillator generates a 2.048-MHz clock. Open-circuit detection can be accomplished by using the integrated comparators, with programmable trigger-point settings. A detailed diagram of the ADS131E0x is shown in Figure 15.

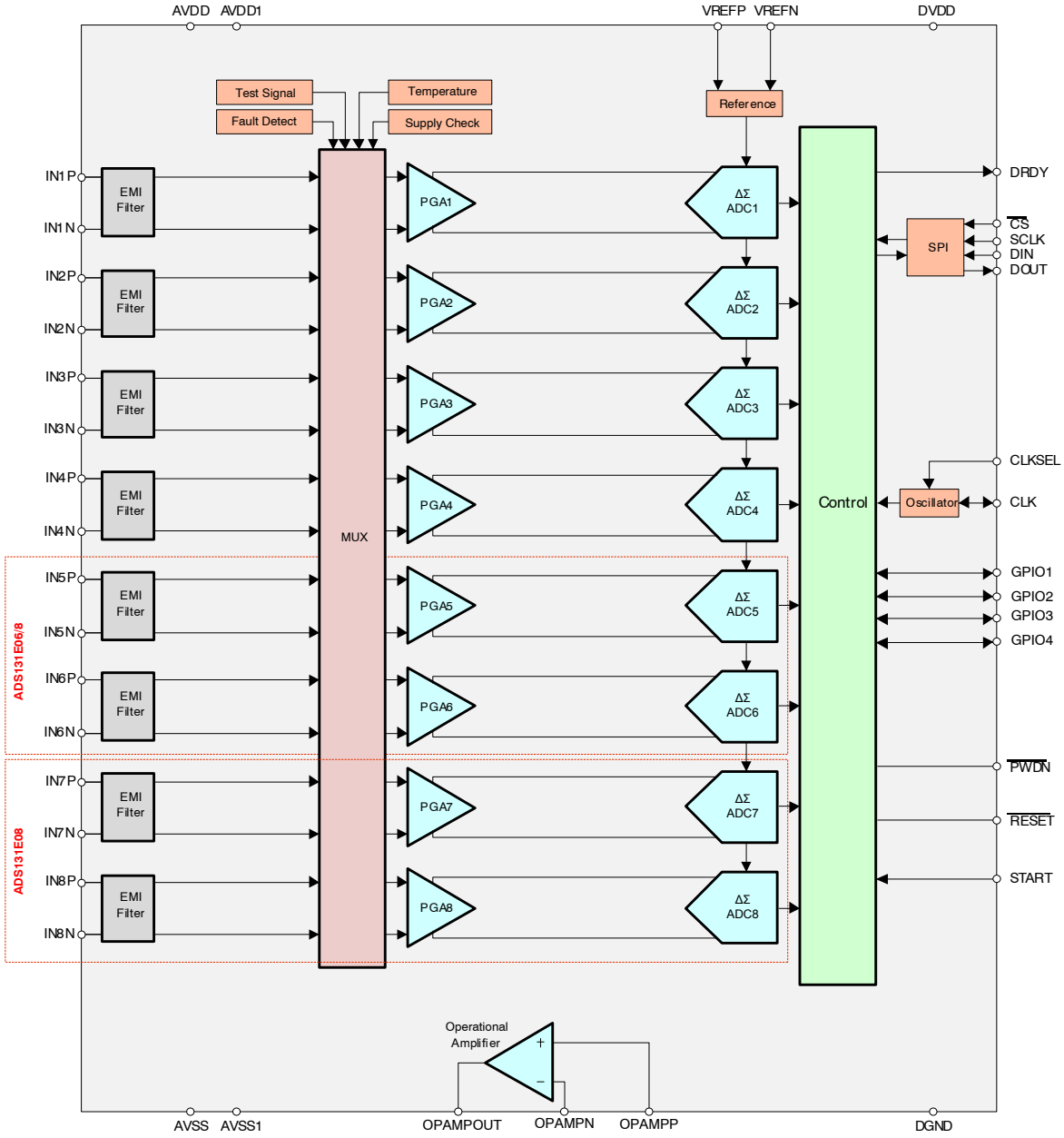

Figure 15. Functional Block Diagram

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THEORY OF OPERATION

This section contains details of the ADS131E0x internal functional elements. The analog blocks are discussed first, followed by the digital interface. Information on implementing power monitoring specific applications is covered towards the end of this document.

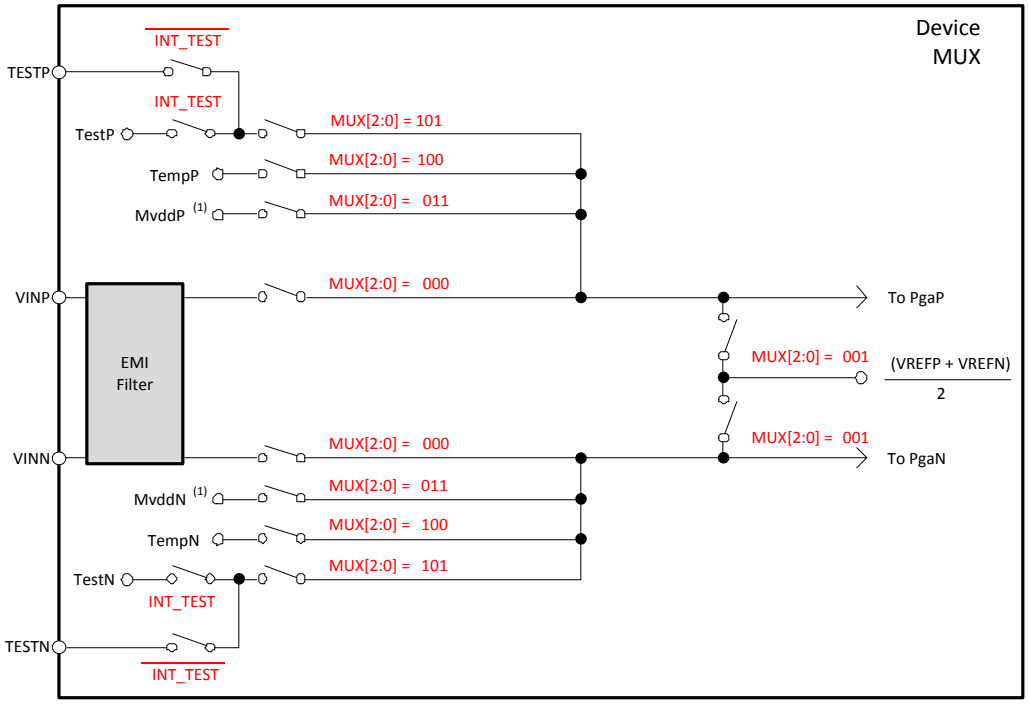
Throughout this document, f_{CLK} denotes the signal frequency at the CLK pin, t_{CLK} denotes the signal period at the CLK pin, f_{DR} denotes the output data rate, t_{DR} denotes the output data time period, and f_{MOD} denotes the frequency at which the modulator samples the input.

EMI FILTER

An RC filter at the input acts as an EMI filter on all channels. The –3-dB filter bandwidth is approximately 3 MHz.

INPUT MULTIPLEXER

The ADS131E0x input multiplexers are very flexible and provide many configurable signal switching options. Figure 16 shows a diagram of the multiplexer on a single channel of the device. VINP and VINN are separate for each of the eight blocks. This flexibility allows for significant device and sub-system diagnostics, calibration, and configuration. Switch settings for each channel are selected by writing the appropriate values to the CHnSET register (see the *CHnSET* Register in the *Register Map* section for details.)



(1) MVDD monitor voltage supply depends on channel number; see the *Supply Measurements (MVDDP, MVDDN)* section.

Figure 16. Input Multiplexer Block for One Channel

Device Noise Measurements

Setting CHnSET[2:0] = 001 sets the common-mode voltage of [(VREFP + VREFN) / 2] to both channel inputs. This setting can be used to test inherent device noise in the user system.

Test Signals (TestP and TestN)

Setting CHnSET[2:0] = 101 provides internally-generated test signals for use in sub-system verification at power-up. Test signals are controlled through register settings (see the *CONFIG2: Configuration Register 2* subsection in the *Register Map* section for details). TEST_AMP controls the signal amplitude and TEST_FREQ controls switching at the required frequency. The test signals are multiplexed and transmitted out of the device at the TESTP and TESTN pins. A bit register (CONFIG2.INT_TEST = 0) deactivates the internal test signals so that the test signal can be driven externally. This feature allows the calibration of multiple devices with the same signal.

Temperature Sensor (TempP, TempN)

The ADS131E0x contain an on-chip temperature sensor. This sensor uses two internal diodes with one diode having a current density 16x that of the other, as shown in Figure 17. The difference in diode current densities yields a difference in voltage that is proportional to absolute temperature.

As a result of the low thermal resistance of the package to the printed circuit board (PCB), the internal device temperature tracks the PCB temperature closely. Note that self-heating of the ADS131E0x causes a higher reading than the temperature of the surrounding PCB.

The scale factor of Equation 1 converts the temperature reading to °C. Before using this equation, the temperature reading code must first be scaled to µV.

$$\text{Temperature (°C)} = \left(\frac{\text{Temperature Reading (µV)} - 168{,}000\ \mu\text{V}}{394\ \mu\text{V/°C}} \right) + 25°\text{C} \quad (1)$$

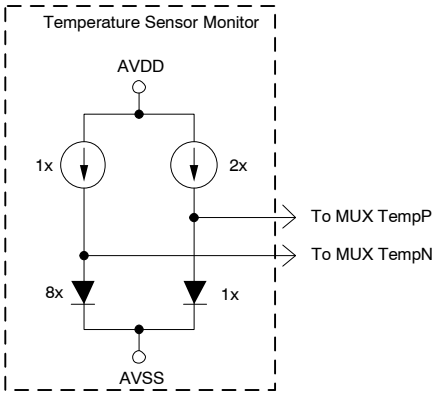


Figure 17. Temperature Sensor Measurement in the Input

Supply Measurements (MVDDP, MVDDN)

Setting CHnSET[2:0] = 011 sets the channel inputs to different device supply voltages. For channels 1, 2, 5, 6, 7, and 8, (MVDDP – MVDDN) is [0.5(AVDD – AVSS)]; for channels 3 and 4, (MVDDP – MVDDN) is DVDD / 4. Note that to avoid saturating the PGA while measuring power supplies, the gain must be set to '1'.

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ANALOG INPUT

The ADS131E0x analog input is fully differential. Assuming PGA = 1, the differential input (INP – INN) can span between $-V_{REF}$ to $+V_{REF}$. Refer to Table 5 for an explanation of the correlation between the analog input and digital codes. There are two general methods of driving the ADS131E0x analog input: single-ended or differential, as shown in Figure 18 and Figure 19, respectively. Note that INP and INN are 180°C out-of-phase in the differential input method. When the input is single-ended, the INN input is held at the common-mode voltage, preferably at mid-supply. The INP input swings around the same common voltage and the peak-to-peak amplitude is (common-mode + 1/2 V_{REF}) and (common-mode – 1/2 V_{REF}). When the input is differential, the common-mode is given by [(INP + INN) / 2]. Both INP and INN inputs swing from (common-mode + 1/2 V_{REF} to common-mode – 1/2 V_{REF}). For optimal performance, it is recommended that the ADS131E0x be used in a differential configuration.

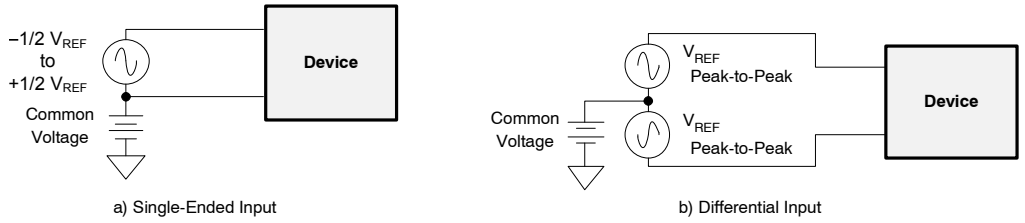

Figure 18. Methods of Driving the ADS131E0x: Single-Ended or Differential

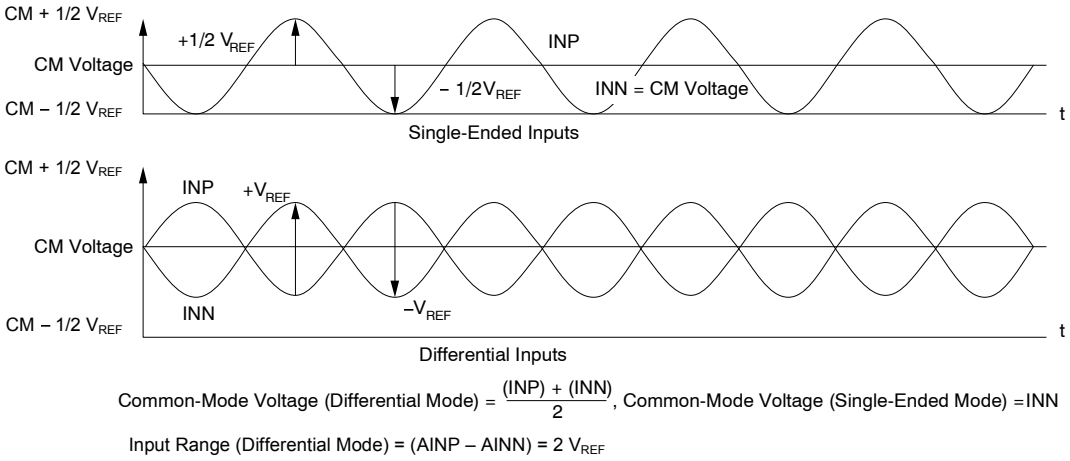

Figure 19. Using the ADS131E0x in Single-Ended and Differential Input Modes

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PGA SETTINGS AND INPUT RANGE

The PGA is a differential input and output amplifier, as shown in Figure 20. It has five gain settings (1, 2, 4, 8, and 12) that can be set by writing to the CHnSET register (see the *CHnSET* Register in the *Register Map* section for details). The ADS131E0x have CMOS inputs and therefore have negligible current noise. Table 3 shows the typical bandwidth values for various gain settings. Note that Table 3 shows small-signal bandwidth. For large signals, performance is limited by PGA slew rate.

The PGA resistor string that implements the gain has 120 kΩ of resistance for a gain of 2. This resistance provides a current path across the PGA outputs in the presence of a differential input signal. This current is in addition to the quiescent current specified for the device in the presence of a differential signal at the input.

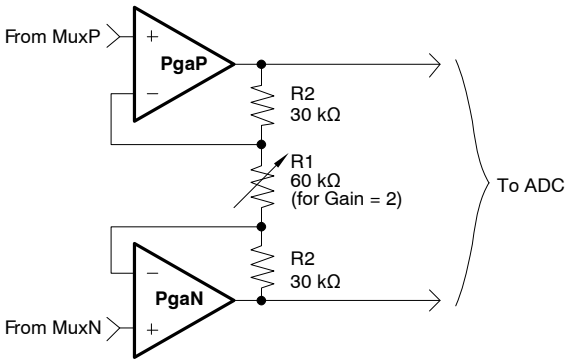

Figure 20. PGA Implementation

Table 3. PGA Gain versus Bandwidth

GAIN	NOMINAL BANDWIDTH AT ROOM TEMPERATURE (kHz)
1	237
2	146
4	96
8	48
12	32

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Input Common-Mode Range

The usable input common-mode range of the analog front-end depends on various parameters, including the maximum differential input signal, supply voltage, and PGA gain. This range is described in Equation 2:

$$AVDD - 0.3 - \left(\frac{\text{Gain } V_{MAX_DIFF}}{2}\right) > CM > AVSS + 0.3 + \left(\frac{\text{Gain } V_{MAX_DIFF}}{2}\right) \quad (2)$$

where:

V_{MAX_DIFF} = maximum differential signal at the PGA input

CM = common-mode range

For example:

If V_{DD} = 3.3 V, gain = 2, and V_{MAX_DIFF} = 1000 mV,
Then 1.3 V < CM < 2.0 V

Input Differential Dynamic Range

The differential (INP – INN) signal range depends on the analog supply and reference used in the system. This range is shown in Equation 3.

$$\text{Max (INP} - \text{INN)} < \frac{V_{REF}}{\text{Gain}} \quad ; \quad \text{Full-Scale Range} = \frac{\pm V_{REF}}{\text{Gain}} = \frac{2\ V_{REF}}{\text{Gain}} \quad (3)$$

For higher dynamic range, a 5-V supply with a 4-V reference (set by the VREF_4V bit of the CONFIG3 register) can be used to increase the differential dynamic range.

ADC ΔΣ Modulator

Each ADS131E0x channel has a ΔΣ ADC. This converter uses a second-order modulator optimized for low-power applications. The modulator samples the input signal at the rate of [$f_{MOD} = f_{CLK} / 2$]. As in the case of any ΔΣ modulator, the ADS131E0x noise is shaped until $f_{MOD} / 2$, as shown in Figure 21. The on-chip digital decimation filters also provide antialias filtering. This ΔΣ converter feature drastically reduces the complexity of the analog antialiasing filters typically required with nyquist ADCs.

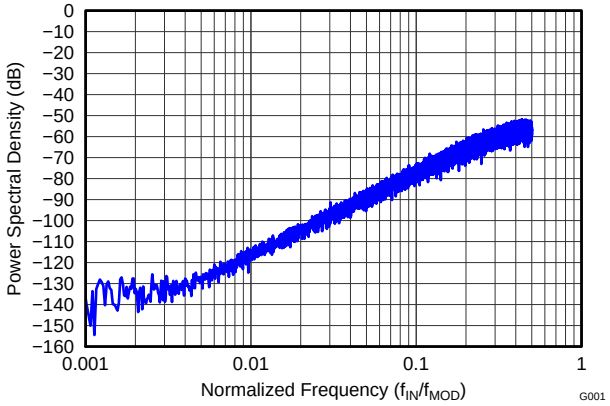

Figure 21. Modulator Noise Spectrum Up To 0.5 × f_{MOD}

DIGITAL DECIMATION FILTER

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rates. Higher data rates are typically used in power applications that implement software phase adjustment.

The digital filter on each channel consists of a third-order sinc filter. The decimation ratio on the sinc filters can be adjusted by the DR bits in the CONFIG1 register (see the *Register Map* section for details). This setting is a global setting that affects all channels and, therefore, all channels operate at the same data rate in the device.

Sinc Filter Stage (sinx / x)

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD}. The sinc filter attenuates the high-frequency modulator noise, then decimates the data stream into parallel data. The decimation rate affects the overall converter data rate.

Equation 4 shows the scaled sinc filter Z-domain transfer function.

$$\left|H(z)\right| = \left|\frac{1 - Z^{-N}}{1 - Z^{-1}}\right|^{3} \tag{4}$$

The sinc filter frequency domain transfer function is shown in Equation 5.

$$\left|H(f)\right| = \left|\frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)}\right|^{3}$$

where:

N = decimation ratio (5)

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The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. Figure 22 shows the sinc filter frequency response and Figure 23 shows the sinc filter roll-off. With a step change at the input, the filter takes 3 t_{DR} to settle. After a rising edge of the START signal, the filter takes t_{SETTLE} time to output settled data. The filter settling times at various data rates are discussed in the *START* subsection of the *SPI Interface* section. Figure 24 and Figure 25 show the filter transfer function until f_{MOD} / 2 and f_{MOD} / 16, respectively, at different data rates. Figure 26 shows the transfer function extended until 4 f_{MOD}. It can be seen that the ADS131E0x passband repeats itself at every f_{MOD}. The input R-C antialiasing filters in the system should be chosen such that any interference in frequencies around multiples of f_{MOD} are attenuated sufficiently.

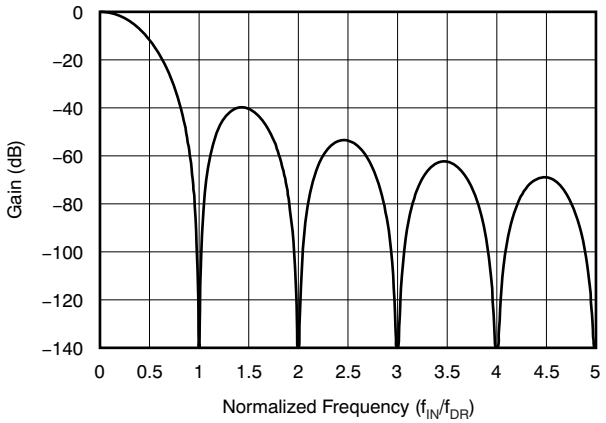

Figure 22. Sinc Filter Frequency Response

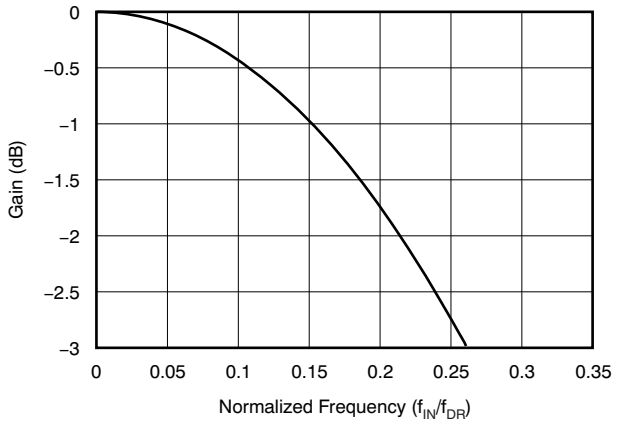

Figure 23. Sinc Filter Roll-Off

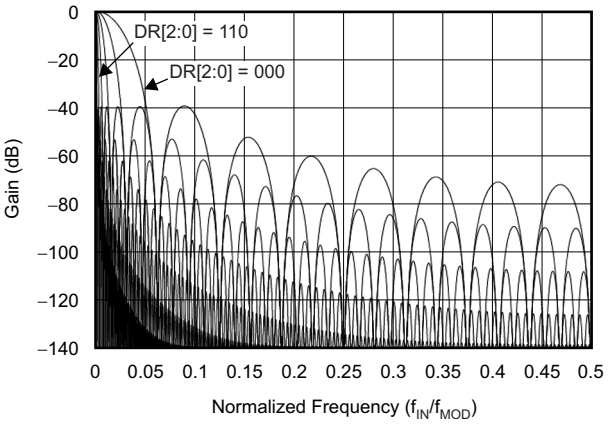

Figure 24. Transfer Function of On-Chip Decimation Filters Until f_{MOD} / 2

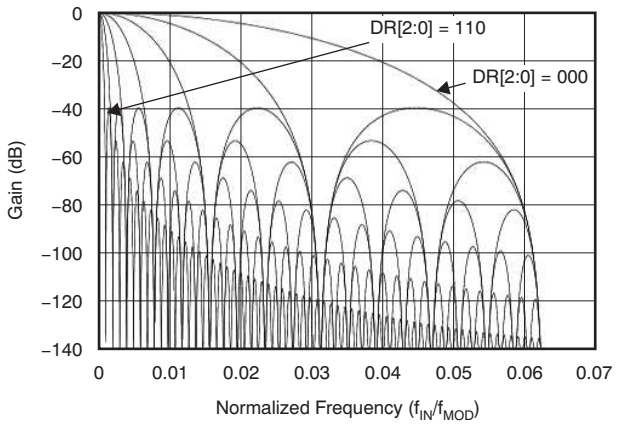

Figure 25. Transfer Function of On-Chip Decimation Filters Until f_{MOD} / 16

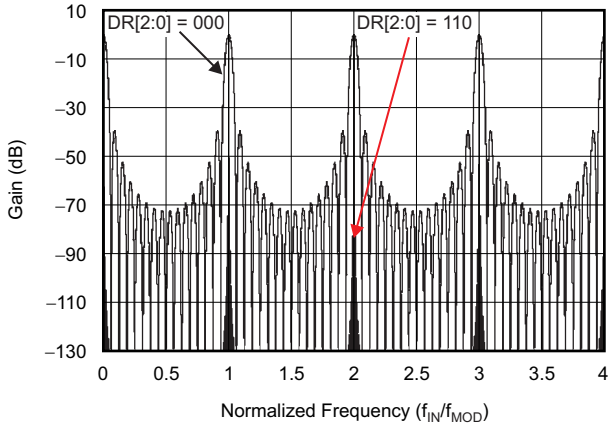

Figure 26. Transfer Function of On-Chip Decimation Filters Until 4 f_{MOD} for DR[2:0] = 000 and DR[2:0] = 110

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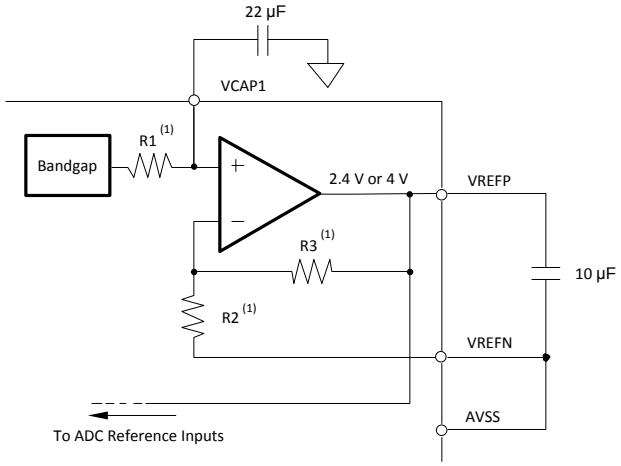
REFERENCE

Figure 27 shows a simplified block diagram of the internal ADS131E0x reference. The reference voltage is generated with respect to AVSS. When using the internal voltage reference, connect VREFN to AVSS.



(1) For V_{REF} = 2.4 V: R1 = 12.5 kΩ, R2 = 25 kΩ, and R3 = 25 kΩ. For V_{REF} = 4 V: R1 = 10.5 kΩ, R2 = 15 kΩ, and R3 = 35 kΩ.

Figure 27. Internal Reference

The external band-limiting capacitors determine the amount of reference noise contribution. For high-end systems, the capacitor values should be chosen such that the bandwidth is limited to less than 10 Hz, so that the reference noise does not dominate the system noise. When using a 3-V analog supply, the internal reference must be set to 2.4 V. In case of a 5-V analog supply, the internal reference can be set to 4 V by setting the VREF_4V bit in the CONFIG2 register.

Alternatively, the internal reference buffer can be powered down and VREFP can be driven externally. Figure 28 shows a typical external reference drive circuitry. Power-down is controlled by the $\overline{\text{PD_REFBUF}}$ bit in the CONFIG3 register. This power-down is also used to share internal references when two devices are cascaded. By default, the device wakes up in external reference mode.

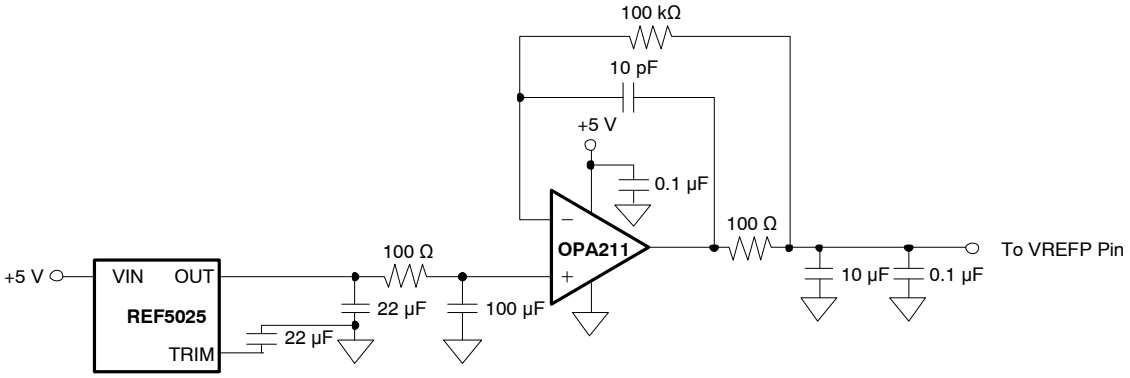


Figure 28. External Reference Driver

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CLOCK

The ADS131E0x provide two different device clocking methods: internal and external. Internal clocking is ideally suited for low-power, battery-powered systems. The internal oscillator is trimmed for accuracy at room temperature. Accuracy varies over the specified temperature range; refer to the Electrical Characteristics for details. Clock selection is controlled by the CLKSEL pin and the CLK_EN register bit.

The CLKSEL pin selects either the internal or external clock. The CLK_EN bit in the CONFIG1 register enables and disables the oscillator clock to be output in the CLK pin. A truth table for these two pins is shown in Table 4. The CLK_EN bit is useful when multiple devices are used in a daisy-chain configuration. It is recommended that during power-down the external clock be shut down to save power.

Table 4. CLKSEL Pin and CLK_EN Bit

CLKSEL PIN	CONFIG1.CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal clock oscillator	3-state
1	1	Internal clock oscillator	Output: internal clock oscillator

DATA FORMAT

The ADS131E0x output resolution is dependent upon the DR[2:0] bit setting in the CONFIG1 register. When DR[2:0] = 000 or 001, the 16 bits of data per channel are sent in binary twos complement format, MSB first. The LSB has a weight of V_{REF} / (2^{15} – 1). A positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals exceeding full-scale. Table 5 summarizes the ideal output codes for different input signals. All 16 bits toggle when the analog input is at positive or negative full-scale.

Table 5. Ideal Output Code versus Input Signal, LSB Weight = V_{REF} / (2^{15} – 1)

INPUT SIGNAL, V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(1)(2)
≥ V_{REF}	7FFFh
+V_{REF} / (2^{15} – 1)	0001h
0	0000h
–V_{REF} / (2^{15} – 1)	FFFFh
≤ –V_{REF} (2^{15} / 2^{15} – 1)	8000h

(1) Assumes gain = 1.
(2) Excludes effects of noise, linearity, offset, and gain error.

When DR[2:0] = 010, 011, 100, 101, or 110, the ADS131E0x outputs 24 bits of data per channel in binary twos complement format, MSB first. The LSB has a weight of V_{REF} / (2^{23} – 1). A positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 6 summarizes the ideal output codes for different input signals.

Table 6. Ideal Output Code versus Input Signal, LSB Weight = V_{REF} / (2^{23} – 1)

INPUT SIGNAL, V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE
≥ V_{REF}	7FFFFFh
+V_{REF} / (2^{23} – 1)	000001h
0	000000h
–V_{REF} / (2^{23} – 1)	FFFFFFh
≤ –V_{REF} (2^{23} / 2^{23} – 1)	800000h

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SPI INTERFACE

The SPI-compatible serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. The interface reads conversion data, reads and writes registers, and controls the ADS131E0x operation. The $\overline{DRDY}$ output is used as a status signal to indicate when data are ready. $\overline{DRDY}$ goes low when new data are available.

Chip Select ($\overline{CS}$)

Chip select ($\overline{CS}$) selects the ADS131E0x for SPI communication. $\overline{CS}$ must remain low for the entire serial communication duration. After the serial communication is finished, four or more t_{CLK} cycles must elapse before taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK and DIN are ignored, and DOUT enters a high-impedance state. $\overline{DRDY}$ asserts when data conversion is complete, regardless of whether $\overline{CS}$ is high or low.

Serial Clock (SCLK)

SCLK is the serial peripheral interface (SPI) serial clock. It is used to shift in commands and shift out data from the device. The serial clock (SCLK) features a Schmitt-triggered input and clocks data on the DIN and DOUT pins into and out of the ADS131E0x.

Care should be taken to prevent glitches on SCLK while $\overline{CS}$ is low. Glitches as small as 1 ns wide could be interpreted as a valid serial clock. After eight serial clock events, the ADS131E0x assume an instruction must be interrupted and executed. If it is suspected that instructions are being interrupted erroneously, toggle $\overline{CS}$ high and back low to return the chip to normal operation. It is also recommended to issue serial clocks in multiples of eight. The absolute maximum SCLK limit is specified in the *Serial Interface Timing* table.

For a single device, the minimum speed needed for SCLK depends on the number of channels, number of bits of resolution, and output data rate. (For multiple cascaded devices, see the *Standard Mode* subsection of the *Multiple Device Configuration* section.) The SCLK rate limitation, as described by Equation 6, applies to RDATAC mode.

$$t_{SCLK} < (t_{DR} - 4\ t_{CLK}) / (N_{BITS}N_{CHANNELS} + 24) \quad (6)$$

For example, if the ADS131E0x is used in an 8-kSPS mode (eight channels, 24-bit resolution), the minimum SCLK speed is 1.72 MHz.

Data retrieval can be done either by putting the device in RDATAC mode or by issuing an RDATA command for data on demand. The SCLK rate limitation, as described by Equation 6, applies to RDATAC mode. For the RDATA command, the limitation applies if data must be read in between two consecutive $\overline{DRDY}$ signals. The above calculation assumes that there are no other commands issued in between data captures.

Data Input (DIN)

The data input pin (DIN) is used along with SCLK to communicate with the ADS131E0x (opcode commands and register data). The device latches data on DIN on the SCLK falling edge.

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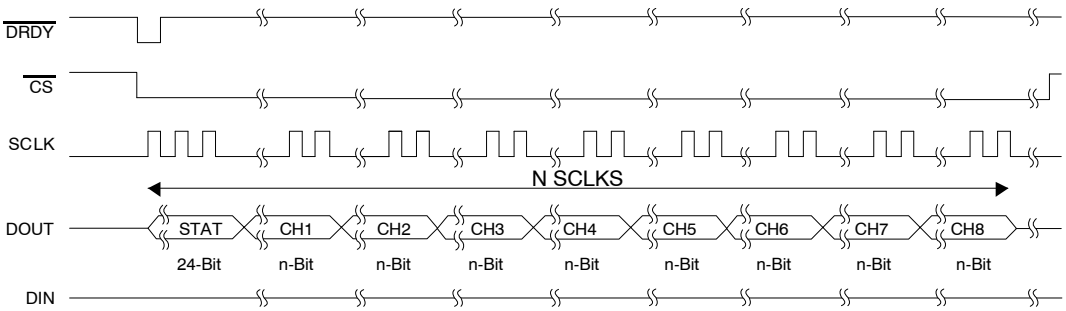
Data Output (DOUT)

The data output pin (DOUT) is used with SCLK to read conversion and register data from the ADS131E0x. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high-impedance state when $\overline{CS}$ is high. In read data continuous mode (see the *SPI Command Definitions* section for more details), the DOUT output line also indicates when new data are available. This feature can be used to minimize the number of connections between the device and system controller.

Figure 29 shows the ADS131E0x data output protocol.



NOTE: N SCLKs = (N bits)(N channels) + 24 bits. N-bit is dependent upon the DR[2:0] registry bit settings (N = 16 or 24).

Figure 29. ADS131E0x SPI Bus Data Output (Eight Channels)

Data Retrieval

Data retrieval can be accomplished in one of two methods. The read data continuous command (see the *RDATAC: Read Data Continuous* section) can be used to set the device in a mode to read the data continuously without sending opcodes. The read data command (see the *RDATA: Read Data* section) can be used to read just one data output from the device (see the *SPI Command Definitions* section for more details). The conversion data are read by shifting the data out on DOUT. The MSB of the data on DOUT is clocked out on the first SCLK rising edge. $\overline{DRDY}$ returns to high on the first SCLK falling edge. DIN should remain low for the entire read operation.

The number of bits in the data output depends on the number of channels and the number of bits per channel. For the ADS131E0x with 32- and 64-kSPS data rates, the number of data outputs is [(24 status bits + 16 bits × 8 channels) = 152 bits]. The format of the 24 status bits is (1100 + FAULT_STATP + FAULT_STATN + GPIO[7:4]). The data format for each channel data are twos complement and MSB first. When channels are powered down using the user register setting, the corresponding channel output is set to '0'. However, the sequence of channel outputs remains the same. The last four (ADS131E04) or two (ADS131E06) channel outputs shown in Figure 29 are '0's.

The ADS131E0x also provide a multiple readback feature. The data can be read out multiple times by simply giving more SCLKs, in which case the MSB data byte repeats after reading the last byte. The DAISY_IN bit in the CONFIG1 register must be set to '1' for multiple readbacks.

Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ is an output. When it transitions low, new conversion data are ready. The $\overline{CS}$ signal has no effect on the data ready signal. $\overline{DRDY}$ behavior is determined by whether the device is in RDATAC mode or the RDATA command is being used to read data on demand. (See the *RDATAC: Read Data Continuous* and *RDATA: Read Data* subsections of the *SPI Command Definitions* section for further details).

When reading data with the RDATA command, the read operation can overlap the next $\overline{DRDY}$ occurrence without data corruption.

The START pin or the START command is used to place the device either in normal data capture mode or pulse data capture mode.

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Figure 30 shows the relationship between $\overline{\text{DRDY}}$, DOUT, and SCLK during data retrieval (in case of an ADS131E0x with a selected data rate that gives 16-bit resolution). DOUT is latched out at the SCLK rising edge; $\overline{\text{DRDY}}$ is pulled high at the SCLK falling edge. Note that $\overline{\text{DRDY}}$ goes high on the first SCLK falling edge regardless of whether data are being retrieved from the device or a command is being sent through the DIN pin. For 24-bit resolution, the data starts from bit 215.

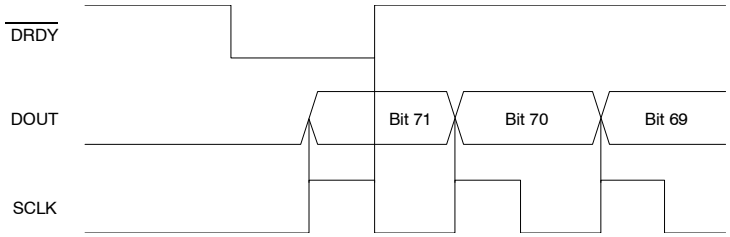

Figure 30. $\overline{\text{DRDY}}$ with Data Retrieval ($\overline{\text{CS}}$ = 0)

GPIO

The ADS131E0x have a total of four general-purpose digital I/O (GPIO) pins available in the normal mode of operation. The digital I/O pins are individually configurable as either inputs or outputs through the GPIOC bits register. The GPIOD bits in the GPIO register control the level of the pins. When reading the GPIOD bits, the data returned are the logic level of the pins, whether they are programmed as inputs or outputs. When the GPIO pin is configured as an input, a write to the corresponding GPIOD bit has no effect. When configured as an output, a write to the GPIOD bit sets the output value.

If configured as inputs, these pins must be driven (do not float). The GPIO pins are set as inputs after power-on or after a reset. Figure 31 shows the GPIO port structure. The pins should be shorted to DGND if not used.

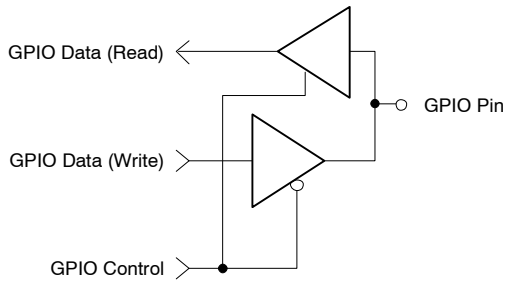

Figure 31. GPIO Port Pin

Power-Down ($\overline{\text{PWDN}}$)

When $\overline{\text{PWDN}}$ is pulled low, all on-chip circuitry is powered down. To exit power-down mode, take the $\overline{\text{PWDN}}$ pin high. Upon exiting from power-down mode, the internal oscillator and the reference require time to wake up. It is recommended that during power-down the external clock is shut down to save power.

Reset ($\overline{\text{RESET}}$)

There are two methods to reset the ADS131E0x: pull the $\overline{\text{RESET}}$ pin low, or send the $\overline{\text{RESET}}$ opcode command. When using the $\overline{\text{RESET}}$ pin, take it low to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the $\overline{\text{RESET}}$ pin back high. The $\overline{\text{RESET}}$ command takes effect on the eighth SCLK falling edge of the opcode command. On reset it takes 18 t_{CLK} cycles to complete initialization of the configuration registers to the default states and start the conversion cycle. Note that an internal $\overline{\text{RESET}}$ is automatically issued to the digital filter whenever the CONFIG1 register is set to a new value with a WREG command.

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START

The START pin must be set high (for a minimum of 2 t_{CLK}s) or the START command sent to begin conversions. When START is low, or if the START command has not been sent, the device does not issue a $\overline{DRDY}$ signal (conversions are halted).

When using the START opcode to control conversion, hold the START pin low. In multiple device configurations the START pin is used to synchronize devices (see the *Multiple Device Configuration* subsection of the *SPI Interface* section for more details).

Settling Time

The settling time (t_{SETTLE}) is the time it takes for the converter to output fully-settled data when the START signal is pulled high. Once START is pulled high, $\overline{DRDY}$ is also pulled high. The next $\overline{DRDY}$ falling edge indicates that data are ready. Figure 32 shows the timing diagram and Table 7 shows the settling time for different data rates. The settling time depends on f_{CLK} and the decimation ratio (controlled by the DR[2:0] bits in the CONFIG1 register). Table 5 shows the settling time as a function of t_{CLK}. Note that when START is held high and there is a step change in the input signal, it takes 3 t_{DR} for the filter to settle to the new value. Settled data are available on the fourth $\overline{DRDY}$ pulse.

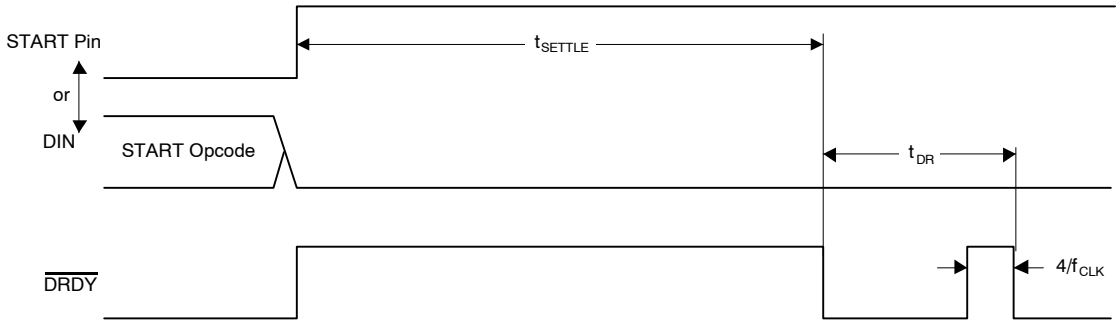

Figure 32. Settling Time

Table 7. Settling Time for Different Data Rates

DR[2:0]	SETTLING TIME	UNIT
000	152	t_{CLK}
001	296	t_{CLK}
010	584	t_{CLK}
011	1160	t_{CLK}
100	2312	t_{CLK}
101	4616	t_{CLK}
110	9224	t_{CLK}

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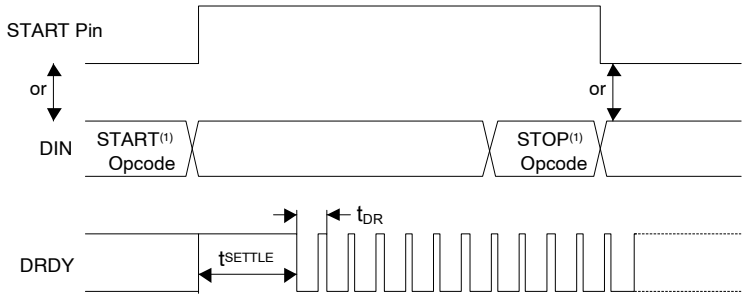
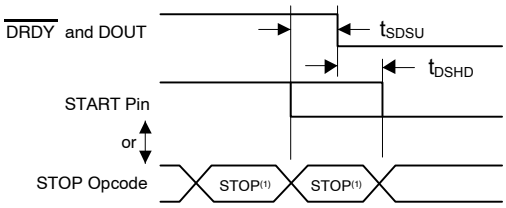
Continuous Mode

Conversions begin when the START pin is taken high or when the START opcode command is sent. As seen in Figure 33, the $\overline{\text{DRDY}}$ output goes high when conversions are started and then goes low when data are ready. Conversions continue indefinitely until the START pin is taken low or the STOP opcode command is transmitted. When the START pin is pulled low or the stop command is issued, the conversion in progress is allowed to complete. Figure 34 and Table 8 show the required $\overline{\text{DRDY}}$ timing to the START pin and the START and STOP opcode commands when controlling conversions in this mode. To keep the converter running continuously, the START pin can be permanently tied high.



(1) START and STOP opcode commands take effect on the seventh SCLK falling edge.

Figure 33. Continuous Conversion Mode



(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Figure 34. START to $\overline{\text{DRDY}}$ Timing

Table 8. Timing Characteristics for Figure 34(1)

SYMBOL	DESCRIPTION	MIN	UNIT
t_{SDSU}	START pin low or STOP opcode to $\overline{\text{DRDY}}$ setup time to halt further conversions	16	1/2 f_{MOD}
t_{DSHD}	START pin low or STOP opcode to complete current conversion	16	1/2 f_{MOD}

(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

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MULTIPLE DEVICE CONFIGURATION

The ADS131E0x are designed to provide configuration flexibility when multiple devices are used in a system. The serial interface typically needs four signals: DIN, DOUT, SCLK, and $\overline{CS}$. With one additional chip select signal per device, multiple devices can be connected together. The number of signals needed to interface *n* devices is 3 + *n*.

To use the internal oscillator in a daisy-chain configuration, one device must be set as the master for the clock source with the internal oscillator enabled (CLKSEL pin = 1) and the internal oscillator clock brought out of the device by setting the $\overline{CLK_EN}$ register bit to '1'. This master device clock is used as the external clock source for the other devices.

When using multiple devices, the devices can be synchronized with the START signal. The delay from START to the $\overline{DRDY}$ signal is fixed for a fixed data rate (see the *START* subsection of the *SPI Interface* section for more details on the settling times). Figure 35 shows the behavior of two devices when synchronized with the START signal.

There are two ways to connect multiple devices with an optimal number of interface pins: standard mode and daisy-chain mode. Refer to the *Standard Mode* and *Daisy-Chain Mode* sections for details.

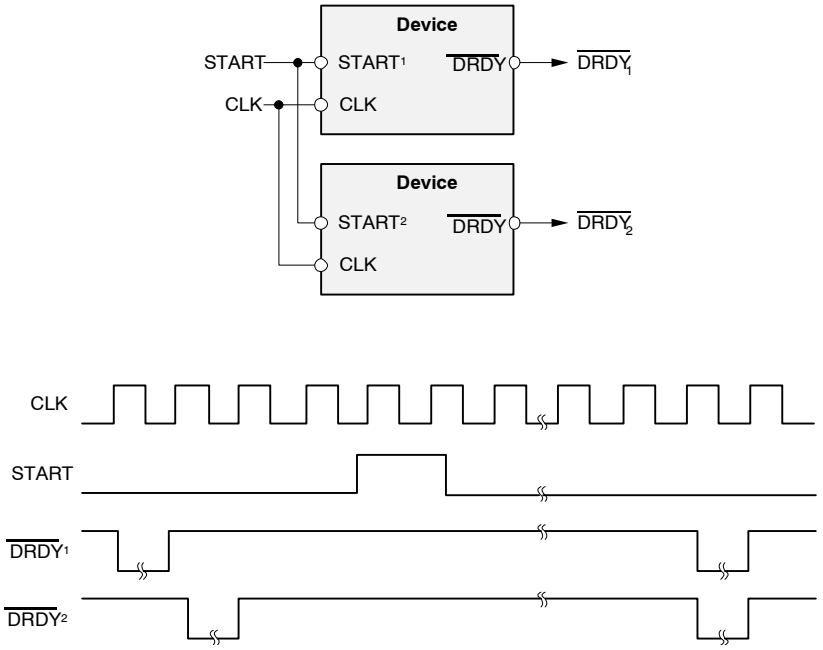

Figure 35. Synchronizing Multiple Converters

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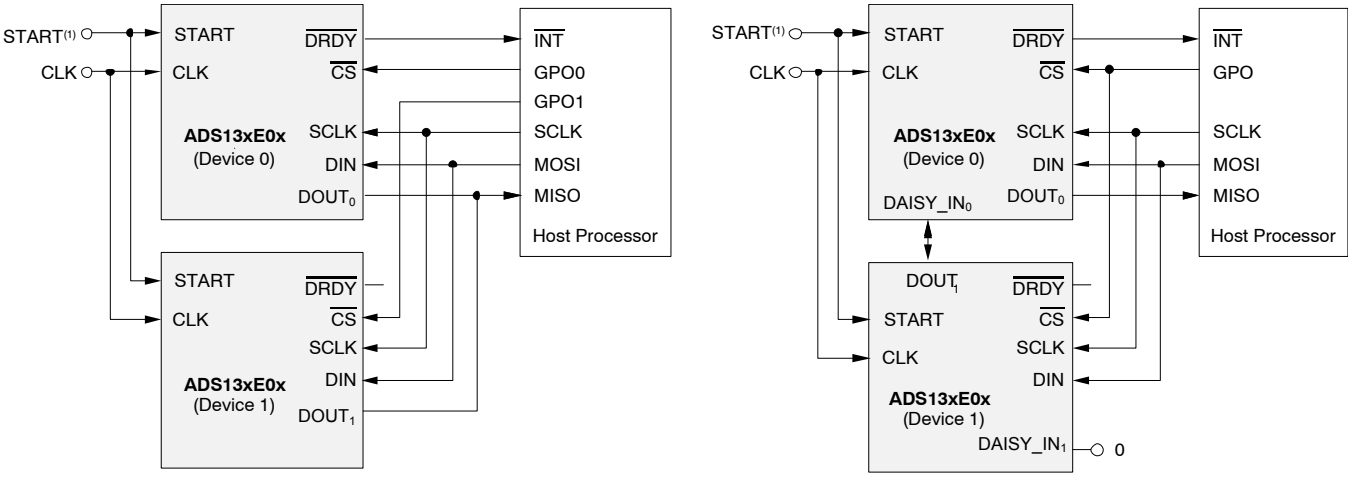
Standard Mode

Figure 36a shows a configuration with two devices cascaded together. Both devices are an ADS131E0x (eight-channel) device. Together, they create a system with 16 channels. DOUT, SCLK, and DIN are shared. Each device has its own chip select. When a device is not selected by the corresponding $\overline{CS}$ being driven to logic 1, the DOUT of this device is high-impedance. This structure allows the other device to take control of the DOUT bus. This configuration method is suitable for the majority of applications.

Daisy-Chain Mode

Daisy-chain mode is enabled by setting the DAISY_IN bit in the CONFIG1 register. Figure 36b shows the daisy-chain configuration. In this mode SCLK, DIN, and $\overline{CS}$ are shared across multiple devices. The DOUT pin of device 1 is connected to the DAISY_IN of device 0, thereby creating a daisy-chain for the data. One extra SCLK must be issued between each data set. Also, when using daisy-chain mode, the multiple readback feature is not available. Short the DAISY_IN pin to digital ground if not used. Figure 2 describes the required ADS131E0x timing shown in Figure 36. Data from the ADS131E0x appear first on DOUT, followed by a *don't care* bit, and finally by the status and data words from the second ADS131E0x device.

When all devices in the chain operate in the same register setting, DIN can be shared as well and thereby reduce the SPI communication signals to four, regardless of the number of devices. Furthermore, an external clock must be used.



a) Standard Configuration

b) Daisy-Chain Configuration

(1) To reduce pin count, set the START pin low and use the START serial command to synchronize and start conversions.

Figure 36. Multiple Device Configurations

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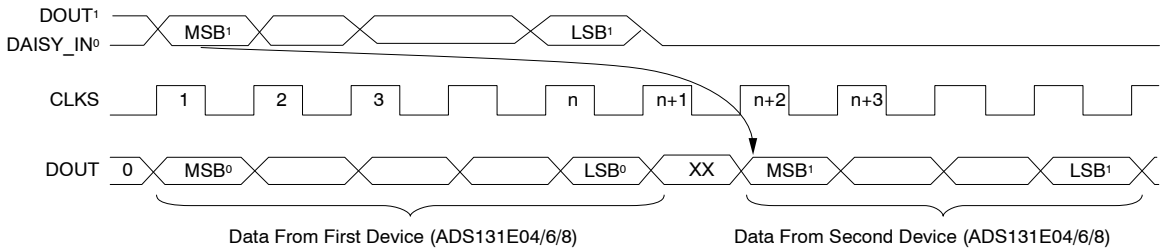
Note that from Figure 2, the SCLK rising edge shifts data out of the ADS131E0x on DOUT. The SCLK rising edge is also used to latch data into the device DAISY_IN pin down the chain. This architecture allows for a faster SCLK rate speed, but it also makes the interface sensitive to board-level signal delays. The more devices in the chain, the more challenging it could become to adhere to setup and hold times. A star-pattern connection of SCLK to all devices, minimizing length of DOUT, and other printed circuit board (PCB) layout techniques helps. Placing delay circuits (such as buffers) between DOUT and DAISY_IN also helps mitigate this challenge. One other option is to insert a *D* flip-flop between DOUT and DAISY_IN clocked on an inverted SCLK. Also note that daisy-chain mode requires some software overhead to recombine data bits spread across byte boundaries. Figure 37 shows a timing diagram for daisy-chain mode.



NOTE: n = (number of channels) × (resolution) + 24 bits. The number of channels is 4, 6, or 8. Resolution is 16-bit or 24-bit.

Figure 37. Daisy-Chain Timing

The maximum number of devices that can be daisy-chained depends on the data rate at which the device is operated at. The maximum number of devices can be approximately calculated with Equation 7.

$$N_{DEVICES} = \frac{f_{SCLK}}{f_{DR}\,(N_{BITS})(N_{CHANNELS}) + 24}$$

where:

N_{BITS} = device resolution (depends on RDR[1:0] setting),
and $N_{CHANNELS}$ = number of channels in the device (4, 6, or 8). (7)

For example, when the ADS131E08 (eight-channel version) is operated at a 24-bit, 8-kSPS data rate with f_{SCLK} = 10 MHz, up to six devices can be daisy-chained together.

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SPI COMMAND DEFINITIONS

The ADS131E0x provide flexible configuration control. The opcode commands, summarized in Table 9, control and configure device operation. The opcode commands are stand-alone, except for the register read and register write operations that require a second command byte plus data. $\overline{CS}$ can be taken high or held low between opcode commands but must stay low for the entire command operation (especially for multibyte commands). System opcode commands and the RDATA command are decoded by the ADS131E0x on the seventh SCLK falling edge. The register read and write opcodes are decoded on the eighth SCLK falling edge. Be sure to follow SPI timing requirements when pulling $\overline{CS}$ high after issuing a command.

Table 9. Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
System Commands			
WAKEUP	Wake-up from standby mode	0000 0010 (02h)	
STANDBY	Enter standby mode	0000 0100 (04h)	
$\overline{RESET}$	Reset the device	0000 0110 (06h)	
START	Start or restart (synchronize) conversions	0000 1000 (08h)	
STOP	Stop conversion	0000 1010 (0Ah)	
OFFSETCAL	Channel offset calibration	0001 1010 (1Ah)	
Data Read Commands			
RDATAC	Enable Read Data Continuous mode. This mode is the default mode at power-up.(1)	0001 0000 (10h)	
SDATAC	Stop Read Data Continuously mode	0001 0001 (11h)	
RDATA	Read data by command; supports multiple read back.	0001 0010 (12h)	
Register Read Commands			
RREG	Read *n nnnn* registers starting at address *r rrrr*	001*r rrrr* (2xh)(2)	000*n nnnn*(2)
WREG	Write *n nnnn* registers starting at address *r rrrr*	010*r rrrr* (4xh)(2)	000*n nnnn*(2)

(1) When in RDATAC mode, the RREG command is ignored.
(2) *n nnnn* = number of registers to be read or written – 1. For example, to read or write three registers, set *n nnnn* = 0 (0010). *r rrrr* = starting register address for read and write opcodes.

WAKEUP: Exit STANDBY Mode

This opcode exits low-power standby mode; see the *STANDBY: Enter STANDBY Mode* subsection of the *SPI Command Definitions* section. Be sure to allow enough time for all circuits in shutdown mode to power up (see the Electrical Characteristics for details). **There are no SCLK rate restrictions for this command and it can be issued at any time.** Any following command must be sent after 4 t_{CLK} cycles.

STANDBY: Enter STANDBY Mode

This opcode command enters low-power standby mode. All parts of the circuit are shut down except for the reference section. The standby mode power consumption is specified in the Electrical Characteristics. **There are no SCLK rate restrictions for this command and it can be issued at any time.** Do not send any other command other than the wakeup command after the device enters standby mode.

$\overline{RESET}$: Reset Registers to Default Values

This command resets the digital filter cycle and returns all register settings to default values. See the *Reset (RESET)* subsection of the *SPI Interface* section for more details. **There are no SCLK rate restrictions for this command and it can be issued at any time.** It takes 18 t_{CLK} cycles to execute the $\overline{RESET}$ command. Avoid sending any commands during this time.

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START: Start Conversions

This opcode starts data conversions. Tie the START pin low to control conversions by command. If conversions are in progress, this command has no effect. The STOP opcode command is used to stop conversions. If the START command is immediately followed by a STOP command, then have a gap of 4 t_{CLK} cycles between them. When the START opcode is sent to the device, keep the START pin low until the STOP command is issued. (See the *START* subsection of the *SPI Interface* section for more details.) **There are no SCLK rate restrictions for this command and it can be issued at any time.**

STOP: Stop Conversions

This opcode stops conversions. Tie the START pin low to control conversions by command. When the STOP command is sent, the conversion in progress completes and further conversions are stopped. If conversions are already stopped, this command has no effect. **There are no SCLK rate restrictions for this command and it can be issued at any time.**

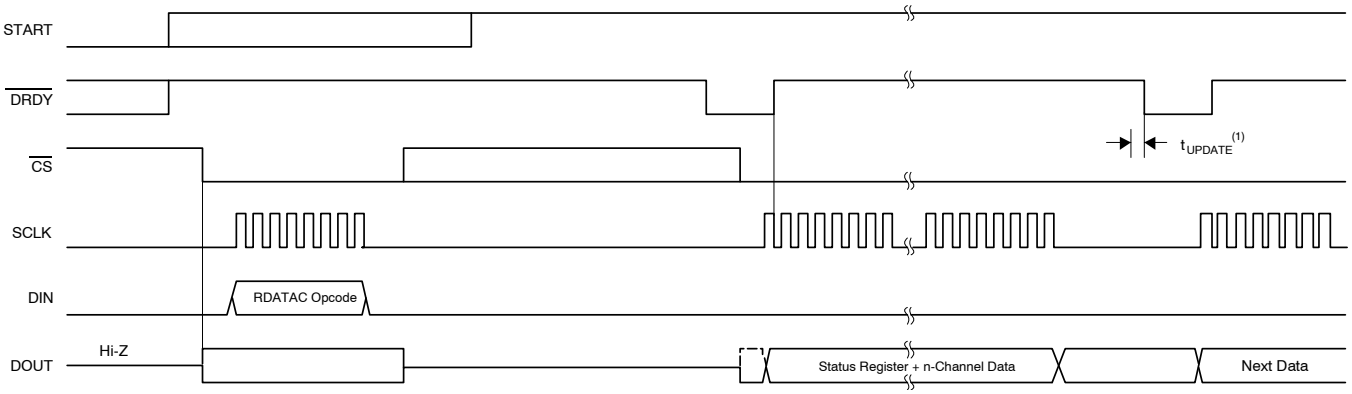
OFFSETCAL: Channel Offset Calibration

This command is used to cancel the channel offset. OFFSETCAL must be executed every time there is a change in PGA gain settings.

RDATAC: Read Data Continuous

This opcode enables the conversion data output on each $\overline{\text{DRDY}}$ without the need to issue subsequent read data opcodes. This mode places the conversion data in the output register and may be shifted out directly. The read data continuous mode is the default mode of the device and the device defaults in this mode on power-up.

RDATAC mode is cancelled by the Stop Read Data Continuous command. If the device is in RDATAC mode, an SDATAC command must be issued before any other commands can be sent to the device. **There are no SCLK rate restrictions for this command.** However, subsequent data retrieval SCLKs or the SDATAC opcode command should wait at least 4 t_{CLK} cycles for the command to execute. RDATAC timing is shown in Figure 38. As Figure 38 shows, there is a *keep out* zone of 4 t_{CLK} cycles around the $\overline{\text{DRDY}}$ pulse where this command cannot be issued in. If no data are retrieved from the device, DOUT and $\overline{\text{DRDY}}$ behave similarly in this mode. To retrieve data from the device after the RDATAC command is issued, make sure either the START pin is high or the START command is issued. Figure 38 shows the recommended way to use the RDATAC command. RDATAC is ideally-suited for applications such as data loggers or recorders where registers are set once and do not need to be reconfigured.



(1) $t_{UPDATE} = 4 / f_{CLK}$. Do not read data during this time.

Figure 38. RDATAC Usage

SDATAC: Stop Read Data Continuous

This opcode cancels the Read Data Continuous mode. There are no SCLK rate restrictions for this command, but the following command must wait for 4 t_{CLK} cycles to execute.

RDATA: Read Data

Issue this command after $\overline{DRDY}$ goes low to read the conversion result (in Stop Read Data Continuous mode). There are no SCLK rate restrictions for this command, and there is no wait time needed for subsequent commands or data retrieval SCLKs. To retrieve data from the device after the RDATA command is issued, make sure either the START pin is high or the START command is issued. When reading data with the RDATA command, the read operation can overlap the next $\overline{DRDY}$ occurrence without data corruption. Figure 39 shows the recommended way to use the RDATA command. RDATA is best suited for systems where register settings must be read or changed often between conversion cycles.

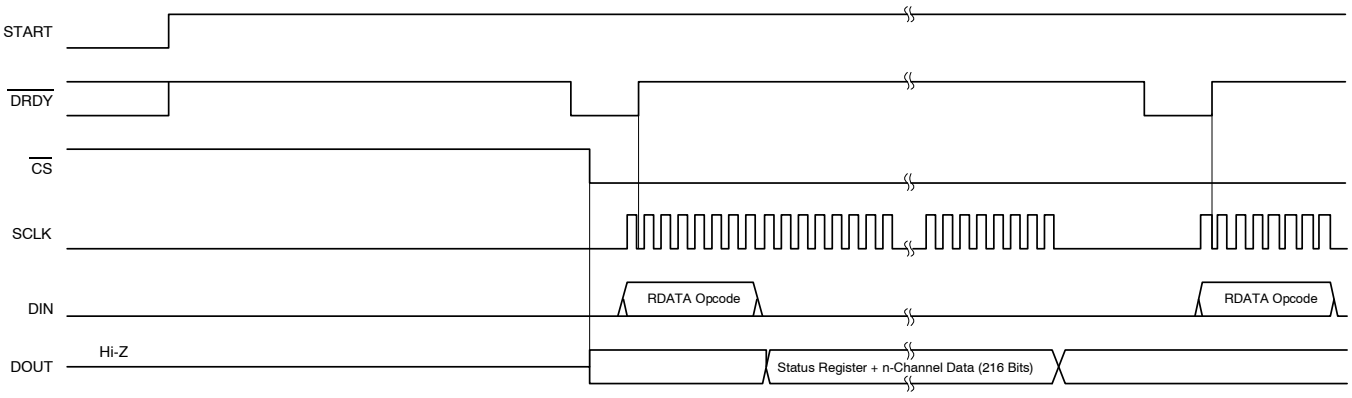


Figure 39. RDATA Usage

Sending Multibyte Commands

The ADS131E0x serial interface decodes commands in bytes and requires 4 t_{CLK} cycles to decode and execute. Therefore, when sending multibyte commands, a 4-t_{CLK} period must separate the end of one byte (or opcode) and the next.

Assuming SCLK is 2.048 MHz, then $t_{SDECODE}$ (4 t_{CLK}) is 1.96 µs. When SCLK is 16 MHz, one byte can be transferred in 500 ns. This byte transfer time does not meet the $t_{SDECODE}$ specification; therefore, a delay must be inserted so the end of the second byte arrives 1.46 µs later. If SCLK is 4 MHz, one byte is transferred in 2 µs. Because this transfer time exceeds the $t_{SDECODE}$ specification, the processor can send subsequent bytes without delay. In this later scenario, the serial port can be programmed to move from single-byte transfers per cycle to multiple bytes.

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RREG: Read From Register

This opcode reads register data. The Register Read command is a two-byte opcode followed by the register data output. The first byte contains the command opcode and the register address. The second opcode byte specifies the number of registers to read – 1.

First opcode byte: 001*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte: 000*n nnnn*, where *n nnnn* is the number of registers to read – 1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in Figure 40. When the device is in read data continuous mode, an SDATAC command must be issued before the RREG command can be issued. The RREG command can be issued at any time. However, because this command is a multibyte command, there are SCLK rate restrictions depending on how the SCLKs are issued. See the *Serial Clock (SCLK)* subsection of the *SPI Interface* section for more details. Note that $\overline{CS}$ must be low for the entire command.

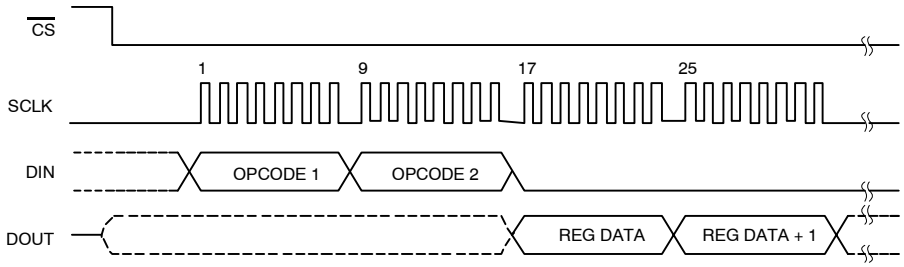

Figure 40. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

WREG: Write to Register

This opcode writes register data. The Register Write command is a two-byte opcode followed by the register data input. The first byte contains the command opcode and the register address.

The second opcode byte specifies the number of registers to write – 1.

First opcode byte: 010*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte: 000*n nnnn*, where *n nnnn* is the number of registers to write – 1.

After the opcode bytes, the register data follows (in MSB-first format), as shown in Figure 41. The WREG command can be issued at any time. However, because this command is a multibyte command, there are SCLK rate restrictions depending on how the SCLKs are issued. See the *Serial Clock (SCLK)* subsection of the *SPI Interface* section for more details. Note that $\overline{CS}$ must be low for the entire command.

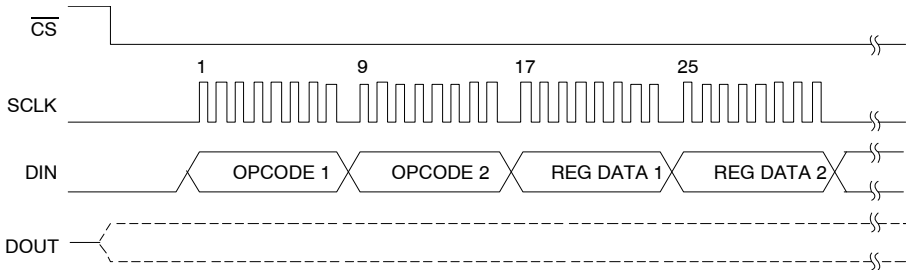

Figure 41. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (OPCODE 1 = 0100 0000, OPCODE 2 = 0000 0001)

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REGISTER MAP

Table 10 describes the various ADS131E0x registers.

Table 10. Register Assignments(1)

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device Settings (Read-Only Registers)										
00h	ID	xx	REV_ID2	REV_ID1	REV_ID0	1	0	0	NU_CH2	NU_CH1
Global Settings Across Channels										
01h	CONFIG1	91	1	DAISY_IN	CLK_EN	1	0	DR2	DR1	DR0
02h	CONFIG2	E0	1	1	1	INT_TEST	0	TEST_AMP0	TEST_FREQ1	TEST_FREQ0
03h	CONFIG3	40	PDB_REFBUF	1	VREF_4V	0	OPAMP_REF	PDB_OPAMP	0	0
04h	FAULT	00	COMP_TH2	COMP_TH1	COMP_TH0	0	0	0	0	0
Channel-Specific Settings										
05h	CH1SET	10	PD1	GAIN12	GAIN11	GAIN10	0	MUX12	MUX11	MUX10
06h	CH2SET	10	PD2	GAIN22	GAIN21	GAIN20	0	MUX22	MUX21	MUX20
07h	CH3SET	10	PD3	GAIN32	GAIN31	GAIN30	0	MUX32	MUX31	MUX30
08h	CH4SET	10	PD4	GAIN42	GAIN41	GAIN40	0	MUX42	MUX41	MUX40
09h	CH5SET	10	PD5	GAIN52	GAIN51	GAIN50	0	MUX52	MUX51	MUX50
0Ah	CH6SET	10	PD6	GAIN62	GAIN61	GAIN60	0	MUX62	MUX61	MUX60
0Bh	CH7SET	10	PD7	GAIN72	GAIN71	GAIN70	0	MUX72	MUX71	MUX70
0Ch	CH8SET	10	PD8	GAIN82	GAIN81	GAIN80	0	MUX82	MUX81	MUX80
Fault Detect Status Registers (Read-Only Registers)										
12h	FAULT_STATP	00	IN8P_FAULT	IN7P_FAULT	IN6P_FAULT	IN5P_FAULT	IN4P_FAULT	IN3P_FAULT	IN2P_FAULT	IN1P_FAULT
13h	FAULT_STATN	00	IN8N_FAULT	IN7N_FAULT	IN6N_FAULT	IN5N_FAULT	IN4N_FAULT	IN3N_FAULT	IN2N_FAULT	IN1N_FAULT
GPIO and Other Registers										
14h	GPIO	0F	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1

(1) Registers 0Dh, 0Eh, 0Fh, 10h, and 11h must be written to all 0's.

User Register Description

ID: ID Control Register (Factory-Programmed, Read-Only)

Address = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REV_ID2	REV_ID1	REV_ID0	1	0	0	NU_CH2	NU_CH1

This register is programmed during device manufacture to indicate device characteristics.

Bits[7:5] **REV_ID[2:0]: Device family identification**

These bits indicate the device family.

000, 001, 010, 011, 100, 101 = Reserved
110 = ADS131E08
111 = Reserved

Bit 4 **Must be set to '1'**

This bit reads high.

Bits[3:2] **Must be set to '0'**

These bits read low.

Bits[1:0] **NU_CH[2:1]: Factory-programmed device identification bits (read-only)**

These bits indicate the device version.

00 = 4-channel device
01 = 6-channel device
10 = 8-channel device
11 = Reserved

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CONFIG1: Configuration Register 1

Address = 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	DAISY_IN	CLK_EN	1	0	DR2	DR1	DR0

This register configures each ADC channel sample rate.

Bit 7 **Must be set to '1'**

Bit 6 **DAISY_IN: Daisy-chain and multiple read-back mode**

This bit determines which mode is enabled.

0 = Daisy-chain mode (default)
1 = Multiple read-back mode

Bit 5 **CLK_EN: CLK connection(1)**

This bit determines if the internal oscillator signal is connected to the CLK pin when the CLKSEL pin = 1.

0 = Oscillator clock output disabled (default)
1 = Oscillator clock output enabled

Bit 4 **Must be set to '1'**

Bit 3 **Must be set to '0'**

Bits[2:0] **DR[2:0]: Output data rate**

These bits determine the output data rate and resolution. See Table 11 for details.
Modulator clock $f_{MOD} = f_{CLK} / 2$. Where $f_{MOD} = 1.024$ MHz.

(1) Additional power is consumed when driving external devices.

Table 11. Data Rate Settings

DR{2:0]	RESOLUTION	DATA RATE (kSPS)
000	16-bit output	64
001	16-bit output	32 (default)
010	24-bit output	16
011	24-bit output	8
100	24-bit output	4
101	24-bit output	2
110	24-bit output	1
111	Do not use	NA

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CONFIG2: Configuration Register 2

Address = 02h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	1	1	INT_TEST	0	TEST_AMP0	TEST_FREQ1	TEST_FREQ0

This register configures the test signal generation. See the *Input Multiplexer* section for more details.

Bits[7:5] **Must be set to '1'**

Bit 4 **INT_TEST: Test source**

This bit determines the source for the Test signal.

0 = Test signals are driven externally (default)
1 = Test signals are generated internally

Bit 3 **Must be set to '0'**

Bit 2 **TEST_AMP: Test signal amplitude**

These bits determine the Calibration signal amplitude.

0 = 1 × –(VREFP – VREFN) / 2.4 mV (default)
1 = 2 × –(VREFP – VREFN) / 2.4 mV

Bits[1:0] **TEST_FREQ[1:0]: Test signal frequency**

These bits determine the calibration signal frequency.

00 = Pulsed at $f_{CLK} / 2^{21}$ (default)
01 = Pulsed at $f_{CLK} / 2^{20}$
10 = Not used
11 = At dc

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CONFIG3: Configuration Register 3

Address = 03h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PDB_REFBUF	1	VREF_4V	0	OPAMP_REF	PDB_OPAMP	0	0

This register configures the multireference operation.

Bit 7 **PDB_REFBUF: Power-down reference buffer**

This bit determines the power-down reference buffer state.

0 = Power-down internal reference buffer (default)
1 = Enable internal reference buffer

Bit 6 **Must be set to '1'**

Default is '1' at power-up.

Bit 5 **VREF_4V: Reference voltage**

This bit determines the reference voltage, VREFP.

0 = VREFP is set to 2.4 V (default)
1 = VREFP is set to 4 V (use only with a 5-V analog supply)

Bit 4 **Must be set to '0'**

Bit 3 **OPAMP_REF: Op amp reference**

This bit determines whether the op amp noninverting input connects to the OPAMPP pin or to the internally-derived 1/2 supply (AVDD + AVSS) / 2.

0 = Noninverting input connected to the OPAMPP pin (default)
1 = Noninverting input connected to (AVDD + AVSS) / 2

Bit 2 **PDB_OPAMP: Op amp power down**

This bit determines the power-down reference buffer state.

0 = Power-down op amp (default)
1 = Enable op amp

Bits[1:0] **Must be set to '0'**

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FAULT: Fault Detect Control Register

Address = 04h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMP_TH2	COMP_TH1	COMP_TH0	0	0	0	0	0

This register configures the fault detection operation.

Bits[7:5] **COMP_TH[2:0]: Fault detect comparator threshold**

These bits determine the fault detect comparator threshold level setting. See the *Fault Detection* section for a detailed description.

Comparator high-side threshold

000 = 95% (default)
001 = 92.5%
010 = 90%
011 = 87.5%
100 = 85%
101 = 80%
110 = 75%
111 = 70%

Comparator low-side threshold

000 = 5% (default)
001 = 7.5%
010 = 10%
011 = 12.5%
100 = 15%
101 = 20%
110 = 25%
111 = 30%

Bits[4:0] **Must be set to '0'**

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CHnSET: Individual Channel Settings (n = 1 to 8)

Address = 05h to 0Ch

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PDn	GAINn2	GAINn1	GAINn0	0	MUXn2	MUXn1	MUXn0

This register configures the power mode, PGA gain, and multiplexer settings channels. See the *Input Multiplexer* section for details. CH[2:8]SET are similar to CH1SET, corresponding to the respective channels (refer to Table 10).

Bit 7 **PDn: Power-down (n = individual channel number)**

This bit determines the channel power mode for the corresponding channel.

0 = Normal operation (default)
1 = Channel power-down

Bits[6:4] **GAINn[2:0]: PGA gain (n = individual channel number)**

These bits determine the PGA gain setting.

000 = Do not use
001 = 1 (default)
010 = 2
011 = Do not use
100 = 4
101 = 8
110 = 12
111 = Do not use

Bit 3 **Must be set to '0'**

Bits[2:0] **MUXn[2:0]: Channel input (n = individual channel number)**

These bits determine the channel input selection.

000 = Normal input (default)
001 = Input shorted (for offset or noise measurements)
010 = Do not use
011 = MVDD for supply measurement
100 = Temperature sensor
101 = Test signal
110 = Do not use
111 = Do not use

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FAULT_STATP: Fault Detect Positive Input Status

Address = 12h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IN8P_FAULT	IN7P_FAULT	IN6P_FAULT	IN5P_FAULT	IN4P_FAULT	IN3P_FAULT	IN2P_FAULT	IN1P_FAULT

This register stores the status of whether the positive input on each channel has a fault or not. See the *Fault Detection* section for details. Ignore the FAULT_STATP values if the corresponding FAULT_SENSP bits are not set to '1'.

FAULT_STATN: Fault Detect Negative Input Status

Address = 13h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IN8N_FAULT	IN7N_FAULT	IN6N_FAULT	IN5N_FAULT	IN4N_FAULT	IN3N_FAULT	IN2N_FAULT	IN1N_FAULT

This register stores the status of whether the negative input on each channel has a fault or not. See the *Fault Detection* section for details. Ignore the FAULT_STATN values if the corresponding FAULT_SENSN bits are not set to '1'.

GPIO: General-Purpose IO Register

Address = 14h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1

This register controls the action of the three GPIO pins.

Bits[7:4] **GPIOD[4:1]: GPIO data**

These bits are used to read and write data to the GPIO ports.
When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect.

Bits[1:0] **GPIOC[4:1]: GPIO control (corresponding to GPIOD)**

These bits determine if the corresponding GPIOD pin is an input or output.

0 = Output
1 = Input (default)

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POWER MONITORING SPECIFIC APPLICATIONS

All channels of the ADS131E0x family of devices are exactly identical, yet independently configurable, thus giving the user the flexibility of selecting any channel for voltage or current monitoring. An overview of this system is illustrated in Figure 42. Also, the simultaneously sampling capability of the device allows the user to monitor both the current and the voltage at the same time. The full-scale differential input voltage of each channel is determined by the PGA gain setting (see the *CHnSET: Individual Channel Settings* section) for the respective channel and V_{REF} (see the *CONFIG3: Configuration Register 3* section). Table 12 summarizes the full-scale differential input voltage range for an internal V_{REF}.

Table 12. Full-Scale Differential Input Voltage Summary

V_{REF}	PGA GAIN	FULL-SCALE DIFFERENTIAL INPUT VOLTAGE, FSDI (V_{PP})	RMS VOLTAGE [= FSDI / ($2\sqrt{2}$)] (V_{RMS})
2.4 V	1	4.8	1.698
	2	2.4	0.849
	4	1.2	0.424
	8	0.6	0.212
	12	0.4	0.141
4.0 V	1	8	2.828
	2	4	1.414
	4	2	0.707
	8	1	0.354
	12	0.66	0.236

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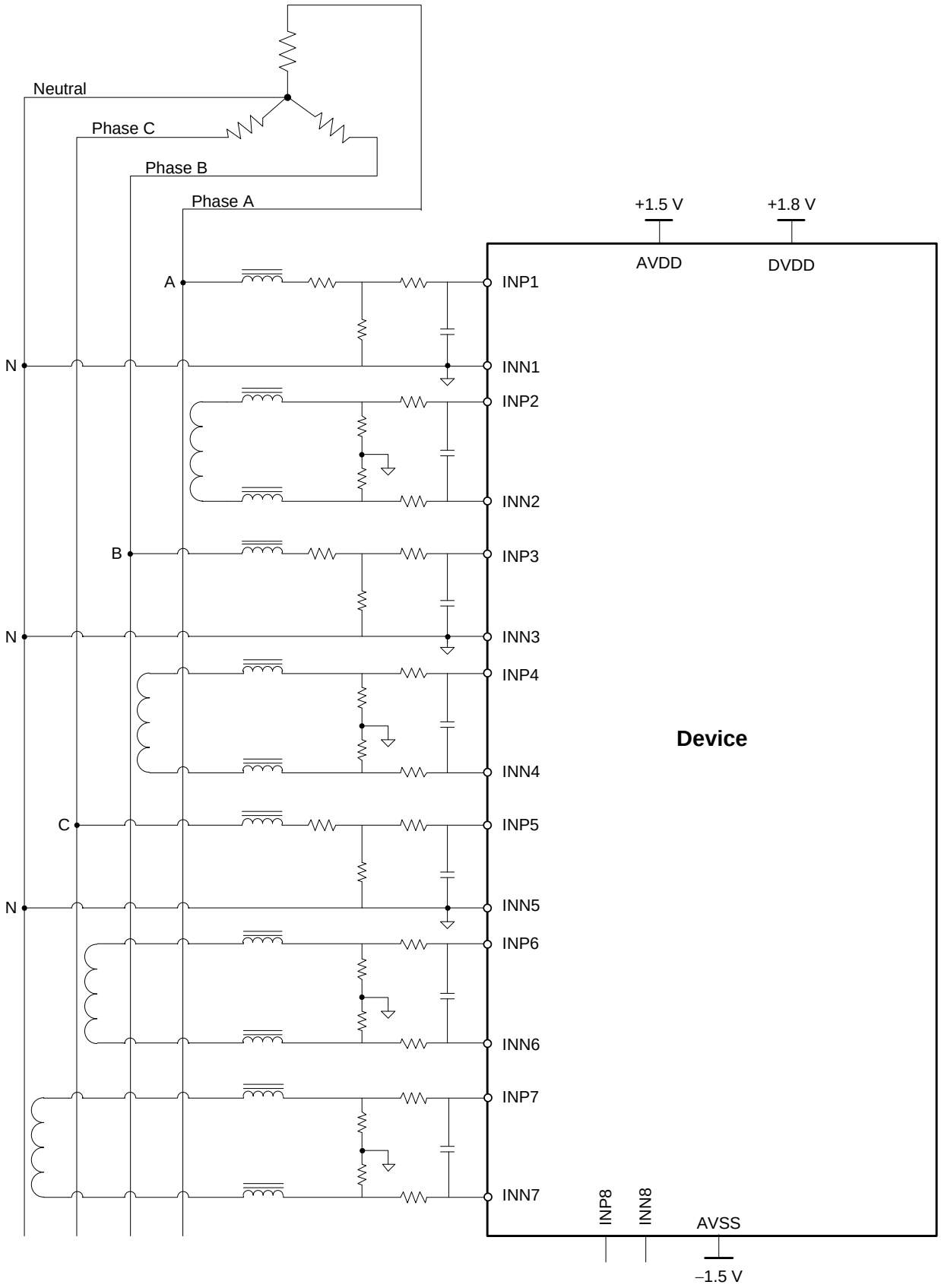

Figure 42. Overview of Power Monitoring System

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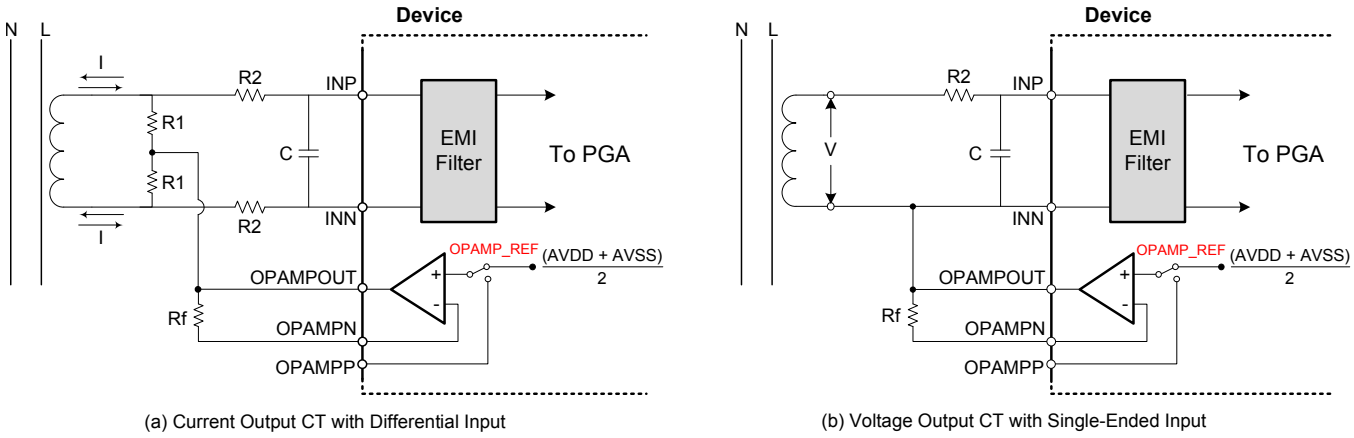
CURRENT SENSING

Figure 43 shows a simplified diagram of typical configurations used for current sensing with a Rogowski coil, current transformer (CT), or an air coil that outputs a current or voltage. In the case of the current output transformers, the burden resistors (R1) are used for current-to-voltage conversion. The output of the burden resistors is connected to the ADS131E0x INP and INN inputs through an antialiasing RC filter for current sensing. In the case of the voltage output transformers (such as certain types of Rogowski coils), the output terminals of the transformers are directly connected to the ADS131E0x INP and INN inputs through an antialiasing RC filter for current sensing. The common-mode bias voltage (AVDD + AVSS) / 2, can be obtained from the ADS131E0x by either configuring the internal op amp in a unity-gain configuration using the R_F resistor and setting bit 3 of the CONFIG3 register, or it can be generated externally with a simple resistor divider network between the positive and negative supplies.

The value of resistor R1 for the current output transformer and turns ratio of the transformer should be selected so as not to exceed the ADS131E0x full-scale differential input voltage (FSDI) range. Likewise, the output voltage (V) for the voltage output transformer should be selected to not exceed the FSDI. In addition, the selection of resistor (R) and turns ratio should not saturate the transformer over the full operating dynamic range of the energy meter. Figure 43a shows differential input current sensing and Figure 43b shows single-ended input sensing.



(a) Current Output CT with Differential Input

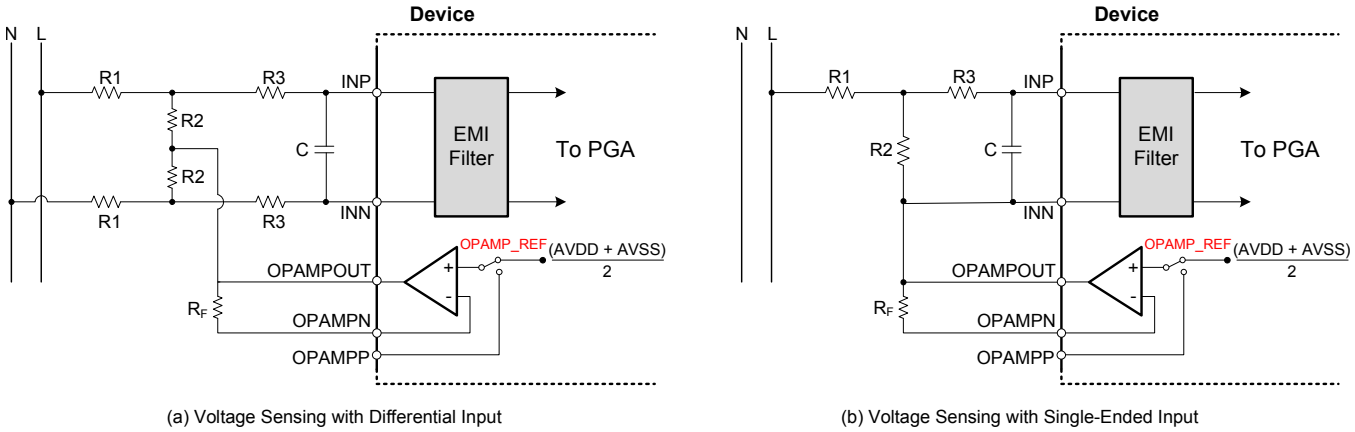
(b) Voltage Output CT with Single-Ended Input

Figure 43. Simplified Current Sensing Connections

VOLTAGE SENSING

Figure 44 shows a simplified diagram of commonly-used differential and single-ended methods of voltage sensing. A resistor divider network is used to step down the line voltage within the acceptable ADS131E0x input range and then directly connect to the inputs (INP and INN) through an antialiasing RC filter formed by resistor R3 and capacitor C. The common-mode bias voltage (AVDD + AVSS) / 2, can be obtained from the ADS131E0x by either configuring the internal op amp in a unity-gain configuration using the R_F resistor and setting bit 3 of the CONFIG3 register, or it can be generated externally by using a simple resistor divider network between the positive and negative supplies.

In either of the below cases (Figure 44a for a differential input and Figure 44b for a single-ended input), the line voltage is divided down by a factor of [R2 / (R1 + R2)]. Values of R1 and R2 must be carefully chosen so that the voltage across the ADS131E0x inputs (INP and INN) does not exceed the FSDI range of ADS131E0x (see Table 12) over the full operating dynamic range of the energy meter.



(a) Voltage Sensing with Differential Input

(b) Voltage Sensing with Single-Ended Input

Figure 44. Simplified Voltage Sensing Connections

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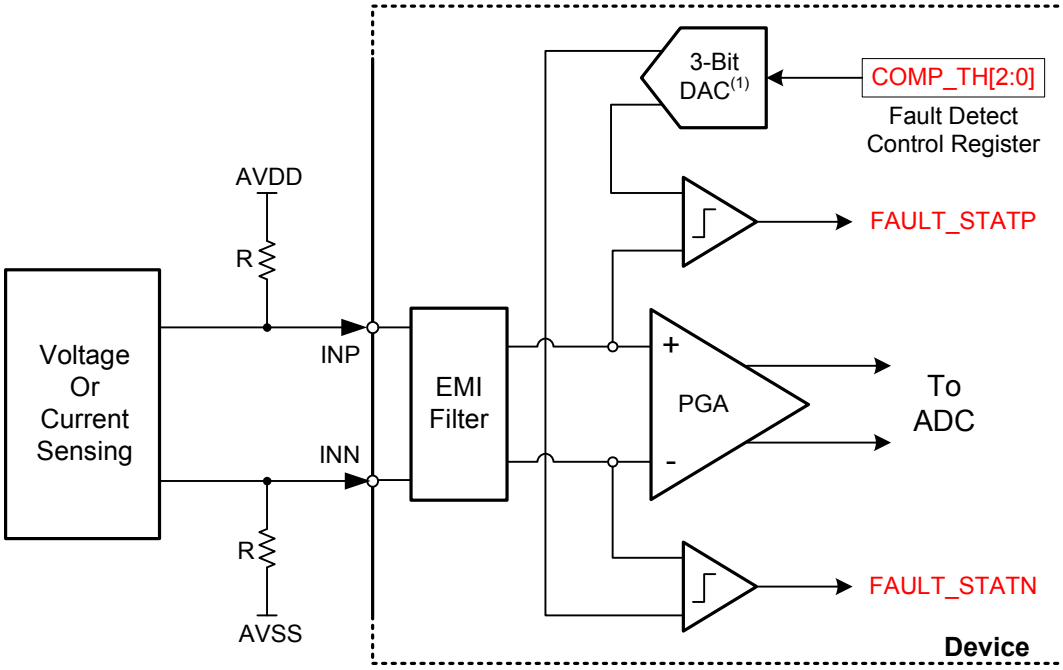
FAULT DETECTION

The ADS131E0x have integrated comparators that can be used in conjunction with the external pull-up or pull-down resistors (R) to detect various fault conditions. The basic principle is to compare the input voltage with the one set by the fault comparator 3-bit digital-to-analog converter (DAC), as shown in Figure 45. The comparator trigger threshold level is set by the COMP_TH[2:0] bits in the FAULT register. Assuming that the ADS131E0x is powered from ±2.5-V supply and COMP_TH[2:0] = 000 (95% and 5%), the high-side trigger threshold is set at +2.25 V [equal to AVSS + (AVDD + AVSS) × 95%] and the low-side threshold is set at –2.25 V [equal to AVSS + (AVDD + AVSS) × 5%]. The threshold calculation formula applies to unipolar as well as bipolar supplies.

A fault condition, such as an input signal going out of a predetermined range, can be detected by setting the appropriate threshold level using the COMP_TH[2:0] bits. An open-circuit fault at the INP or INN pin can be detected by using the external pull-up and pull-down resistors, which rail the corresponding input when the input circuit breaks, causing the fault comparators to trip. To pinpoint which of the inputs is out of range, the status of the FAULT_STATP and FAULT_STATN registers can be read, which is available as part of the output data stream; see the *Data Output (DOUT)* subsection of the *SPI Interface* section.



(1) The configurable 3-bit DAC is common to all channels.

Figure 45. Fault Detect Comparators

QUICK-START GUIDE

PCB LAYOUT

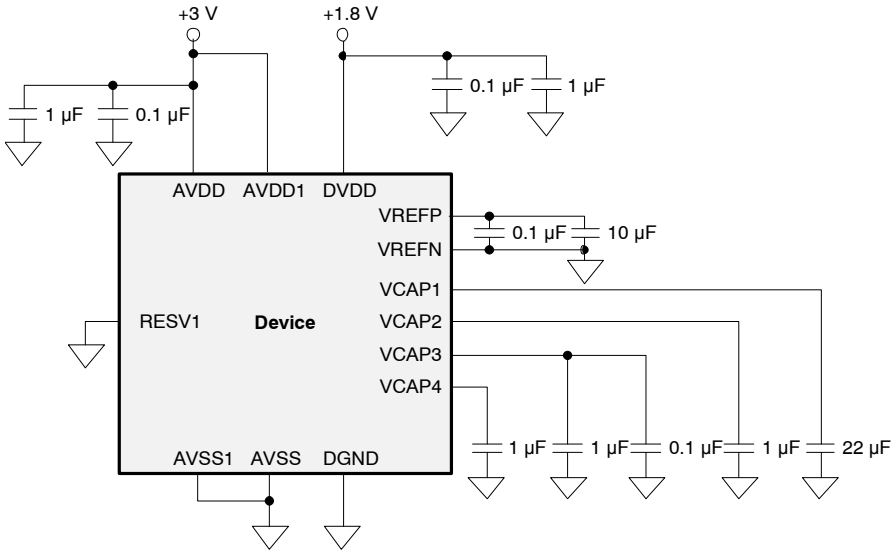
Power Supplies and Grounding

The ADS131E0x have three supplies: AVDD, AVDD1, and DVDD. Both AVDD and AVDD1 should be as quiet as possible. AVDD1 provides the supply to the charge pump block and has transients at f_{CLK}. Therefore, it is recommended that AVDD1 and AVSS1 be star-connected to AVDD and AVSS. It is important to eliminate noise from AVDD and AVDD1 that is non-synchronous with device operation. Each ADS131E0x supply should be bypassed with 10-µF and a 0.1-µF solid ceramic capacitors. It is recommended to place the digital circuits [such as digital signal processors (DSPs), microcontrollers, and field-programmable gate arrays (FPGAs)] in the system such that the return currents on those devices do not cross the ADS131E0x analog return path. The ADS131E0x can be powered from unipolar or bipolar supplies.

The decoupling capacitors can be surface-mount, low-cost, low-profile multi-layer ceramic. In most cases the VCAP1 capacitor can also be a multilayer ceramic. However, in systems where the board is subjected to high- or low-frequency vibration, it is recommend that a non-ferroelectric capacitor (such as a tantalum or class 1 capacitor, C0G or NPO for example) be installed. EIA class 2 and class 3 dielectrics (such as X7R, X5R, and X8R) are ferroelectric. The piezoelectric property of these capacitors can appear as electrical noise coming from the capacitor. When using the internal reference, noise on the VCAP1 node results in performance degradation.

Connecting the Device to Unipolar (+3 V or +1.8 V) Supplies

Figure 46 illustrates the ADS131E0x connected to a unipolar supply. In this example, the analog supply (AVDD) is referenced to analog ground (AVSS) and the digital supplies (DVDD) are referenced to digital ground (DGND).



NOTE: Place the supply, reference, and VCAP1 to VCAP4 capacitors as close to the package as possible.

Figure 46. Single-Supply Operation

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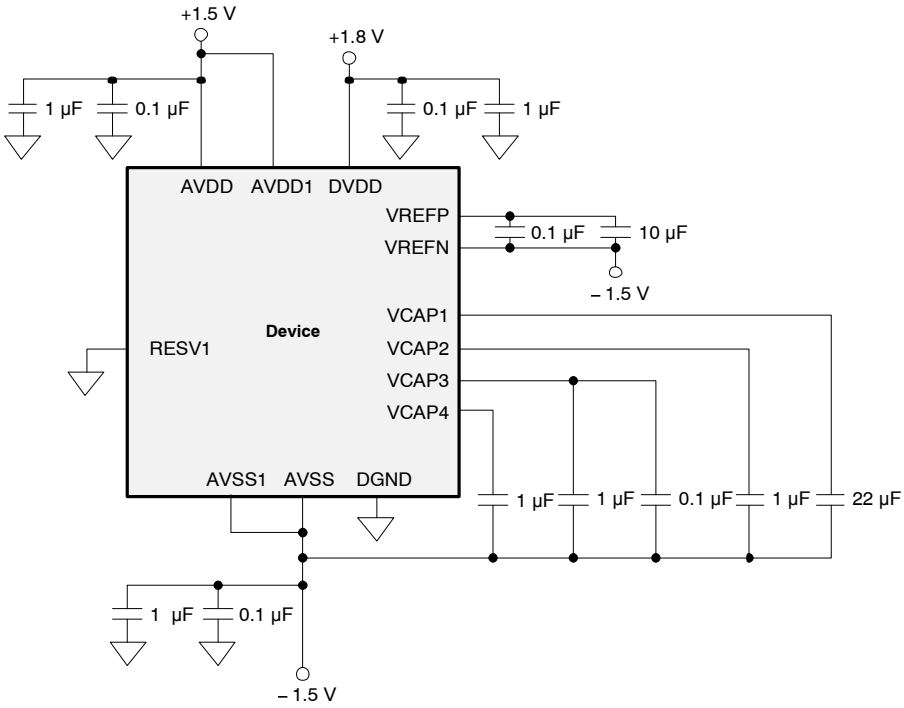
Connecting the Device to Bipolar (±1.5 V or 1.8 V) Supplies

Figure 47 illustrates the ADS131E0x connected to a bipolar supply. In this example, the analog supplies connect to the device analog supply (AVDD). This supply is referenced to the device analog return (AVSS), and the digital supply (DVDD) is referenced to the device digital ground return (DGND).



NOTE: Place the capacitors for supply, reference, and VCAP1 to VCAP4 as close to the package as possible.

Figure 47. Bipolar Supply Operation

Shielding Analog Signal Paths

As with any precision circuit, careful PCB layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins and AVSS. These analog input pins are high-impedance and extremely sensitive to extraneous noise. The AVSS pin should be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the ADS131E0x input bias current if shielding is not implemented. Digital signals should be kept as far as possible from the analog input signals on the PCB.

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POWER-UP SEQUENCING

Before device power-up, all digital and analog inputs must be low. At power-up, these signals should remain low until the power supplies have stabilized, as shown in Figure 48. Once the supply voltages have reached the final value, the digital power-on reset (t_{POR}) executes to set the digital portion of the chip. The reset pin, or reset command, should be issued after t_{POR} and when the VCAP1 voltage is greater than 800 mV. The VCAP1 pin charge time is set by RC time constant; see Figure 27. If the VCAP1 capacitor is 22 µF, a reset can be issued within 400 ms after power up. After releasing RESET, the configuration register must be programmed (see the *CONFIG1: Configuration Register 1* subsection of the *Register Map* section for details). The power-up sequence timing is shown in Table 13.

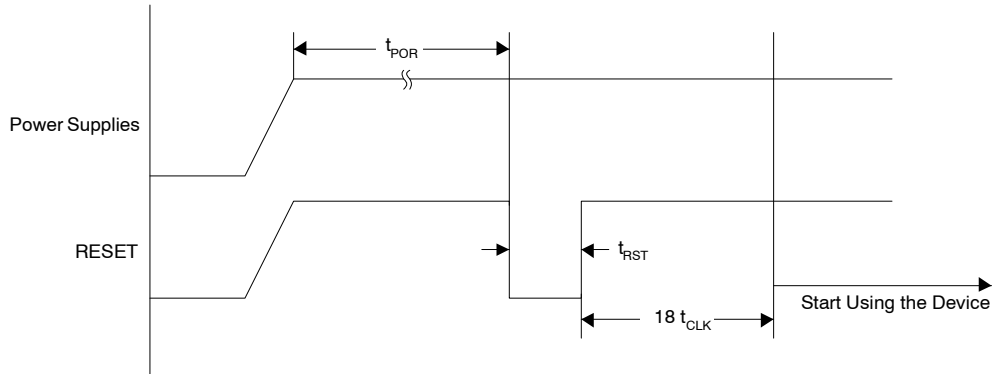

Figure 48. Power-Up Timing Diagram

Table 13. Power-Up Sequence Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{POR}	Wait after power-up until reset	2^{16}			t_{CLK}
t_{RST}	Reset low width	1			t_{CLK}

SETTING THE DEVICE FOR BASIC DATA CAPTURE

This section outlines the procedure to configure the device in a basic state and capture data. This procedure is intended to put the device in a data sheet condition to check if the device is working properly in the user system. It is recommended that this procedure be followed initially to get familiar with the device settings. When this procedure is verified, the device can be configured as needed. For details on the timings for commands refer to the appropriate sections in the data sheet. The flow chart of Figure 49 details the initial ADS131E0x configuration and setup.

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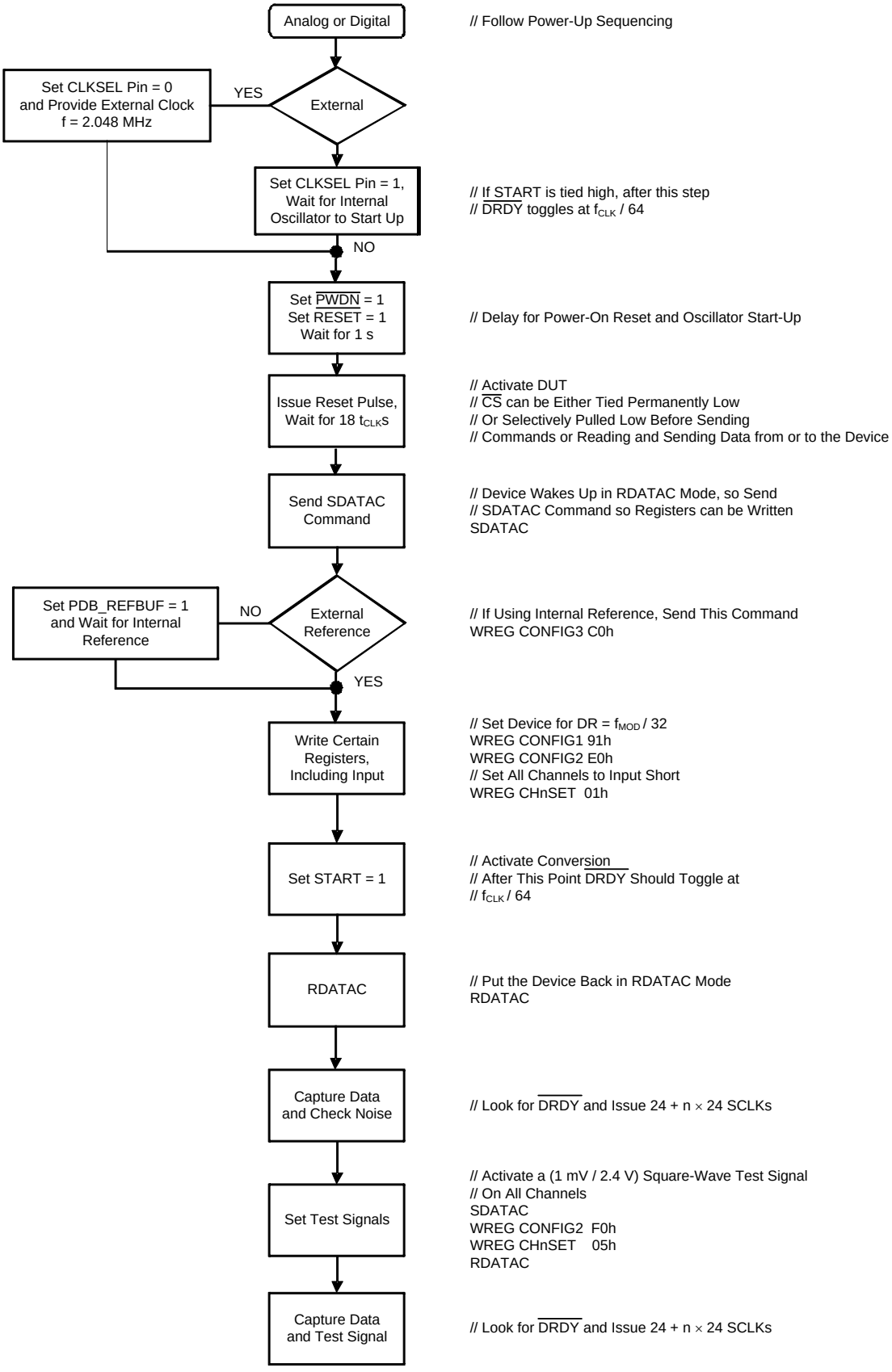

Figure 49. Initial Flow at Power-Up

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS131E04IPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS131E04IPAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS131E06IPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS131E06IPAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS131E08IPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS131E08IPAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
COMBOSMARTMETER	ACTIVE			0		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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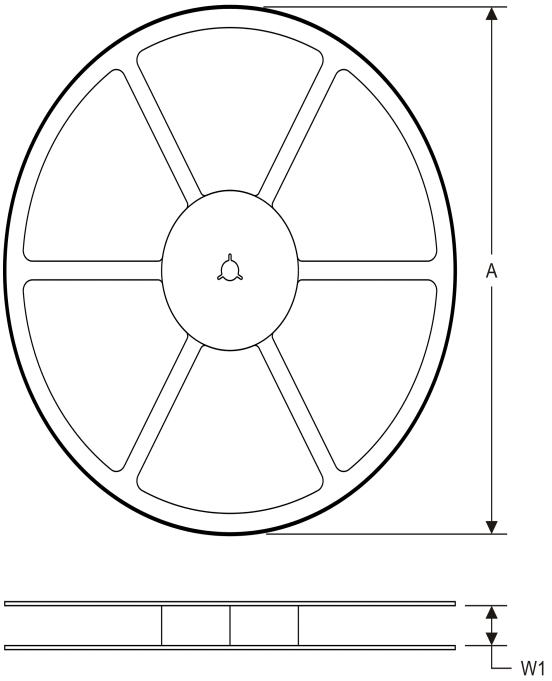
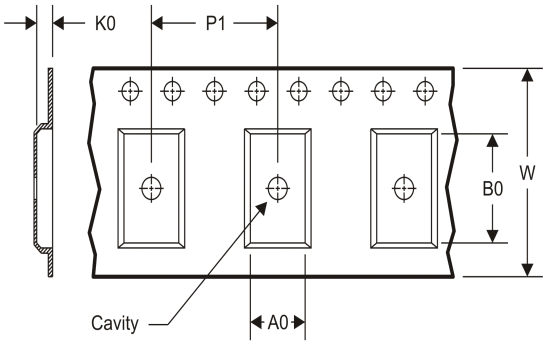
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



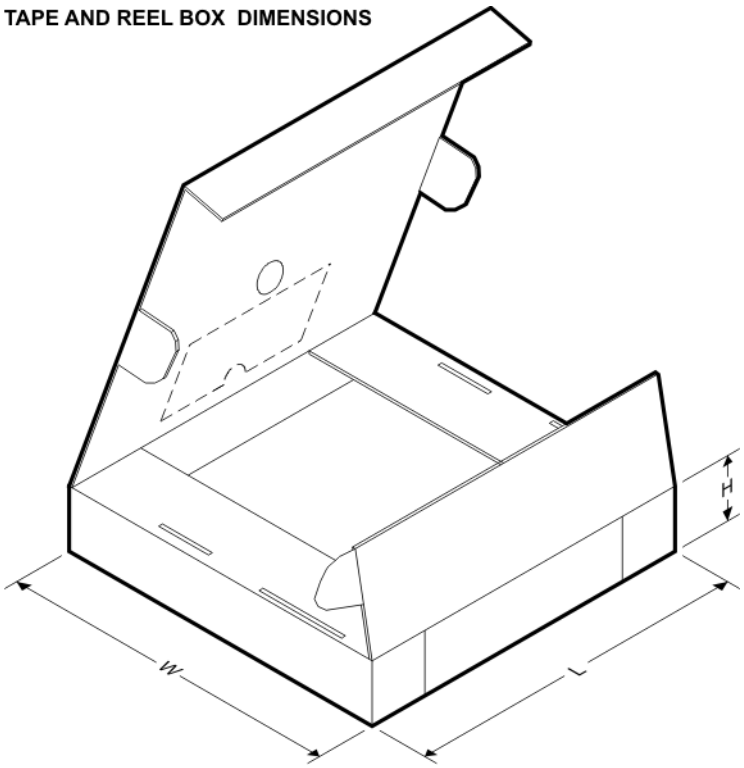
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS131E04IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
ADS131E06IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
ADS131E08IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

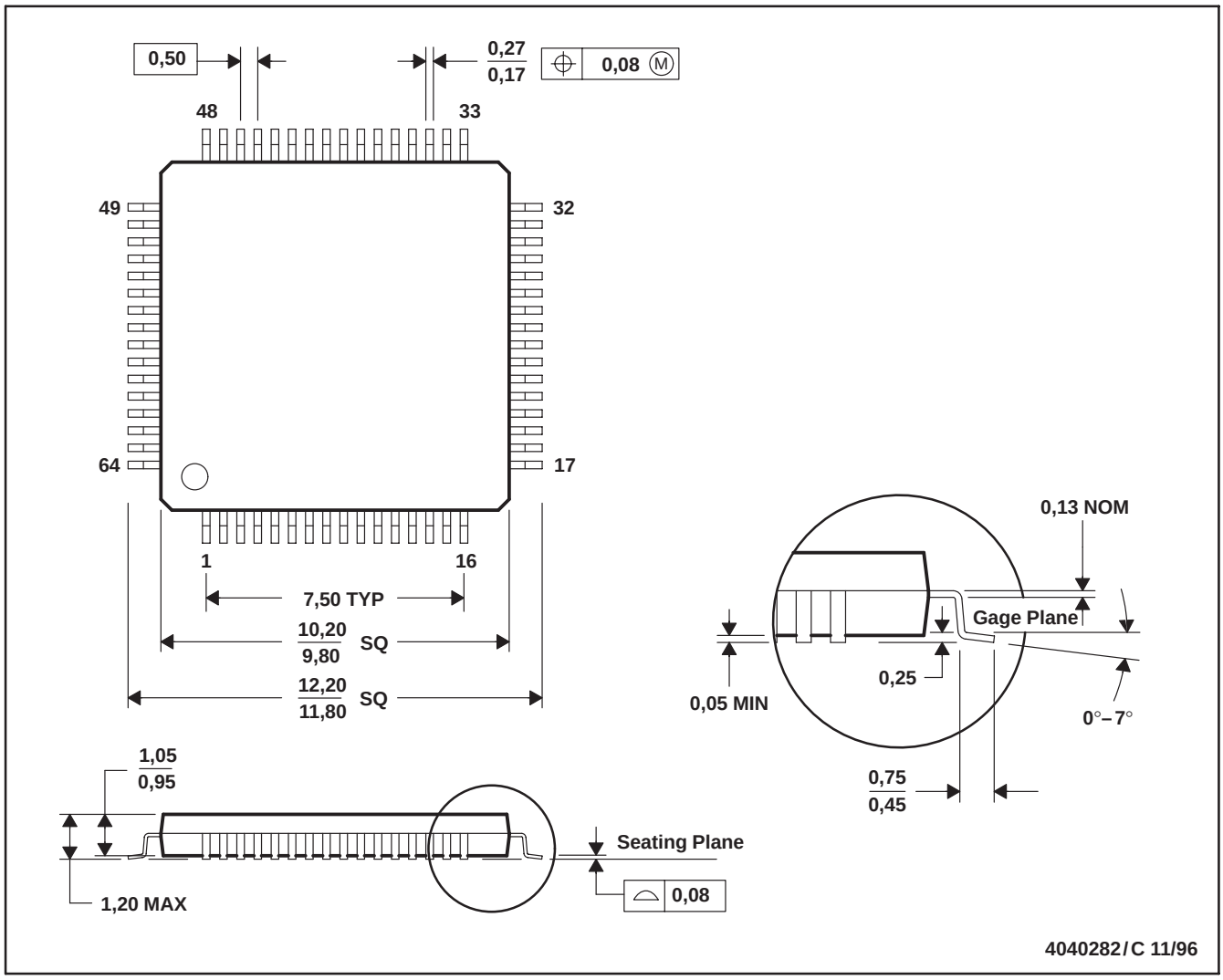
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

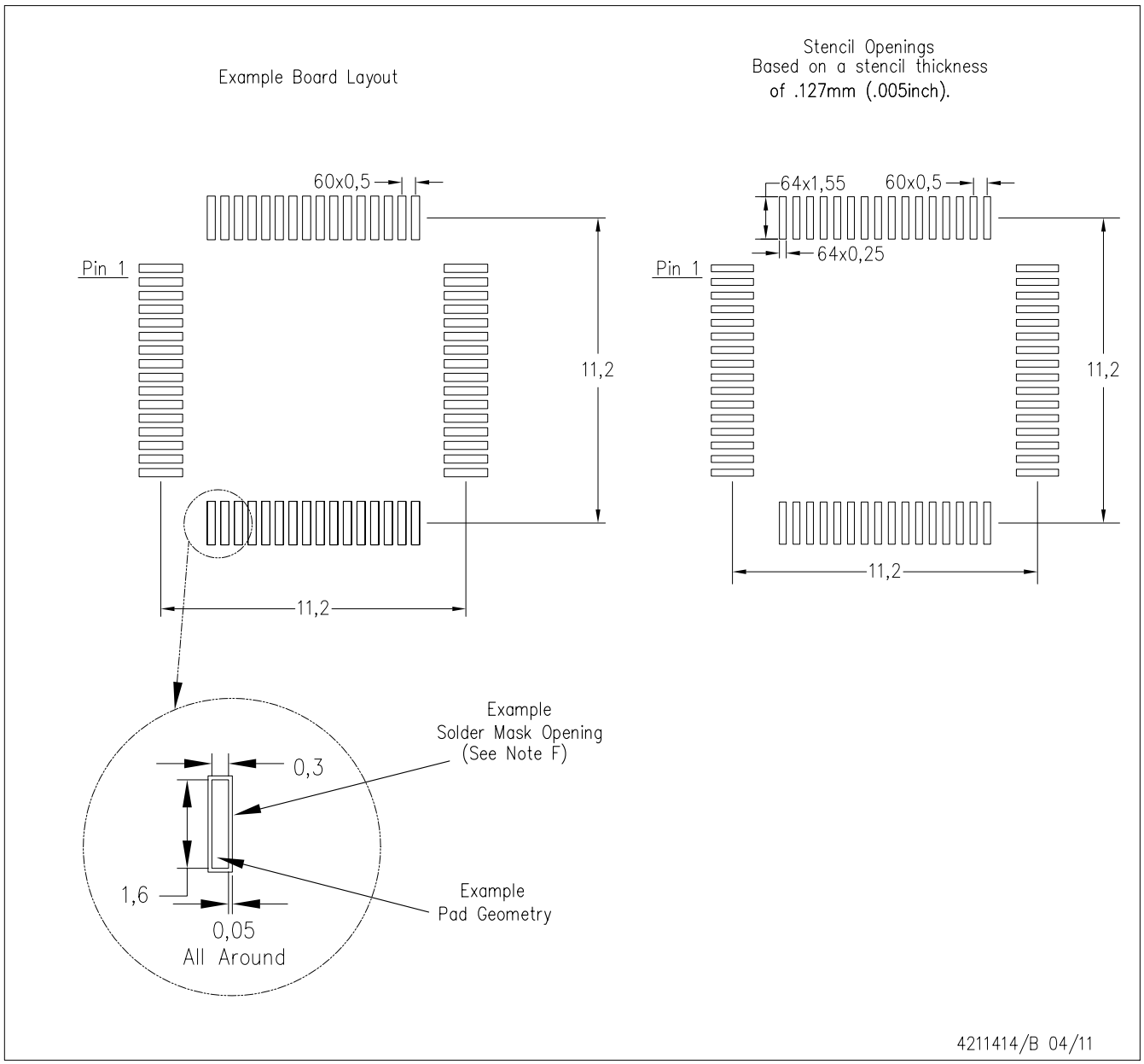
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS131E04IPAGR	TQFP	PAG	64	1500	367.0	367.0	45.0
ADS131E06IPAGR	TQFP	PAG	64	1500	367.0	367.0	45.0
ADS131E08IPAGR	TQFP	PAG	64	1500	367.0	367.0	45.0

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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