REALTEK/AVANCE LOGIC, INC.
TWO CHANNEL AC'97 AUDIO CODEC
ALC101

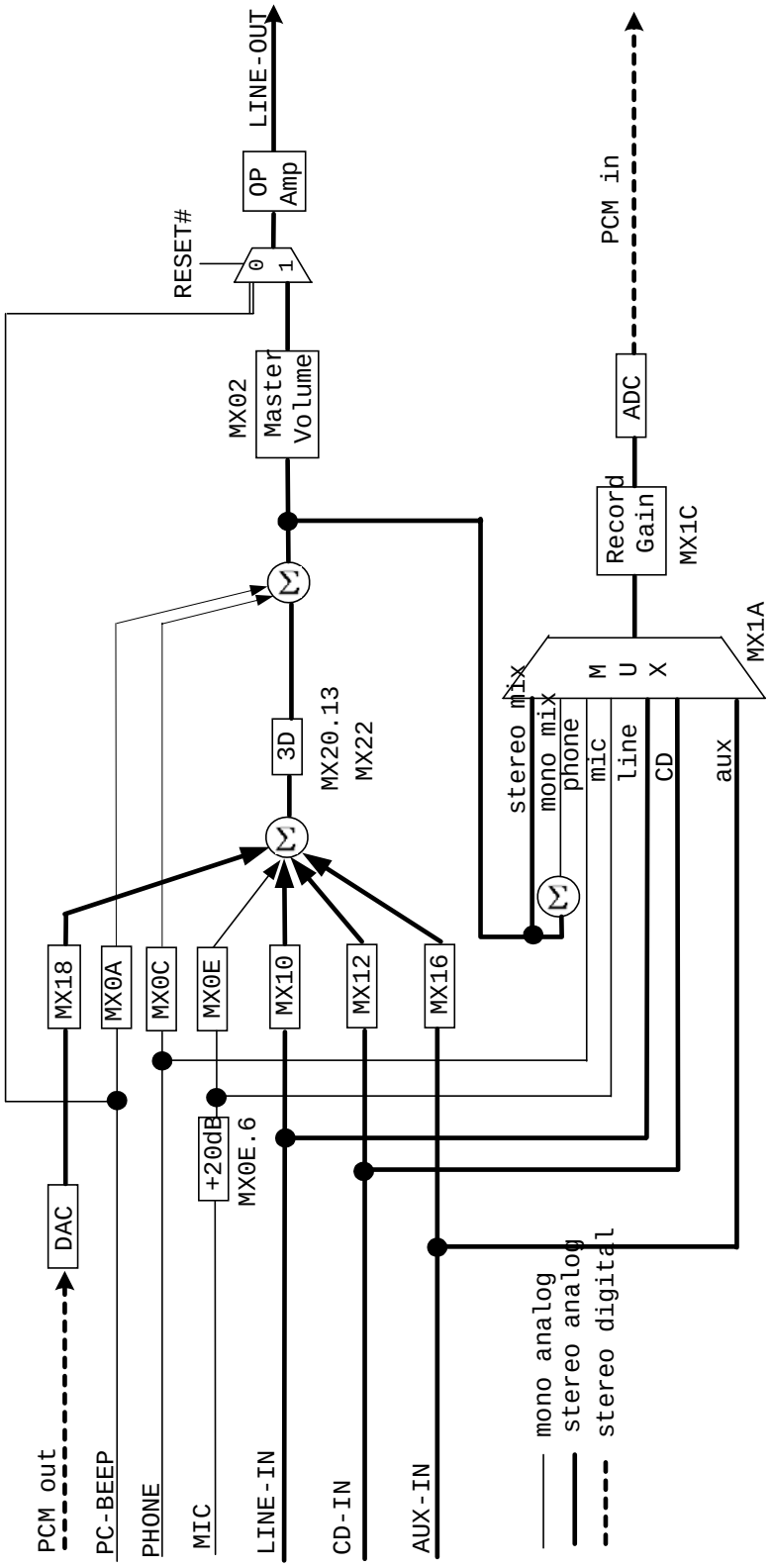
1. Features

- Single chip audio CODEC with high S/N ratio
- Compliant with AC'97 2.2 specification
- 16-bit stereo full-duplex CODEC with fixed 48KHz sampling rate
- 3 analog line-level stereo inputs with 5-bit volume control: LINE-IN, CD-IN, AUX-IN
- 1 analog line-level mono input: PHONE-IN
- 1 MIC input
- Power management
- 3D Stereo Enhancement
- LINE output with 50mW/20Ω headphone driver
- External Amplifier power down capability
- Power supply: Digital: 3.3V Analog: 5V/3.3V
- Clocking by external 14.318MHz or 24.576MHz source to save crystal
- Standard 48-pin LQFP Package and 20-pin SOP

2. General Description

The ALC101 is an 18-bit, full duplex AC'97 2.2 compatible stereo audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC101 AC'97 CODEC supports multiple CODEC extensions with independent variable sampling rates and built-in 3D effects. The ALC101 CODEC provides a pair of stereo outputs with independent volume controls and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC101 CODEC operates from a 5V/3.3V power supply with EAPD (External Amplifier Power Down) control for use in notebook and PC applications. The ALC101 integrates a 50mW/20ohm headset audio amplifier into the CODEC, saving BOM costs. The ALC101 CODEC supports host/soft audio from Intel 810/815/820/845 chipsets as well as audio controller based VIA/SIS/ALI chipsets. Bundled Windows series drivers (Win95/98/ME/2000/XP/NT) and sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation, 5-band equalizer) provide an excellent entertainment package for PC users. Finally, internal PLL circuits generate required timing signals, eliminating the need for external clocking devices.

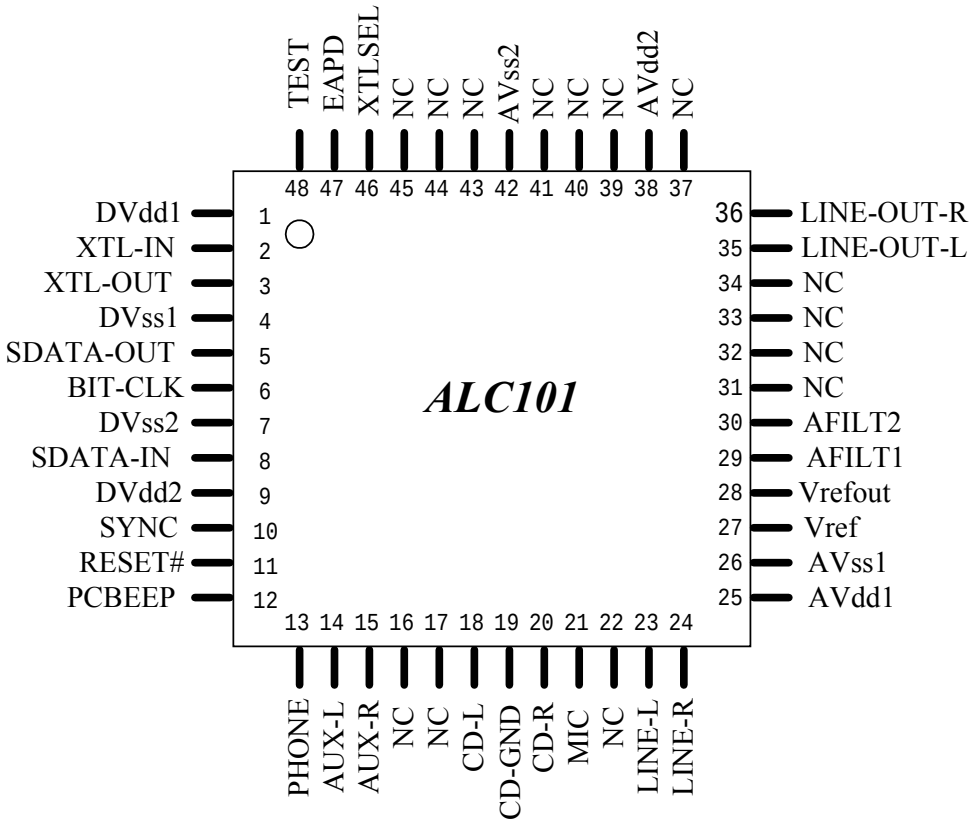
3. Block Diagram



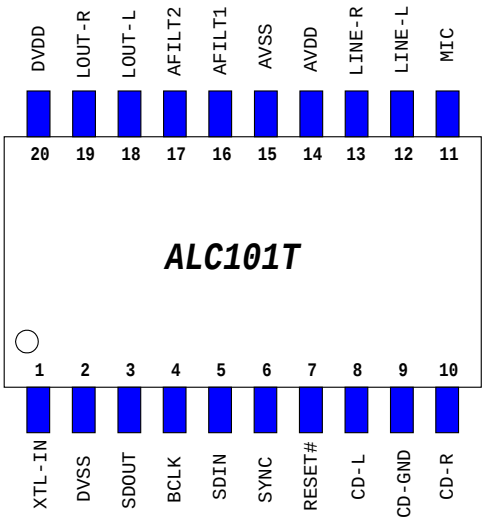
Mixer Function Diagram:

4. Pin Assignments

LQFP-48:



SOP-20:



5. Pin Description

I: Analog or digital input
O: Analog or digital output
P: Power pin or ground pin

5.1 Digital I/O Pins

Name	IO	Pin No (LQFP-48)	Pin No (SOP-20)	Description	Characteristic Definition
RESET#	I	11	7	AC'97 master H/W reset	Schmitt trigger input
XTL-IN	I	2	1	Crystal input pad	Crystal input pad (24.576MHz / 14.318MHz)
XTL-OUT	O	3	-	Crystal output pad	Crystal output pad
SYNC	I	10	6	Sample Sync (48Khz)	Schmitt trigger input
BIT-CLK	O	6	4	Bit clock output (12.288Mhz)	CMOS input/output Vt=0.35Vdd
SDATA-OUT	I	5	3	Serial TDM AC97 output	Schmitt trigger input
SDATA-IN	O	8	5	Serial TDM AC97 input	CMOS output
XTLSEL	I	46	-	Crystal Select	Internal pulled high (At least 20K ohm)
EAPD	O	47	-	External Amplifier power down control	2mA CMOS output
TEST	I	48	-	Enable test function	Internal pull high, refer to session 5.7.3 for detail information.

5.2 Analog I/O Pins

Name	IO	Pin No (LQFP-48)	Pin No (SOP-20)	Description	Characteristic Definition
PCBEEP	I	12	-	Speaker phone input	Analog input (1Vrms), Rin=8K
PHONE	I	13	-	Mono phone input	Analog input (1Vrms), Rin=8K
AUX-L	I	14	-	AUX Left channel	Analog input (1Vrms), Rin=16K
AUX-R	I	15	-	AUX Right channel	Analog input (1Vrms), Rin=16K
CD-L	I	18	8	CD audio Left channel	Analog input (1Vrms), Rin=16K
CD-GND	I	19	9	CD audio analog GND	Analog input (1Vrms), Rin=16K
CD-R	I	20	10	CD audio Right channel	Analog input (1Vrms), Rin=16K
MIC	I	21	11	Mic input	Analog input (1Vrms), Rin=8K
LINE-L	I	23	12	Line input Left channel	Analog input (1Vrms), Rin=32K
LINE-R	I	24	13	Line input Right channel	Analog input (1Vrms), Rin=32K
LINE-OUTL	O	35	18	Line-Out Left channel	Analog output (1.7Vrms with AMP), Rout=10
LINE-OUTR	O	36	19	Line-Out Right channel	Analog output (1.7Vrms with AMP), Rout=10

5.3 Filter/Reference

Name	IO	Pin No (LQFP-48)	Pin No (SOP-20)	Description	Characteristic Definition
VREF	-	27	-	Reference voltage	Analog output
VREFOUT	O	28	-	Ref. voltage out with 5mA drive	Analog output (2.25V – 2.75V)
AFILT1	-	29	16	ADC anti-alias Filter 1	1000pf to AGND
AFILT2	-	30	17	ADC anti-alias Filter 2	1000pf to AGND

5.4 Power/Ground

Name	IO	Pin No (LQFP-48)	Pin No (SOP-20)	Description	Characteristic Definition
AVDD1	I	25	14	Analog VDD (5.0V)	
AVDD2	I	38	-	Analog VDD (5.0V)	
AVSS1	I	26	15	Analog GND	
AVSS2	I	42	-	Analog GND	
VDD1	I	1	20	Digital VDD (3.3V)	
VDD2	I	9	-	Digital VDD (3.3V)	
VSS1	I	4	2	Digital GND	
VSS2	I	7	-	Digital GND	

5.5 Others

Name	IO	Pin No (LQFP-48)	Pin No (SOP-20)	Description	Characteristic Definition
NC		16,17,31,32 ,33,34,37,3 9,40,41,43, 44,45	-	No Connection.	

6. Registers

6.1 Mixer Registers

Access to registers with an odd number will return a 0. Reading unimplemented registers will also return a 0.

REG. (HEX)	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DE-FAULT
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	5800h
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
0Ah	PCBEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	0	8000h
0Ch	PHONE Volume	Mute	X	X	X	X	X	X	X	X	X	X	PH4	PH3	PH2	PH1	PH0	8008h
0Eh	MIC Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	MI4	MI3	MI2	MI1	MI0	8008h
10h	Line-In Volume	Mute	X	X	NL4	NL3	NL2	NL1	NL0	X	X	X	NR4	NR3	NR2	NR1	NR0	8808h
12h	CD Volume	Mute	X	X	CL4	CL3	CL2	CL1	CL0	X	X	X	CR4	CR3	CR2	CR1	CR0	8808h
16h	Aux Volume	Mute	X	X	AL4	AL3	AL2	AL1	AL0	X	X	X	AR4	AR3	AR2	AR1	AR0	8808h
18h	PCM Out Volume	Mute	X	X	PL4	PL3	PL2	PL1	PL0	X	X	X	PR4	PR3	PR2	PR1	PR0	8808h
1Ah	Record Select	X	X	X	X	X	LRS2	LRS1	LRS0	X	X	X	X	X	RRS2	RRS1	RRS0	0000h
1Ch	Record Gain	Mute	X	X	X	LRG3	LRG2	LRG1	LRG0	X	X	X	X	RRG3	RRG2	RRG1	RRG0	8000h
20h	General Purpose	X	X	3D	X	X	X	X	0	LBK	X	X	X	X	X	X	X	0000h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DP1	DP0	0000h
26h	Power Down Ctrl/Status	EAPD	X	X	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	0	0	X	X	REV1	REV0	AMAP	X	X	X	X	X	X	X	X	X	0600h
7Ch	Vendor ID1	0	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	414Ch
7Eh	Vendor ID2	0	1	0	0	0	1	1	1	0	0	1	1	0	0	0	0	4730h

X: reserved bit, read as 0.

6.2 MX00 Reset

Default: 5800H

Writing any value to this register will start a register reset, and causes all of the registers to revert to their default values. Reading this register returns the ID code of the specific part.

Bit	Type	Function
15	-	**Reserved**
14:10	R	Returns 10110b (Realtek 3D Enhancement)
9	R	Read as 0 (Does not support 20-bit ADC)
8	R	Read as 0 (Supports 18-bit ADC)
7	R	Read as 0 (Does not support 20-bit DAC)
6	R	Read as 0 (Does not support 18-bit DAC)
5	R	Read as 0 (Does not support for Loudness)
4	R	Read as 0 (Does not support Headphone output)
3	R	Read as 0 (No simulated stereo for analog 3D block use)
2	R	Read as 0 (No Bass & Treble Control)
1	R	**Reserved**, read as 0
0	R	Read as 0 (No Dedicated Mic PCM input)

Writing to this register will reset all mixer register to their default value. The written data is ignored.

6.3 MX02 Master Volume (LINE-OUT)

Default: 8000H

This registers controls the overall volume level of the line out functions. Each step on the left and right channels correspond to 1.5dB in increase/decrease in volume.

Bit	Type	Function
15	R/W	**Mute Control:** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**Master Left Volume:** (MLV[4:0]) in 1.5 dB step
7:5	-	**Reserved**
4:0	R/W	**Master Right Volume:** (MRV[4:0]) in 1.5 dB step

❶ For MRV/MLV: 00h 0 dB attenuation
1Fh 46.5 dB attenuation

❷ Implement 5-bit volume control only. Writing 1xxxxx will be interpreted as x11111 and when read will respond with x11111.

6.4 MX0A PCBEEP Volume

Default: 8000H

This register controls the input volume for the PC beep signal. Each step in bits 4:1 correspond to a 3dB increase/decrease in volume. 16 levels of volume are available, from 0000 to 1111.

The purpose of this register is to allow the PC Beep signals to pass through the ALC101, eliminating the need for an external system speaker/buzzer. The PC BEEP pin is directly routed (internally hardwired) to the LINE-OUTL & R pins. If the PC speaker/buzzer is eliminated, it is recommended to connect the external speakers at all times so the POST codes can be heard during reset.

Bit	Type	Function
15	R/W	**Mute Control:** 0: Normal 1: Mute (-∞ dB)
14:5	-	**Reserved**
4:1	R/W	**PC Beep Volume:** PBV[3:0] in 3 dB steps
0	-	**Reserved**

For PBV: 00h 0 dB attenuation
0Fh 45 dB attenuation

6.5 MX0C PHONE Volume

Default: 8008H

Register 0Ch controls the telephone input volume for software modem applications. Because software modem applications may not have a speaker, the CODEC can offer a speaker-out service. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 0: Normal 1: Mute (-∞ dB)
14:5	-	**Reserved**
4:0	R/W	**Phone Volume:** PV[4:0] in 1.5 dB steps

For PV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.6 MX0E MIC Volume

Default: 8008H

Register 0Eh controls the microphone input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111. Each step in bit 6 corresponds to a magnification of 20dB increase in volume.

Bit	Type	Function
15	R/W	**Mute Control:** 0: Normal 1: Mute (-∞ dB)
14:7	-	**Reserved**
6	R/W	**20 dB Boost Control:** 0: Normal 1: 20 dB boost
5	-	**Reserved**
4:0	R/W	**Mic Volume:** MV[4:0] in 1.5 dB steps

For MV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.7 MX10 LINE_IN Volume

Default: 8808H

Register 10h controls the LINE_IN input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**Line-In Left Volume:** NLV[4:0] in 1.5 dB steps
7:5	-	**Reserved**
4:0	R/W	**Line-In Right Volume:** NRV[4:0] in 1.5 dB steps

For NLV/NRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.8 MX12 CD Volume

Default: 8808H

Register 12h controls the CD input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**CD Left Volume:** CLV[4:0] in 1.5 dB steps
7:5	-	**Reserved**
4:0	R/W	**CD Right Volume:** CRV[4:0] in 1.5 dB steps

For CLV/CRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.9 MX16 AUX Volume

Default: 8808H

Register 16h controls the auxiliary input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	AUX Left Volume: ALV[4:0] in 1.5 dB steps
7:5	-	**Reserved**
4:0	R/W	**AUX Right Volume:** ARV[4:0] in 1.5 dB steps

For ALV/ARV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.10 MX18 PCM_OUT Volume

Default: 8808H

Register 18h controls the PCM_OUT output volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 0: Normal 1: Mute (-∞ dB)
14:13	-	**Reserved**
12:8	R/W	**PCM Volume:** PLV[4:0] in 1.5 dB steps
7:5	-	**Reserved**
4:0	R/W	**PCM Right Volume:** PRV[4:0] in 1.5 dB steps

For PLV/PRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.11 MX1A Record Select

Default: 0000H

Register 1Ah controls the record input selection. Depending on the value entered, the record input can be taken from the Mic, CD, Video, Aux, Line, Stereo Mixer, Mono Mixer or Phone.

Bit	Type	Function
15:11	-	**Reserved**
10:8	R/W	**Left Record Source Select:** LRS[2:0]
7:3	-	**Reserved**
2:0	R/W	**Right record Source Select:** RRS[2:0]

❶ For LRS

0 MIC
1 CD LEFT
2 VIDEO LEFT (Not Supported)
3 AUX LEFT
4 LINE LEFT
5 STEREO MIXER OUTPUT LEFT
6 MONO MIXER OUTPUT
7 PHONE

❷ For RRS

0 MIC
1 CD RIGHT
2 VIDEO RIGHT (Not Supported)
3 AUX RIGHT
4 LINE RIGHT
5 STEREO MIXER OUTPUT RIGHT
6 MONO MIXER OUTPUT
7 PHONE

6.12 MX1C Record Gain

Default: 8000H

Register 1Ch controls the record gain. Each step in bits 3:0 correspond to 1.5dB in increase/decrease in gain for the right channel, allowing 16 levels of gain, from 0000 to 1111. Each step in bits 11:8 correspond to 1.5dB in increase/decrease in gain for the left channel, allowing 16 levels of gain, from 0000 to 1111.

Bit	Type	Function
15	R/W	**Mute Control:** 0: Normal 1: Mute (-∞ dB)
14:12	-	**Reserved**
11:8	R/W	**Left Record Gain Select:** LRG[3:0]) in 1.5 dB steps
7:4	-	**Reserved**
3:0	R/W	**Right Record Gain Select:** RRG[3:0] in 1.5 dB steps

For LRG/RRG: 0Fh +22.5dB
00h 0 dB (No Gain)

6.13 MX20 General Purpose Register

Default: 0000H

This register is used to control several functions. Bit 13 enables or disables 3D control. Bit 7 enables loopback of the AD output to the DA input without involving the AC-Link, allowing for full system performance measurements.

Bit	Type	Function
15:14	R	**Reserved**, Read as 0
13	R/W	**3D Control:** 1: On 0: Off
12:8	R	**Reserved**, Read as 0
7	R/W	**AD to DA Loop-back Control:** 0: Disable 1: Enable
6:0	-	**Reserved**

6.14 MX22 3D Control

Default: 0000H

This register is used to control the 3D stereo enhancement function built into the AC'97 component. The register bits, DP1-DP0 are used to control the separation ratios in the 3D control for both LINE_OUT and DAC_OUT respectively. This allows for independent control of the stereo enhancement between LINE_OUT and DAC_OUT.

The 3D stereo enhancement function provides for a deeper and wider sound experience with a potential 6-speaker arrangement. Note that the 3D bit in the general purpose register (bit 13) must be set to 1 to enable this function.

Bit	Type	Function
15:2	R	**Reserved**, Read as 0
1:0	R/W	**Depth Control:** DP[1:0]

3D effect control:

DP[1:0]	Function
00	Off (R=0KΩ)
01	33% (R=5KΩ)
10	66%(R=7.5KΩ)
11	100%(R=10KΩ)

6.15 MX26 Powerdown Control/Status

Default: 000FH

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status; a "1" indicating that the subsection is "ready." Ready is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7 and bit 15.

When the AC-Link "CODEC Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this powerdown control /status register to determine exactly which subsections, if any are ready.

Bit	Type	Function
15	R/W	**PR7 External Amplifier Power Down:** (EAPD) 0: EAPD output low (enable external amplifier) 1: EAPD output high (shut down external amplifier)
14:13	-	**Reserved**
12	R/W	PR4 0: Normal 1: Power down AC-Link
11	R/W	PR3 0: Normal 1: Power down Mixer (Vref off)
10	R/W	PR2 0: Normal 1: Power down Mixer (Vref still on)
9	R/W	PR1 0: Normal 1: Power down PCM DAC (front DAC)
8	R/W	PR0 0: Normal 1: Power down PCM ADC and input MUX
7:4	R	**Reserved**, Read as 0
3	R	**Vref Status:** 1: Vref is up to normal level 0: Not ready
2	R	**Analog Mixer Status** 1: Ready 0: Not ready
1	R	**DAC Status:** 1: Ready 0: Not ready
0	R	**ADC Status:** 1: Ready 0: Not ready

True table for power down mode:

	ADC	DAC	Mixer	Verf	ACLINK	EAPD
PR0=1	PD					
PR1=1		PD				
PR2=1	PD	PD	PD			
PR3=1	PD	PD	PD	PD		
PR4=1	PD	PD			PD	
PR7=1						High

PD: Power down Blank: Don't care High: output high

6.16 MX28 Extended Audio ID

Default: 0600H

The Extended Audio ID register is a read only register used to communicate information to the digital controller on two functions. ID1 and ID0 echo the configuration of the CODEC as defined by the programming of pins 47 and 48 externally. "00" returned defines the CODEC as the primary CODEC, while any other code identifies the CODEC as one of three secondary CODEC possibilities.

Bit	Type	Function
15	R	**ID1**, always read as 0.
14	R	**ID0**, always read as 0.
13:12	R	**Reserved**, Read as 0
11:10	R	REV[1:0]=01 indicates that the ALC101 is AC'97 rev2.2 compliant.
9	R	**AMAP** read as 1 (DAC mapping base on CODEC ID)
8:1	-	**Reserved**
0	R	**VRA** read as 0 (Variable sample rate is not supported)

6.17 MX7C VENDOR ID1

Default: 414CH

The two registers (MX7C Vendor ID1 and MX7E Vendor ID2) contain four 8-bit ID codes. The first three codes have been assigned by Microsoft for Plug and Play definitions. The fourth code is a Realtek assigned code identifying the ALC101. The MX7C Vendor ID1 register contains the value 414Ch, which is the first and second characters of the Microsoft ID code. The MX7C Vendor ID2 register contains the value 4730h, which is the third of the Microsoft ID code.

Bit	Type	Function
15:0	R	Vendor ID “AL”

6.18 MX7E VENDOR ID2

Default: 4730H

Bit	Type	Function
15:8	R	Vendor ID “G”
7:4	R	Chip ID 0011 (ALC101)
3:0	R	Read as 0.

7. Electrical Characteristics

7.1 DC Characteristics

7.1.1 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies					
Digital	DVdd	3.0	3.3	3.6	V
Analog	AVdd	3.3	5.0	5.5	V
Operating Ambient Temperature	Ta	0	-	+70	^{o}C
Storage Temperature	Ts			+125	^{o}C
ESD (Electrostatic Discharge)					
	Susceptibility Voltage				
Pin-38 (AVdd2)	4000V				
Others	Over 5000V				

7.1.2 Threshold Hold Voltage

Dvdd= 3.3V±5%, $T_{ambient}$=25^{0}C, with 50pF external load.

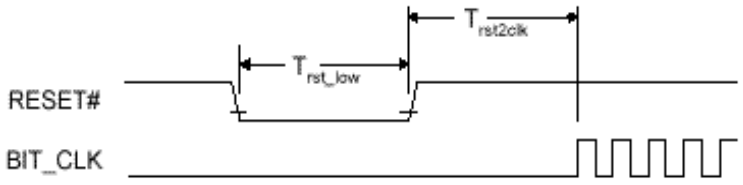
Parameter	Symbol	Minimum	Typical (Dvdd=3.3v)	Maximum	Units
Digital Power Supply	Dvdd	3.0	3.3	3.6	V
Input voltage range	V_{in}	-0.30	-	Dvdd+0.30	V
Low level input voltage	V_{IL}	-	-	0.35Dvdd	V
High level input voltage	V_{IH}	0.60DVdd	-	-	V
High level output voltage	V_{OH}	0.9DVdd		-	V
Low level output voltage	V_{OL}	-	-	0.1DVdd	V
Input leakage current	-	-10	-	10	uA
Output leakage current (Hi-Z)	-	-10	-	10	uA
Output buffer drive current	-	-	8	-	mA

7.1.3 Digital Filter Characteristics

Filter	Symbol	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-76.0		dB
	Passband Frequency Response		+- 0.15		dB
DAC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-78.5		dB
	Passband Frequency Response		+- 0.15		dB

7.2 AC Timing Characteristics

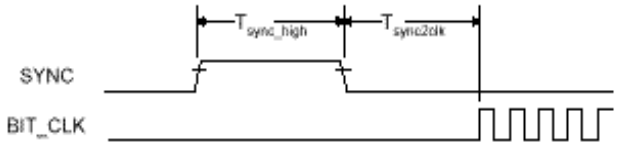
7.2.1 Cold Reset



Cold reset timing diagram

Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	us
RESET# inactive to BIT_CLK Startup delay	$T_{rst2clk}$	162.8	-	-	ns

7.2.2 Warm Reset



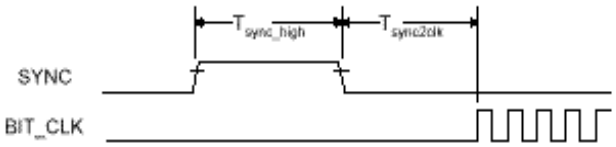
Warm reset timing diagram

Parameter	Symbol	Minimum	Typical	Maximum	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	us
SYNC inactive to BIT_CLK Startup delay	$T_{sync2clk}$	162.8	-	-	ns

7.2.3 AC-Link Clocks

The ALC101 derives its clock internally from an externally connected 24.576MHz crystal or an oscillator through the XTAL_IN pin. Synchronization with the AC'97 controller is achieved through the BIT_CLK pin at 12.288MHz (half of crystal frequency.

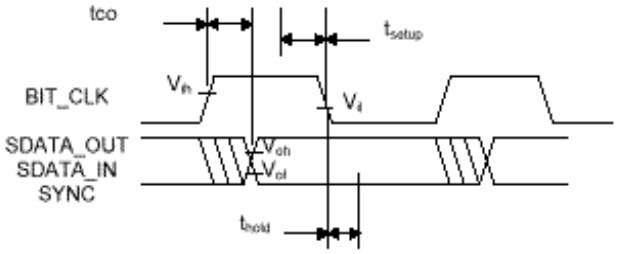
The beginning of all audio sample packets, or "Audio Frames," transferred over AC-Link is synchronized to the rising edge of the "SYNC" signal driven by the AC'97 controller. Data is transitioned on AC-Link on every rising edge of BIT_CLK, and subsequently sampled by the receiving side on each immediately following falling edge of BIT_CLK.



BIT_CLK and SYNC timing diagram

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width (note 2)	T_{clk_low}	36	40.7	45	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	T_{sync_period}	-	20.8	-	us
SYNC high pulse width	T_{sync_high}	-	1.3	-	us
SYNC low pulse width	T_{sync_low}	-	19.5	-	us
Note 1: 47.5~70pF **********					
Note 2: Worse case duty cycle restricted to 45/55.					

7.2.4 Data Output and Input Times



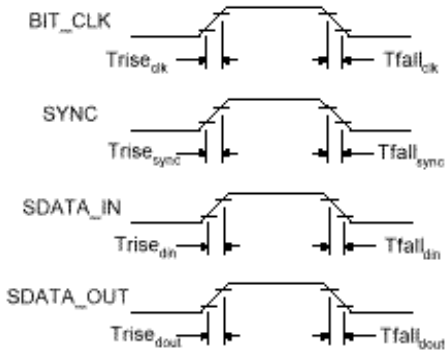
Data Output and Input timing diagram

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Valid Delay from rising edge of BIT_CLK	t_{co}	-	-	15	ns
Note 1: Timing is for SDATA and SYNC outputs with respect to BIT_CLK *at the device driving the output.* Note 2: 50pF external load					

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Setup to falling edge of BIT_CLK	t_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	t_{hold}	10	-	-	ns
Note: Timing is for SDATA and SYNC outputs with respect to BIT_CLK *at the device driving the output.*					

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK combined rise or fall plus flight time		-	-	7	ns
SDATA combined rise or fall plus flight time		-	-	7	ns
Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purpose.					

7.2.5 Signal Rise and Fall Times

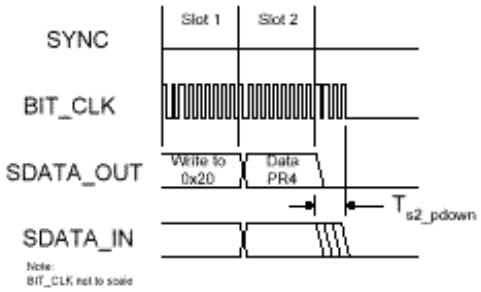


Signal Rise and Fall timing diagram

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK rise time	$Trise_{clk}$	-	-	4	ns
BIT_CLK fall time	$Tfall_{clk}$	-	-	4	ns
SYNC rise time	$Trise_{sync}$	-	-	6	ns
SYNC fall time	$Tfall_{sync}$	-	-	6	ns
SDATA_IN rise time	$Trise_{din}$	-	-	6	ns
SDATA_IN fall time	$Tfall_{din}$	-	-	6	ns
SDATA_OUT rise time	$Trise_{dout}$	-	-	6	ns
SDATA_OUT fall time	$Tfall_{dout}$	-	-	6	ns
Note 1: 75pF external load (50 pF in AC'97 rev2.1) Note 2: rise is from 10% to 90% of Vdd (V_{ol} to V_{oh}) Note 3: fall is from 90% to 10% of Vdd (V_{oh} to V_{ol})					

7.2.6 AC-Link Low Power Mode Timing

The ALC101 AC-Link can be placed into low power mode by programming register 26h. Both BIT_CLK and SDATA_IN will be brought to and held at a logic low voltage level. The AC'97 controller can wake up the ALC101 by providing the proper reset signals.

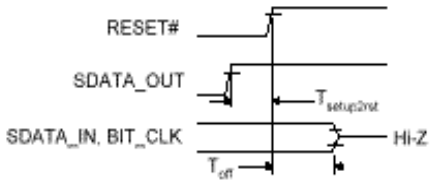


AC-Link low power mode timing diagram

Parameter	Symbol	Minimum	Typical	Maximum	Units
End of slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	us

BIT_CLK and SDATA_IN are transitioned low immediately (within the maximum specified time) following the decode of the write to the Powerdown register (26h) with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-Link into its low power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame after all audio sources have been neutralized. The AC'97 controller should also drive SYNC and SDATA_OUT low after changing the ALC101 to low power mode.

7.2.7 ATE Test Mode



ATE test mode timing diagram

****To meet AC'97 rev2.2, there are EAPD, BIT_CLK, and SDATA_IN should be floating in test mode.***

Parameter	Symbol	Minimum	Typical	Maximum	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns

7.2.8 AC-Link IO Pin Capacitance and Loading

Output Pin	1 CODEC	2 CODEC	3 CODEC	4 CODEC
BIT_CLK (must support ≥ 2 CODECs)	55pF	62.5pF	75pF	85pF
SDATA_IN	47.5pF	55pF	60pF	62.5pF

7.2.9 BIT-CLK and SDATA-IN State

When RESET# is active, BIT-CLK and SDATA-IN must be floating. The ac-link signals are driven by another AC'97 on a CNR board. This requirement is not mentioned in the AC'97 specifications Rev 2.2. Please refer to CNR (Communication Network Riser) specifications Rev.1.0 pages 23~25 or AC'97 Rev.2.2 for detailed information.

8. Analog Performance Characteristics

Standard test condition: $T_{ambient}=25^0C$, Dvdd=3.3V ±5%,Avdd=5.0V±5%
1KHz input sine wave; Sampling frequency=48KHz; 0dB=1Vrms
10KΩ/50pF load; Test bench Characterization BW: 20Hz~20KHz
0dB attenuation; tone and 3D disabled

Parameter	Minimum	Typical	Maximum	Units
Full scale input voltage				
Line inputs (Mixers)	1.0	1.6	-	Vrms
Line inputs (A/D)	1.0	-	-	
Mic input (0 dB)	1.0	-	-	
Mic input (20 dB boost)	0.10	-	-	
Full scale output voltage				
Line output (D/A)	-	1.0	-	Vrms
Analog to Analog S/N				
CD to LINE_OUT	-	90	-	dB
Other to LINE_OUT	-	85	-	
Analog frequency response	20	-	20,000	Hz
S/N (A-weighted)				
D/A	-	75	-	dB
A/D	-	70	-	
Total Harmonic Distortion (A-weighted)				
D/A	-	70	-	DB
A/D	-	65	-	
D/A & A/D frequency response	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection	-74	-	-	dB
Out-of-Band Rejection	-	-40	-	dB
Group delay	-	-	1	ms
Power Supply Rejection	-	-40	-	dB
Cross-talk between Input Channels			-70	dB
MIC Amplifier 20dB Gain	18	20	22	dB
Input impedance (gain = 0dB)				
MIC, PCBEEP, PHONE		8		KΩ
CD-In, Aux-In		16		KΩ
Line-In		32		
Analog Output Impedance (LINE-OUT)		2		Ω
Power Supply Current			-	
VA		35		mA
VD(@CL=50pf)		5		mA
Power Down Current				
VA		0.8		mA
VD(@CL=50pf)		1.0		mA
V_{refout}	-	2.25-2.75	-	V
V_{refout} Drive Current		8		mA

9. Design Suggestions

9.1 Clocking

Unlike ALC models 201-650, the ALC101 only supports primary mode. Its ID[1:0] is always '00'. Therefore, there is only one clock source:

CODEC ID[1:0]	BIT-CLK (12.288MHz)	Clock source
00	Output	14.318M / 24.576M Crystal or external clock source (XTAL-IN)*
-	-	-
-	-	-
-	-	-

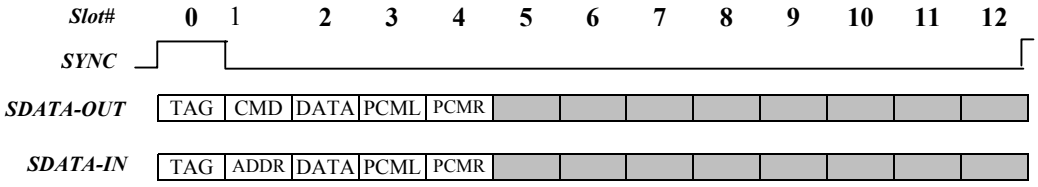
The default clock source frequency decided by XTLSEL, if 14.318MHz crystal or external clock is selected, then the internal PLL will transmit it into 24.576MHz clock.

9.2 AC-Link

When the ALC101 takes serial data from the AC97 controller, it samples **SDATA_OUT** on the falling edge of **BIT_CLK**. When the ALC101 sends serial data to the AC97 controller, it starts to drive **SDATA_IN** on the rising edge of **BIT_CLK.**

The ALC101 will return any uninstalled bits or registers with 0 for read operations. The ALC101 also stuffs the unimplemented slots or bits with 0 in **SDATA-IN**. Note that AC-LINK is MSB-justified.

Refer to "Audio CODEC '97 Component Specification Revision 2.1/2.2" for details.



ALC101 slot arrangement

9.3 Reset

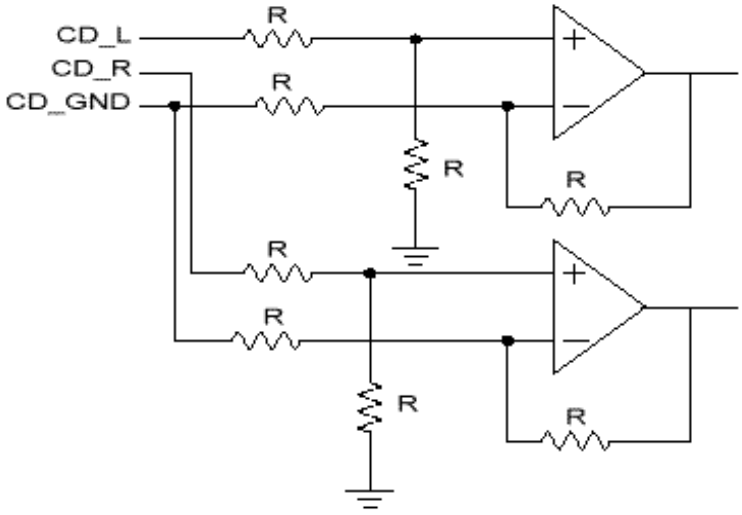
There are 3 kinds of reset operation. ***Cold***, ***Warm*** and ***Register*** reset which listed below:

Reset Type	Trigger condition	CODEC response
Cold	Assert RESET# for a specified period	Reset all hardware logic and all registers to its default value.
Register	Write register indexed 00h	Reset all registers to its default value.
Warm	Driven SYNC high for specified period without BIT_CLK	Reactivates AC-LINK, no change to register values.

The AC97 controller should drive SYNC and SDATA-OUT low during the period of RESET# assertion to guarantee ALC101 reset successfully.

9.4 CD Input

Pay attention to differential CD input. Below is an example of differential CD input.



Example of differential CD input

9.5 Odd Addressed Register Access

The ALC101 will return "0000h" when the odd-addressed registers and unimplemented registers are read.

9.6 Power-down Mode

The power down control register (index 26h) requires special attention, especially PR4 (powerdown AC-link).

9.7 Test Mode

9.7.1 ATE In Circuit Test Mode

SDATA_OUT is sampled high at the trailing edge of RESET#. In this mode the ALC101 will drive BIT_CLK, SDATA_IN, EAPD and SPDIFO to high impedance.

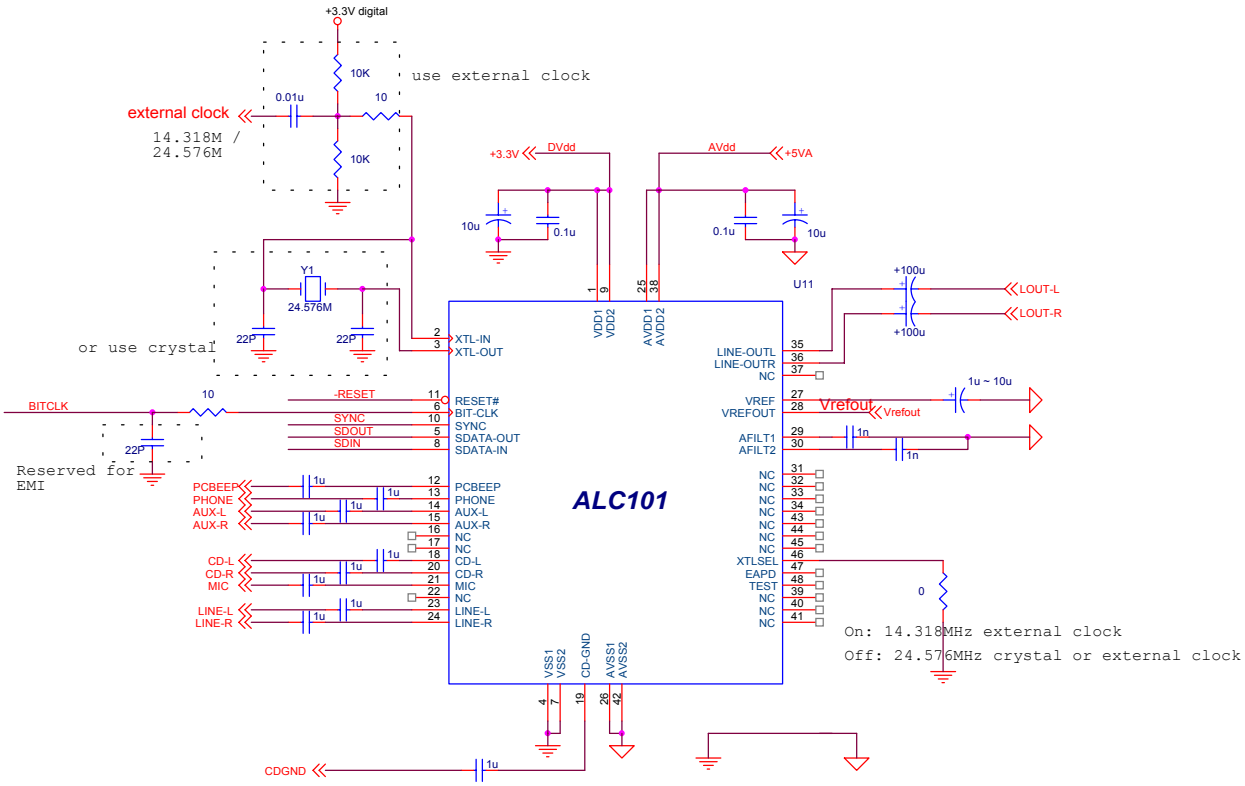
9.7.2 Vendor Specific Test Mode

SYNC is sampled high at the trailing edge of RESET#. At this mode ALC101 will drive BIT_CLK, SDATA_IN, EAPD and SPDIFO to high impedance.

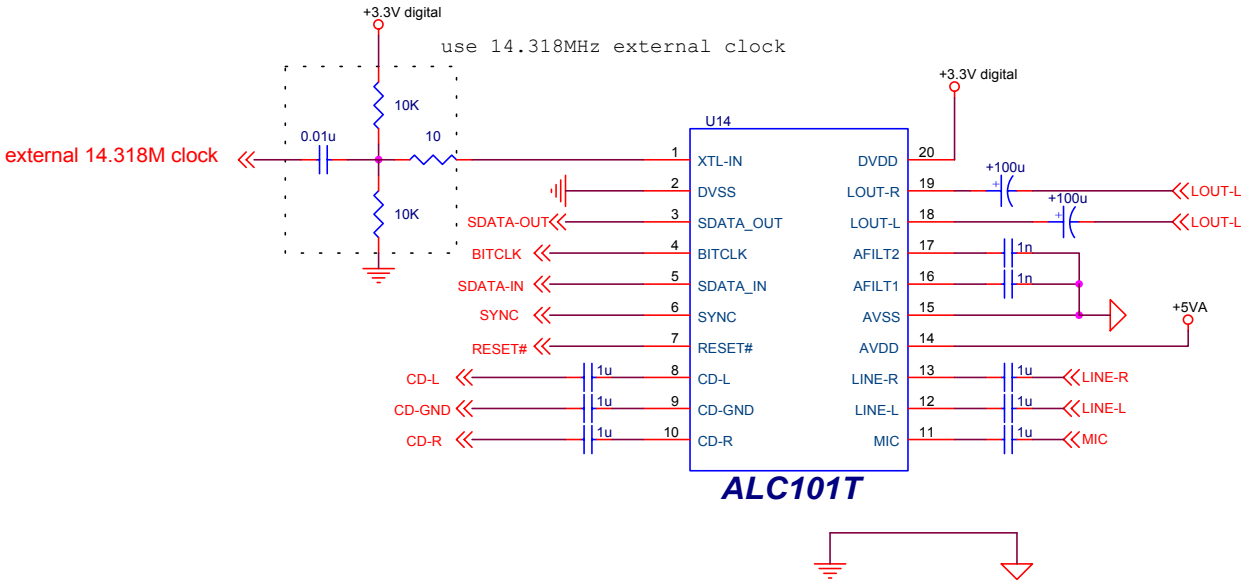
Note: To make the most compatibility with AC'97 rev2.2, ALC101 will float its digital output pins in both ATE and Vendor-Specific test mode. Please refer to AC'97 rev2.2 section 9.2 for detail description about test mode.

10. Application Circuit

10.1 48-pin LQFP Filter Connection Diagram

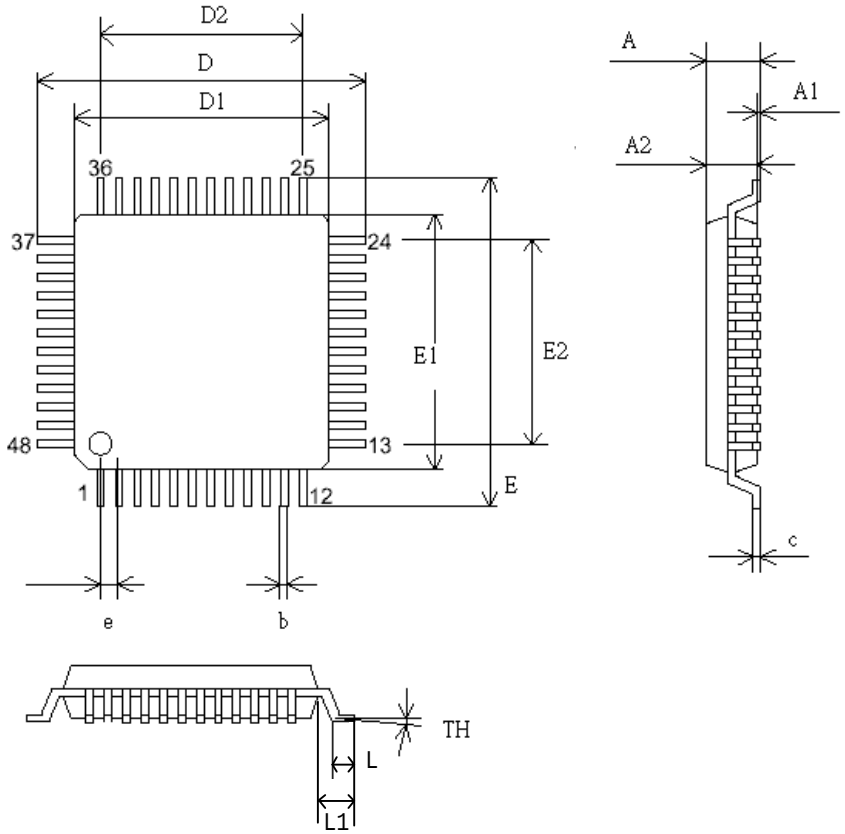


10.2 20-pin SOP Filter Connection Diagram



11. Mechanical Dimensions

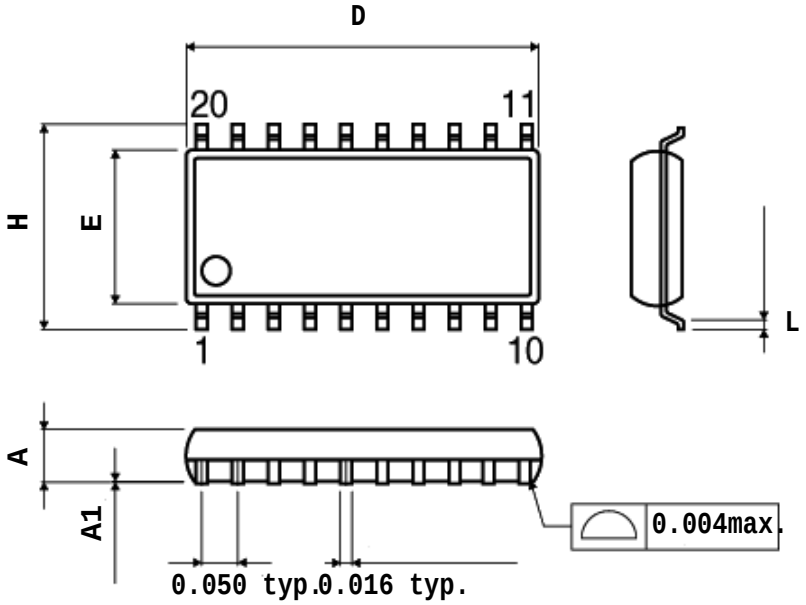
11.1 LQFP-48



SYMBOL	MILLIMETER			INCH		
	MIN.	TYPICAL	MAX.	MIN.	TYPICAL	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.016 BSC		
TH	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1		1.00			0.0393	

TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO.	PKGC-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		

11.2 SOP-20



SYMBOL	INCH		
	MINIMUM	TYPICAL	MAXIMUM
A	0.093	-	0.104
A1	0.004	-	0.012
D	0.496	-	0.508
E	0.291	-	0.299
H	0.394	-	0.419
L	0.016	-	0.050

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