FAN8005D2

3-CH Motor Driver

Features

- 3-Channel BTL (Balanced transformer-less) driver
- Built-in variable regulator with reset (Series-REG)
- Built-in thermal shutdown circuit
- Built-in power save circuit
- Built-in general OP-amp
- Operating supply voltage: 4.5V ~ 5.5V
- Corresponds to 3.3V or 5V DSP

Description

The FAN8005D2 is a monolithic integrated circuit, suitable for a 3-ch motor driver which drives focus actuator, tracking actuator, and sled motor of a CD-media system.

28-SSOPH-300



Typical Applications

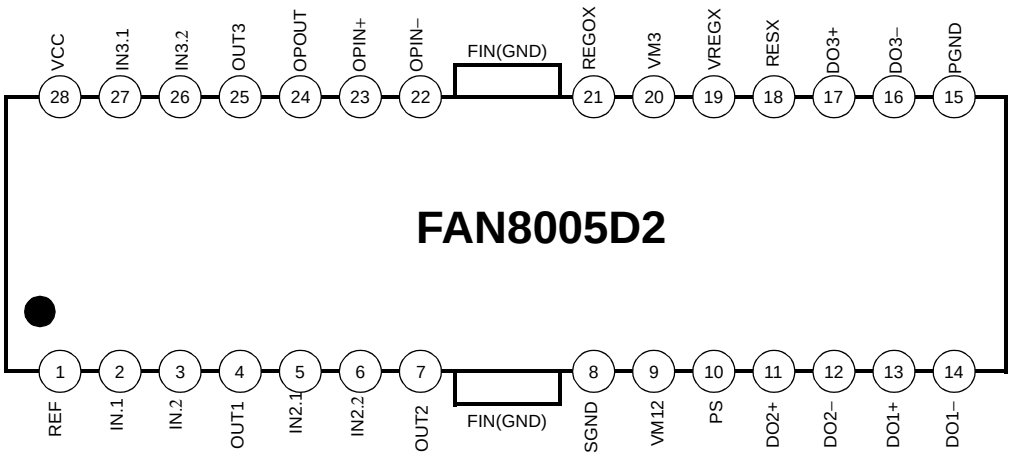
- Compact disk player
- Digital video disk player
- Compact disk ROM

Ordering Information

Device	Package	Operating Temp.
FAN8005D2	28-SSOPH-300	–35°C ~ +85°C
FAN8005D2TF	28-SSOPH-300	–35°C ~ +85°C

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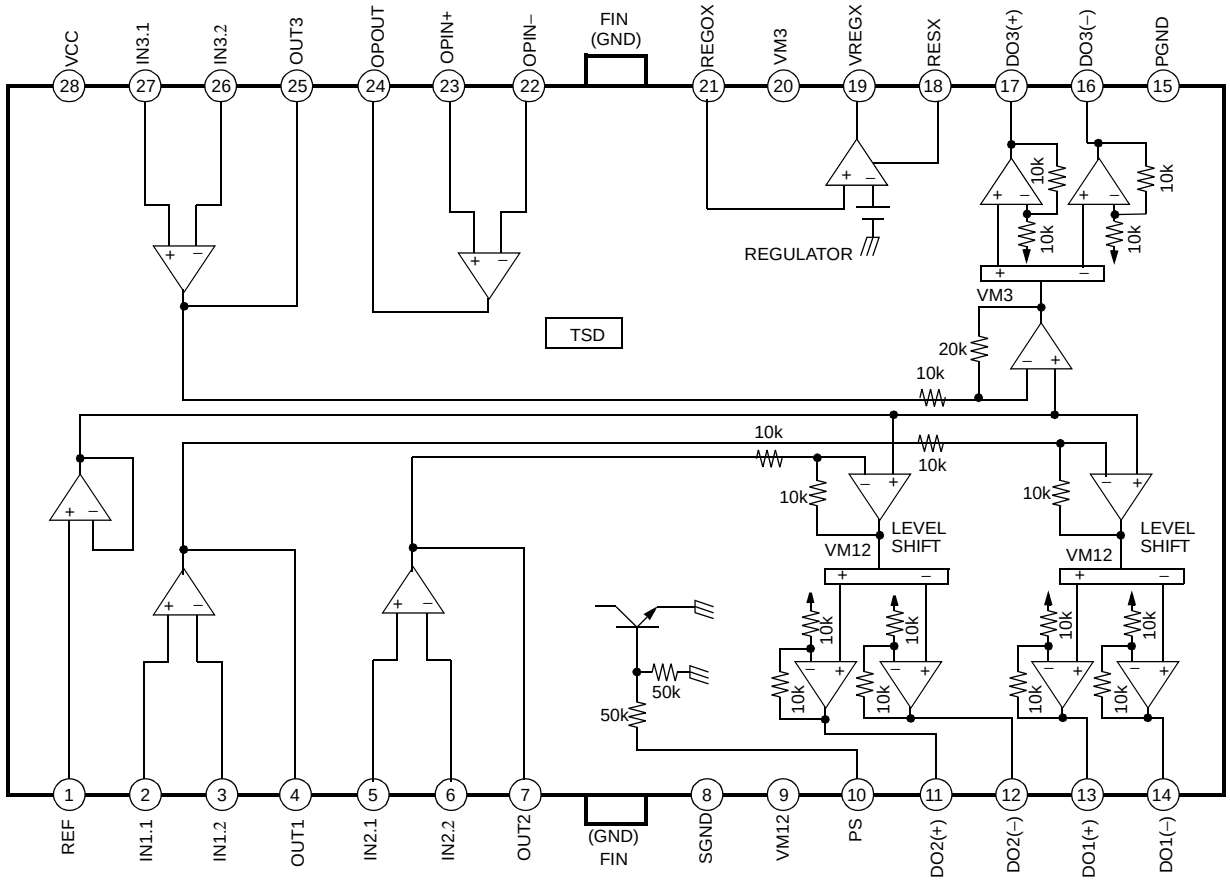
Pin Assignments



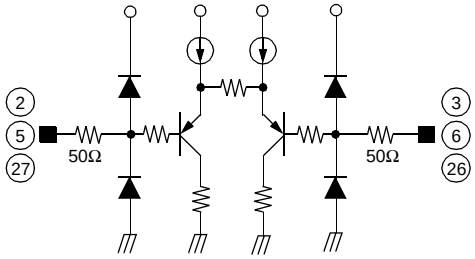
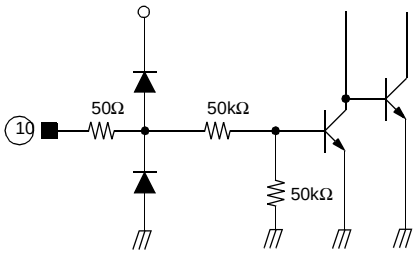
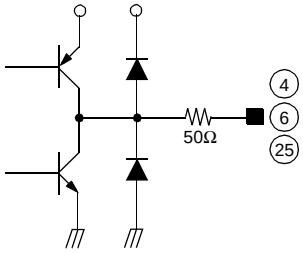
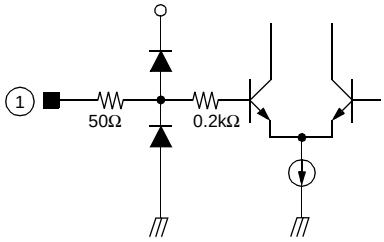
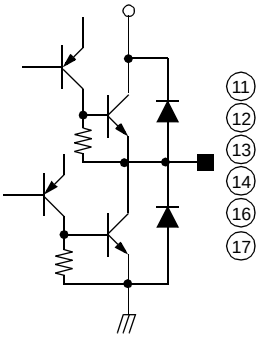
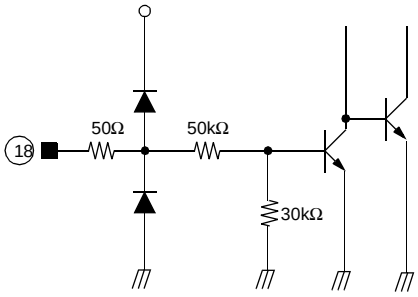
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Descrition
1	REF	I	Bias voltage input
2	IN1.1	I	Op-amp CH1 input (+)
3	IN1.2	I	Op-amp CH1 input (–)
4	OUT1	O	Op-amp CH1 output
5	IN2.1	I	Op-amp CH2 input (+)
6	IN2.2	I	Op-amp CH2 input (–)
7	OUT2	O	Op-amp CH2 output
8	SGND	-	Signal ground
9	VM12	-	BTL CH1, 2 supply voltage
10	PS	I	Power save
11	DO2+	O	Drive2 output (+)
12	DO2–	O	Drive2 output (–)
13	DO1+	O	Drive1 output (+)
14	DO1–	O	Drive1 output (–)
15	PGND	-	Power ground
16	DO3–	O	Drive3 output (–)
17	DO3+	O	Drive3 output (+)
18	RESX	I	Regulator reset
19	VREGX	O	Op-amp output
20	VM3	-	BTL CH3 supply voltage
21	REGOX	I	Op-amp input(+)
22	OPIN–	I	Op-amp input (–)
23	OPIN+	I	Op-amp input (+)
24	OPOUT	O	Op-amp output
25	OUT3	O	Op-amp CH3 output
26	IN3.2	I	Op-amp CH3 input (–)
27	IN3.1	I	Op-amp CH3 input (+)
28	VCC	-	Supply voltage

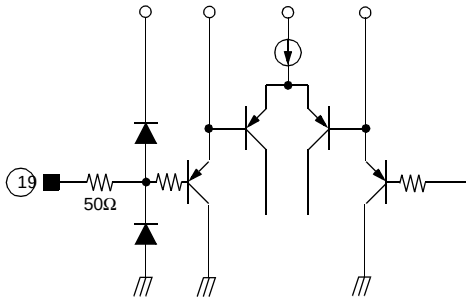
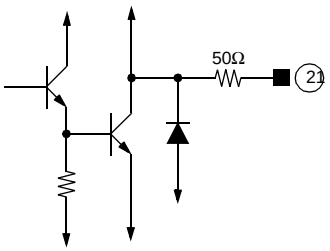
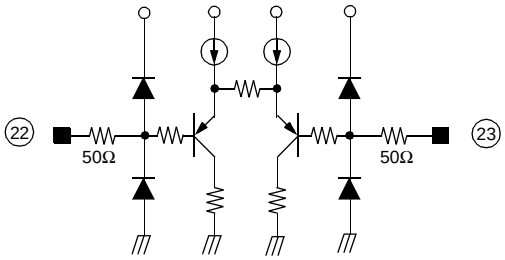
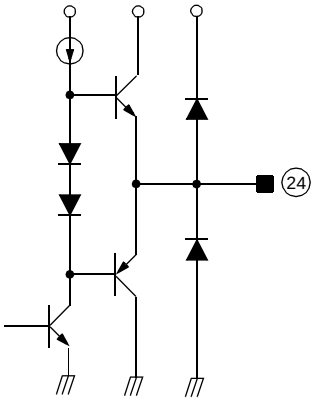
Internal Block Diagram



Equivalent Circuits

Error amp input	Power save input
	
Error amp output	**Signal reference input**
	
Power output	**Regulator reset**
	

Equivalent Circuits (Continued)

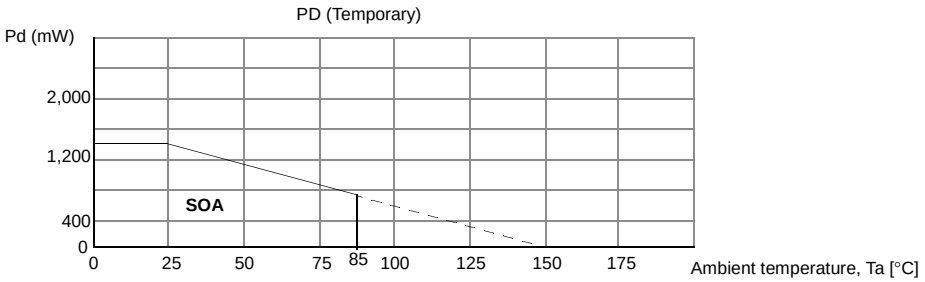
Regulator	Regulator output
	
General op amp input	**General op amp output**
	

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	V_{CCmax}	7	V
Power dissipation	P_D	@1.4	W
Operating temperature range	T_{OPR}	–35 ~ +85	°C
Storage temperature range	T_{STG}	–55 ~ +150	°C

Notes:

1. When mounted on a 76.2mm × 114mm × 1.57mm PCB (Phenolic resin material).
2. Power dissipation reduces 11.2mW / °C for using above Ta = 25°C
3. Do not exceed P_D and SOA (Safe operating area).



Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	-	5.5	V

Electrical Characteristics

(Unless otherwise specified, Ta=25°C, V_{CC}=VM12=VM3=5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Quiescent current	I_{CC}	V_{IN}=0V	-	13	-	mA
Power save on current	I_{PS}	PS pin=GND	-	-	1	mA
Power save on voltage	V_{PSon}	-	-	-	0.5	V
Power save off voltage	V_{PSoff}	-	2	-	-	V
BTL DRIVE CIRCUIT						
Output offset voltage 1	V_{OO1}	V_{IN}=2.5V (CH1,2)	–50	-	+50	mV
Output offset voltage 2	V_{OO2}	V_{IN}=2.5V (CH3)	–60	-	+60	mV
Maximum output voltage 1	V_{OM1}	V_{CC}=5V, R_L=8Ω (CH1, 2)	2.7	3.5	-	V
Maximum output voltage 2	V_{OM2}	V_{CC}=5V, R_L=24Ω (CH3)	3	3.8	-	V
Closed loop voltage gain 1	G_{VC1}	f=1kHz, V_{IN}=0.1V_{RMS} (CH1, 2)	10.5	12	13.5	dB
Closed loop voltage gain 2	G_{VC2}	f=1kHz, V_{IN}=0.1V_{RMS} (CH3)	16	18	20	dB
Ripple rejection ratio	RR	V_{IN}=0.1V_{RMS}, f=120Hz	-	60	-	dB
Slew rate	SR	V_O=2Vp-p, f=120kHz	-	1	-	V/µs
ERROR AMP CIRCUIT						
Input offset voltage	V_{OFOP}	-	–20	-	+20	mV
Input bias current	I_{BOP}	-	-	-	300	nA
High level output voltage	V_{OHOP}	V_{CC}=5V, R_L=10kΩ	4.5	4.8	-	V
Low level output voltage	V_{OLOP}	V_{CC}=5V, R_L =10kΩ	-	0.2	0.5	V
Output sink current	I_{SINK}	V_{CC}=5V, R_L= 1kΩ	1	3	-	mA
Output source current	I_{SOURCE}	V_{CC}=5V, R_L=1kΩ	1	3	-	mA
Slew rate	SR_{OP}	f=120kHz, $2V_{p-p}$	-	1	-	V/µs
GENERAL OP AMP CIRCUIT						
Input offset voltage	V_{OFOP}	-	–20	-	+20	mV
Input bias current	I_{BOP}	-	-	-	300	nA
High level output voltage	V_{OHOP}	V_{CC}=5V, R_L=1kΩ	3	4	-	V
Low level output voltage	V_{OLOP}	V_{CC}=5V, R_L =1kΩ	-	1	1.3	V
Output sink current	I_{SINK}	V_{CC}=5V, R_L= 50Ω	2	5	-	mA
Output source current	I_{SOURCE}	V_{CC}=5V, R_L=50Ω	2	5	-	mA
Open loop voltage gain	G_{VO}	V_{IN}=–75dB, f=1kHz	-	75	-	dB
Ripple rejection ratio	RR_{OP}	V_{IN}=–20dB, f =120Hz	-	65	-	dB
Slew rate	SR_{OP}	f=120kHz, $2V_{p-p}$	-	1	-	V/µs
Common mode rejection ratio	CMRR	V_{IN}=–20dB, f=1kHz	-	80	-	dB
VARIABLE REGULATOR CIRCUIT						
Regulator output voltage	V_{REG}	IL=100mA	3.0	-	4.5	V
Load regulation	ΔV_{R1}	IL=0→200mA	–40	-	10	mV
Line regulation	ΔV_{CC}	IL=200mA, V_{CC}=5→8V	–20	-	30	mV

Application Information

1. Reference Input & Power Save Function

Pin 1 (REF) is a reference input pin.

- Reference input
  The applied voltage at the reference input pin must be between 1.5V and 3.5V, when V_{CC}=5V.
- Power save input
  The following input conditions must be satisfied for the power save function.

Power save on voltage	Below 0.5V	Power save function operation
Power save off voltage	Above 2V	Normal operation

2. Protection Function

Thermal shutdown (TSD)

- If the chip temperature rises above 175°C, the thermal shutdown (TSD) circuit is activated and the output circuit is in the mute state, that is off state. The TSD circuit has a temperature hysteresis of 25°C.

3. Regulator & Reset Function

The regulator configuration with the external components is illustrated in figure 1.

- The external circuit is composed of the KSB772 PNP transistor and a capacitor about 33μF, and two feedback resistors R1, R2.
  The capacitor operates both as a ripple eliminator and as a compensator of the feedback loop.
- The output voltage (REG OUT) is

$$Vout = \left(1 + \frac{R1}{R2}\right) \times 2.5$$

- When the voltage of pin18 (Vreset) is 0V, the regulator reset function is activated, and the output voltage (REG OUT) becomes 0V. Otherwise, if the voltage of pin 18 is 5V, the regulator operates properly.

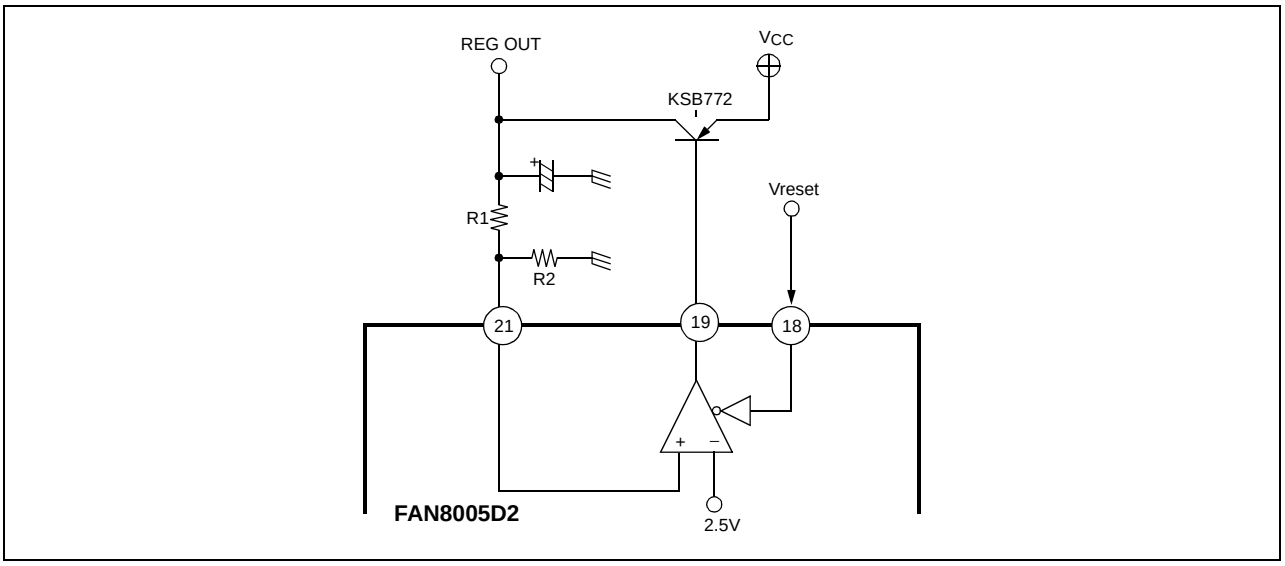
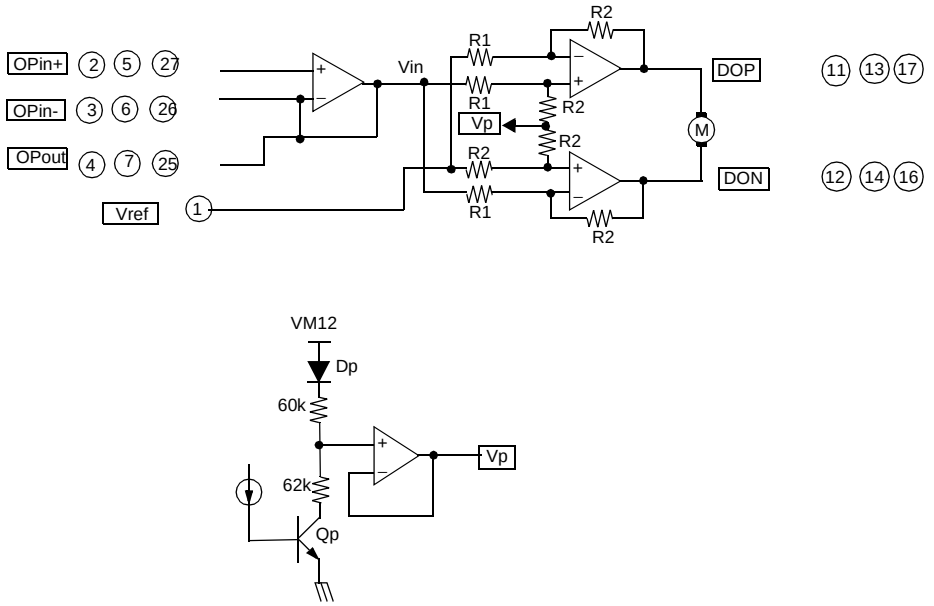


Figure 1. Regulator circuit

4. Focus / Tracking Actuator Sled Motor Drive Part



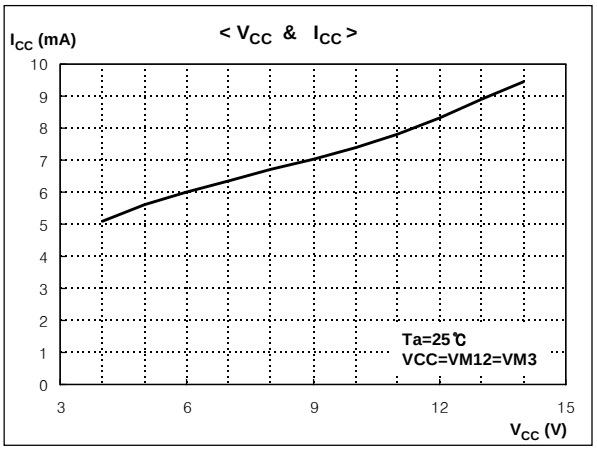
- The voltage, Vref is the reference voltage given by the external bias voltage of the pin 1.
- The input signal (Vin) through pins 3,6 and 26 are amplified one time and then fed to the output stage. (assume that input opamp was used as a buffer)
- The total closed loop voltage gain is as follows (assume that R2=2R1)

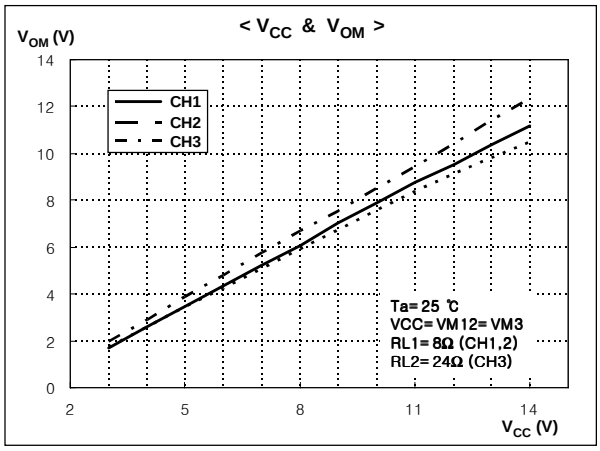
$$Vin = Vref + \Delta V$$
$$DOP = Vp + 2\Delta V$$
$$DON = Vp - 2\Delta V$$
$$Vout = DOP - DON = 4\Delta V$$
$$Gain = 20\log\frac{Vout}{\Delta V} = 20\log 4 = 12dB$$

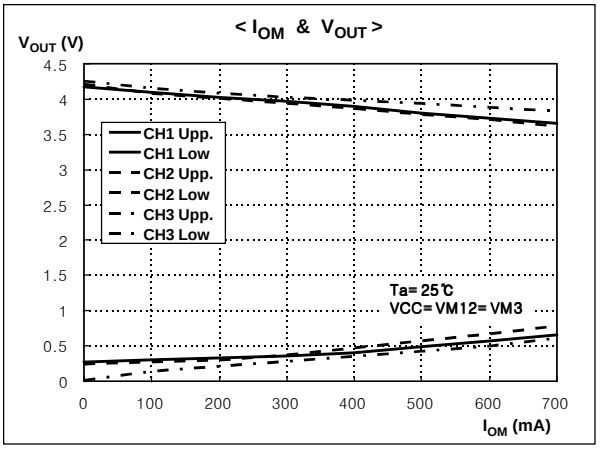
- To change the total closed loop voltage gain, Use the input opamp as an amplifier
- The output stage is the balanced transformerless (BTL) driver.
- The bias voltage Vp is expressed as ;

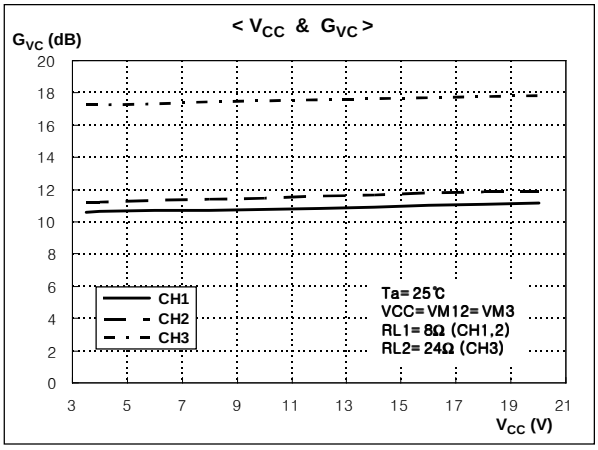
$$Vp = (PVCC1 - VDp - VcesatQp) \times \frac{62k}{60k + 62k} + VcesatQp$$
$$= \frac{PVCC1 - VDp + VcesatQp}{1.97} + VcesatQp \quad \text{----------} \quad (1)$$

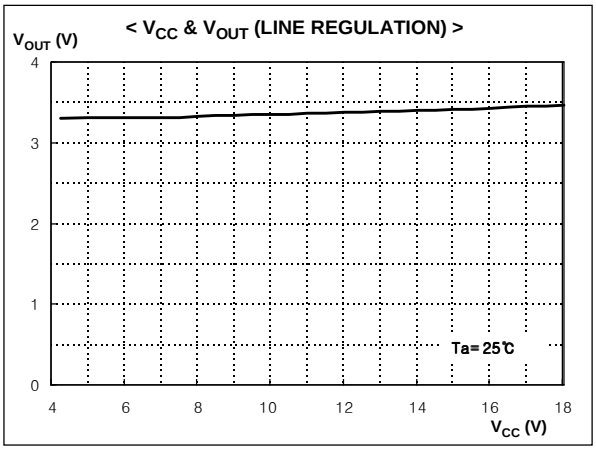
Typical Performance Characteristics

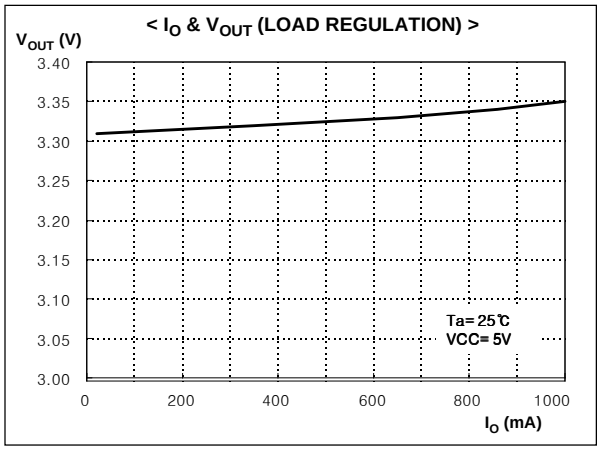




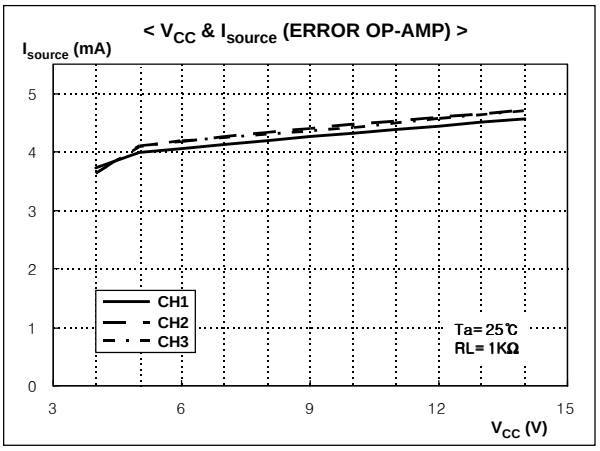


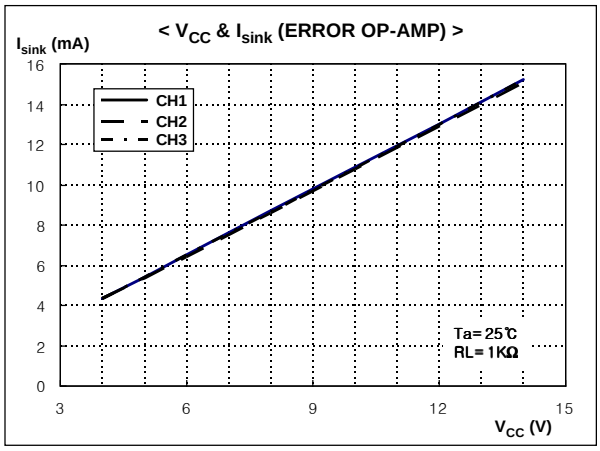


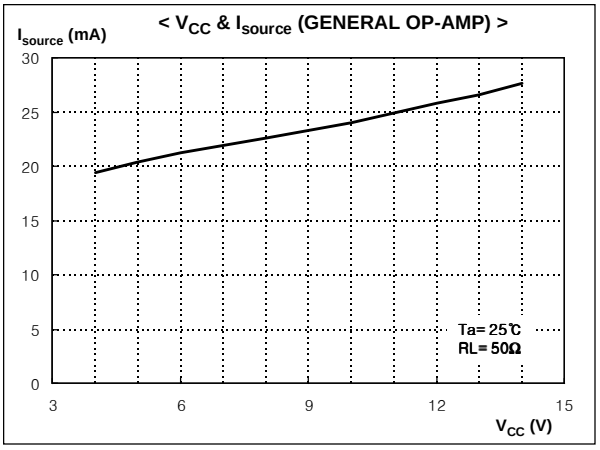


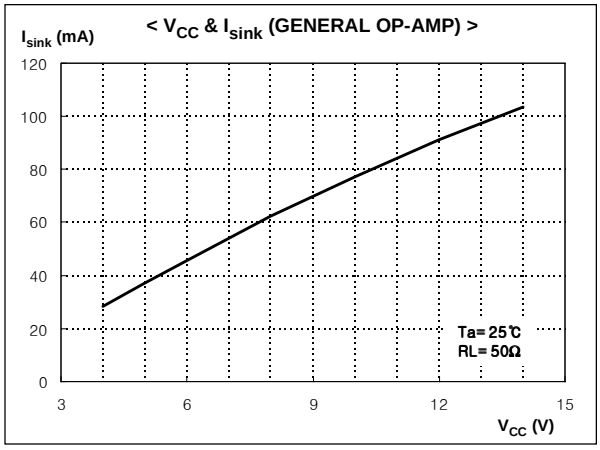


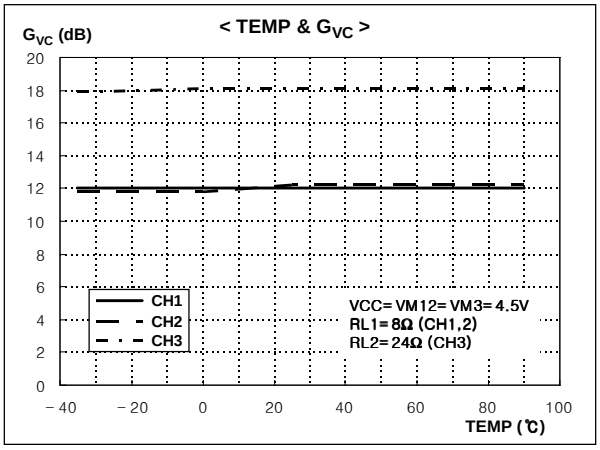
Typical Performance Characteristics (Continued)

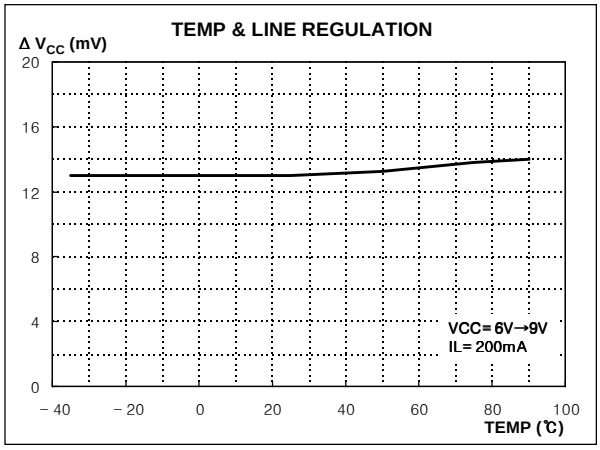






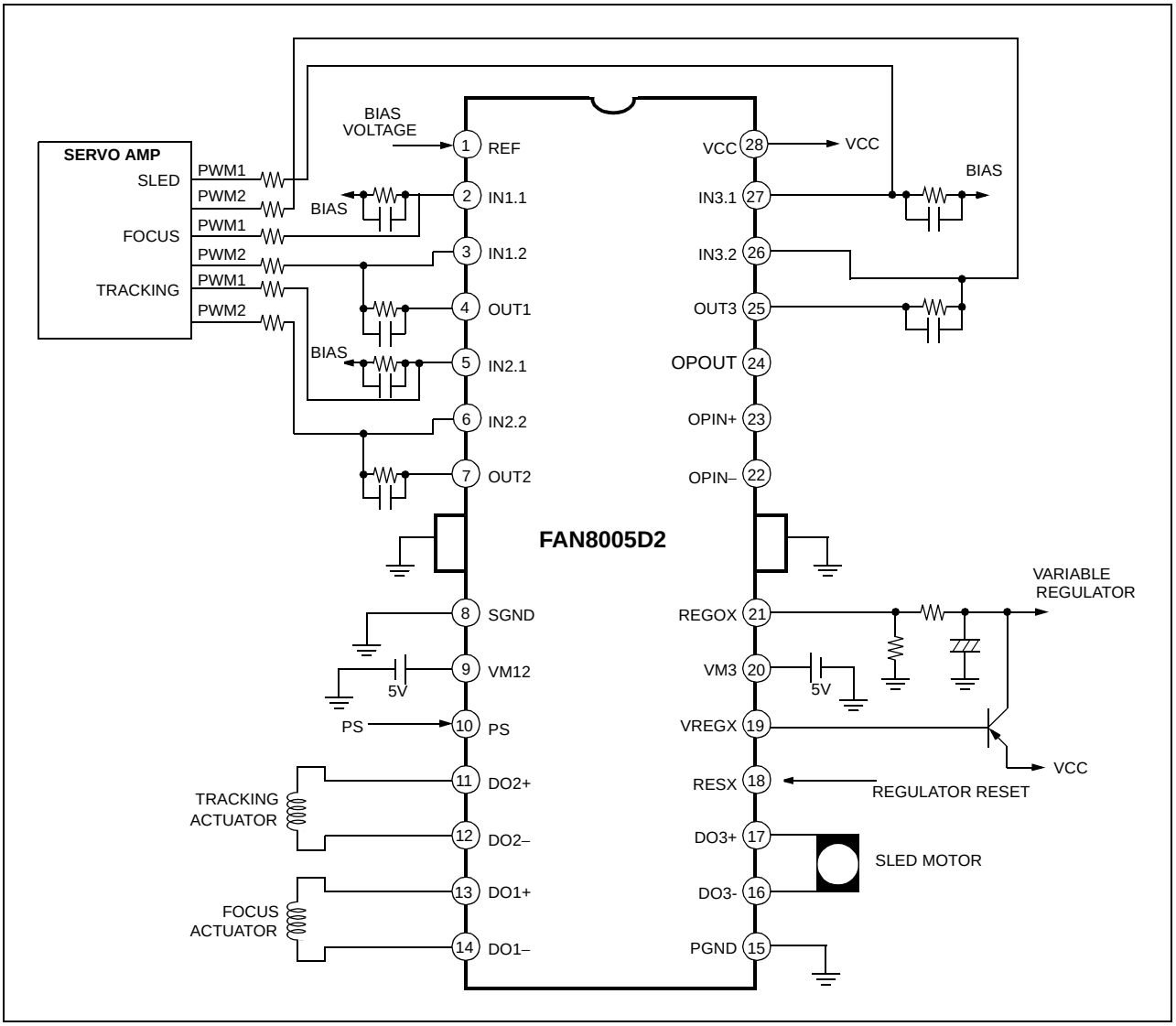






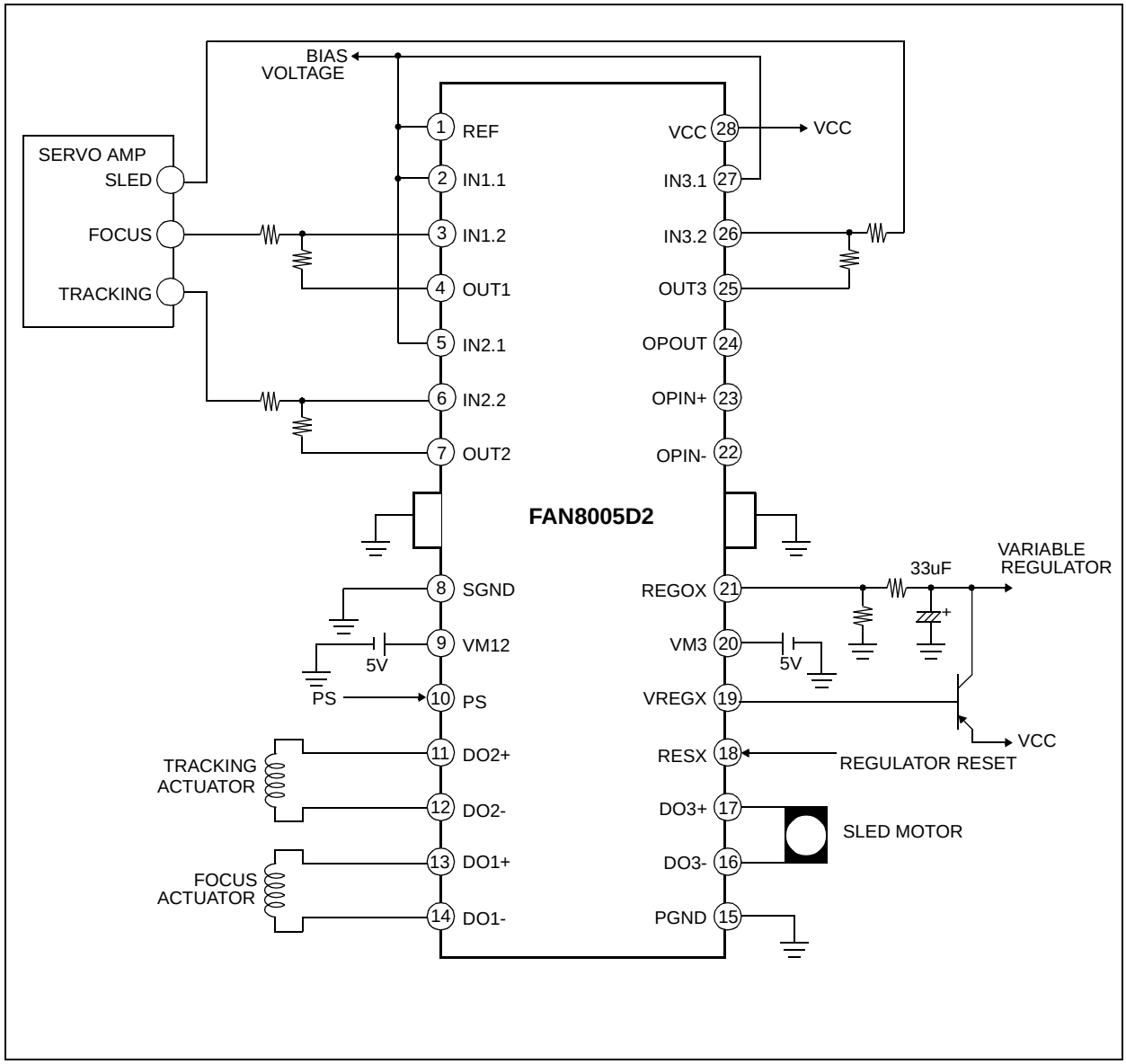
Application Circuits 1

(Differential PWM control mode)



Application Circuits 2

(Voltage control mode)



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