Winbond
Advanced ACPI Controller
W83303AD/W83303AG

winbond

W83303AD/AG
Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1	N.A.			N.A.	All of the versions before 0.50 are for internal use.
2	N.A.	10/25/04	0.5	N.A.	First published preliminary version.
3	N.A.	12/20/04	0.51	N.A.	Add part no of W8303AG with Pb-free package.
4	12,13,14	1/09/06	0.52	N.A.	Modified the application circuit.
5					
6					
7					
8					

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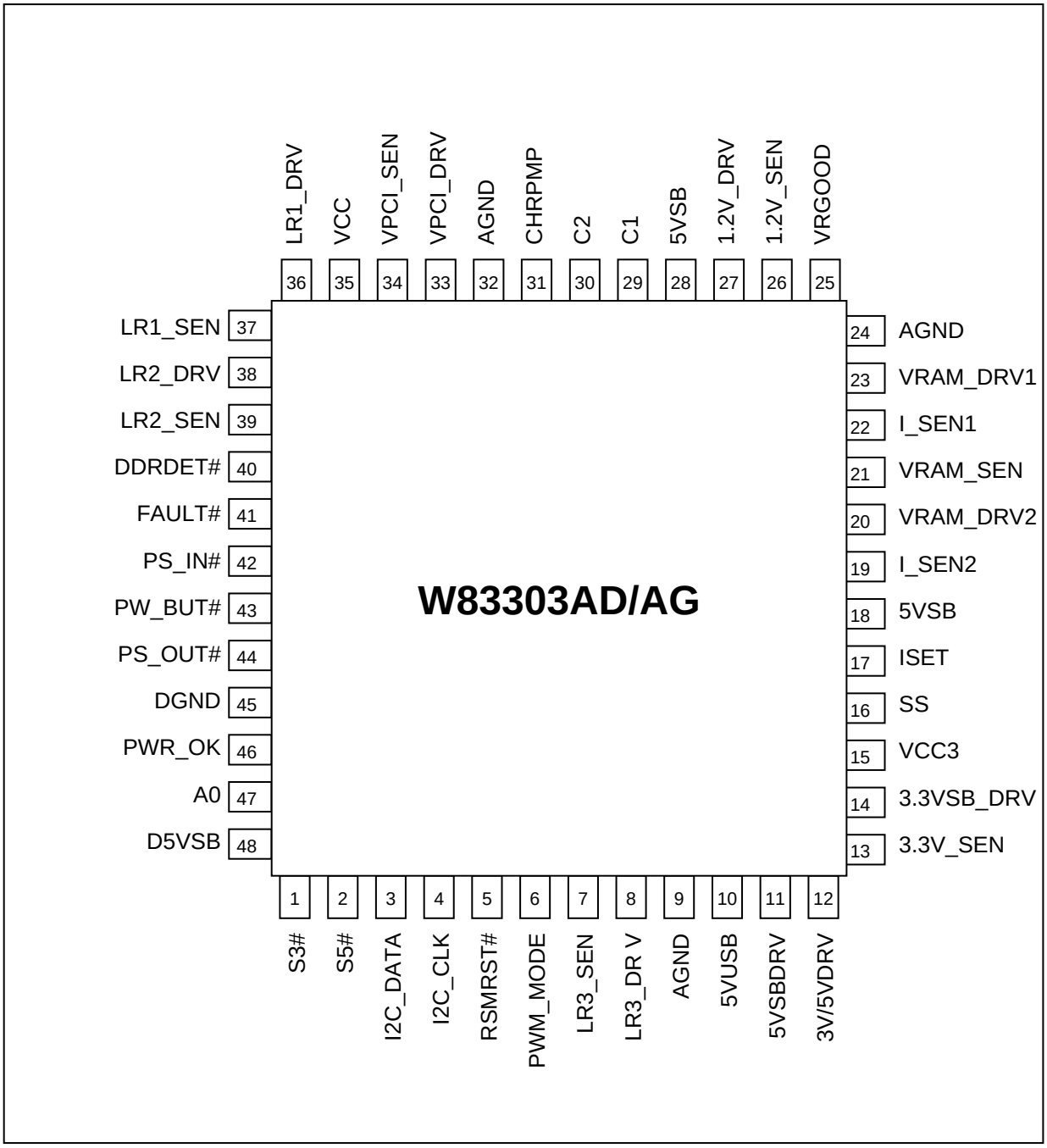
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1. GENERAL FUNCTION DESCRIPTION

- Provides Voltages
  - 5V Active/Sleep (5VDUAL)
  - Programmable $5V_{DL}$/$5V_{STR}$/$5V_{CC}$ for USB Devices(5VUSB)
  - 3.3V Active/Sleep (3.3VDUAL)
  - Programmable Dual-Channels RAM Active/Sleep (V_{STR}) for DDR
  - Auto-detective $2.6V_{STR}$/$1.8V_{STR}$ for DDR/DDRII Voltage
  - Two Programmable Linear Regulators and one Linear Regulator Ranging 1.2V~5.00V for Over-Clocking Application
  - 1.2V VCCVID for Intel® P4 CPU or FSB_VTT for Grandsdale
  - 1.5V VPCI Voltage
- Supports VRGOOD signal for Intel® P4 CPU Power Good Control
- Supports RSMRST# Signal Control
- Provides Signals for ATX Power Supply PS_ON# Control
- I2C Interface
- Selectable I2C Address
- Internal Charge Pump Support Up to 9.5VSB
- Drive All N-Channel MOSFET
- Soft Start
- Under-Voltage Monitoring for 3VDUAL, VPCI and VRAM Channels

2. W83303AD/AG PIN-OUT



3. PIN DESCRIPTIONS

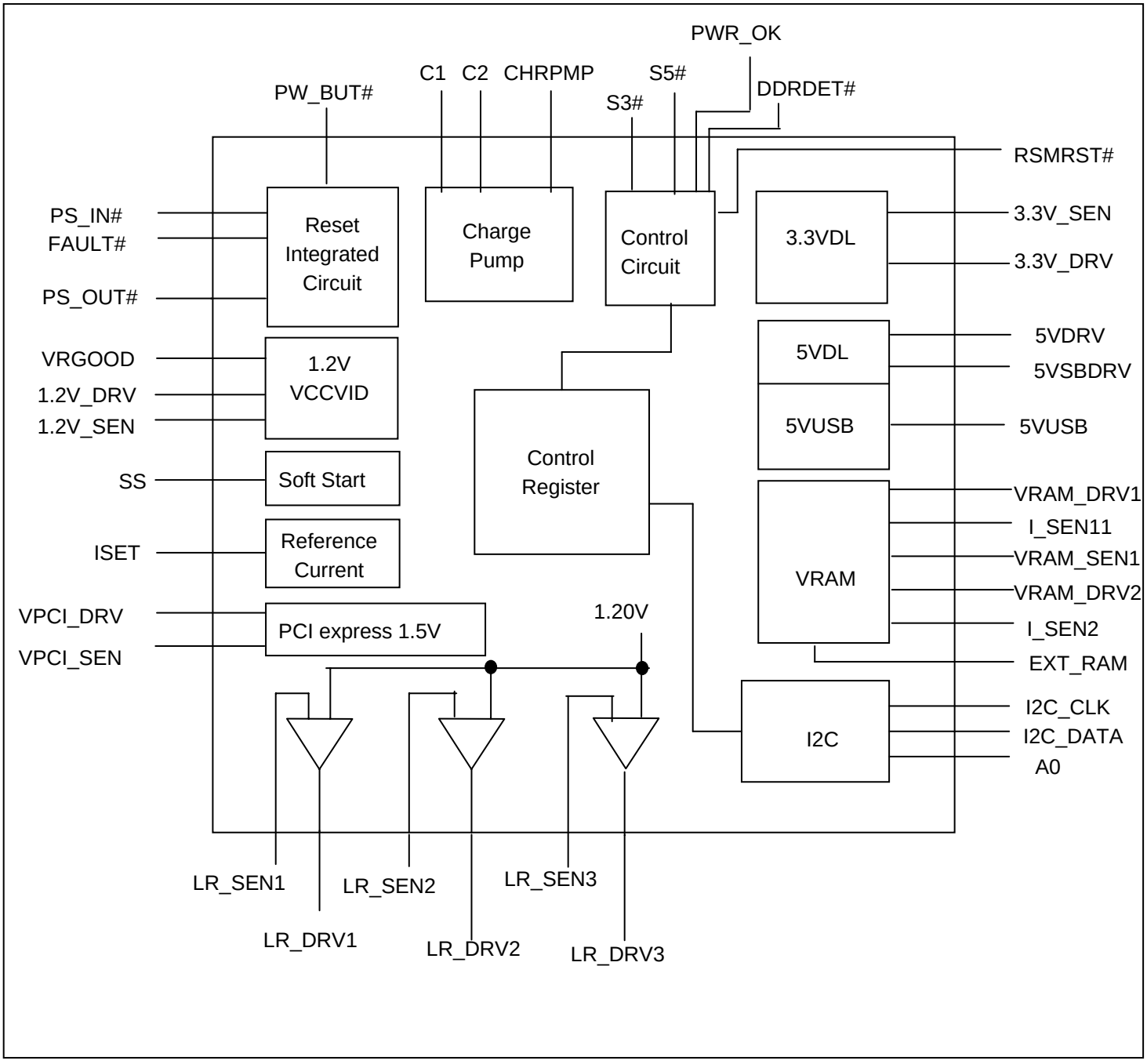
NO	NAME	I/O	FUNCTION DESCRIPTION
1	S3#	I	SYSTEM ACPI CONTROL SIGNALS
2	S5#	I	
3	I2C_DATA	I/O	I2C Interface, and the default ID value are defined as 5CH (0101 110X) as well as 5EH (0101 111X), and X is used to control read/write.
4	I2C_CLK	I	
5	RSMRST#	OD	A signal to indicate 3VDUAL power status. The signal will be issued after 82ms delay when the level of 3VDUAL higher than 2.8V
6	PWM_MODE	I	0=Internal RAM for Linear Mode; 1= external RAM for PWM Mode
7	LR3_SEN	I	Linear Regulators ranging form 1.2V to 5V and can be adjusted by external resistors
8	LR3_DRV	O	
9	AGND	P	Power ground
10	5VUSB	O	Power switch for USB devises provides a programmable Voltage (5VDUAL/5VSTR/ 5VCC) for USB devices. It can be set by register CR00
11	5VSBDRV	O	
12	5VDRV	O	
13	3.3V_SEN	I	3.3VDUAL Voltage regulator
14	3.3VSB_DRV	O	
15	VCC3	P	Power 3.3Vcc
16	SS	I	Soft-Start pin. Attach a capacitor to this pin to determine the soft-start rate; and the slew-rate of SS is set by adjust the capacity of the external capacitor.
17	I_{SET}	I	Attached a specific external resistor to determine the internal reference current.
18	5VSB	P	Power Pin
19	I_SEN2	I	2 channels of V_{STR} output for DDR or DDRII with internal current sharing design to balance the current on the channels. In which I_SEN1 & I_SEN2 pins should be connected together to 5VSB or 3VDUAL if only one channel used. The DDR or DDRII determine by DDRDET#. If DDRDET# =0 VRAM=DDR(2.6V) ; DDRDET#=1 VRAM=DDRII(1.8V).
20	VRAM_DRV2	O	
21	VRAM_SEN	I	
22	I_SEN1	I	
23	VRAM_DRV1	O	
24	AGND	P	Power ground
25	VRGOOD	OD	The signal is applied for the Intel® Northwood CPU using; it's a signal to declare the CPU VID status.

Pin Descriptions, continued

NO	NAME	I/O	FUNCTION DESCRIPTION
26	1.2V_SEN	I	1.2V_{CC} voltage regulator for Intel® P4 CPU application.
27	1.2V_DRV	O	
28	5VSB	P	Power Pin
29	C1	I	Charge pump pins. It supports 10mA driving current and insures output voltage 9V or above.
30	C2	I	
31	CHRPMP	P	
32	AGND	P	Power pin
33	VPCI_DRV	O	1.5V Voltage Regulator for PCI Express. If this power plane won't be used, the VPCI_SEN must be connected to 3VDUAL to avoid the fault trigger of LUV event.
34	VPCI_SEN	I	
35	VCC	P	Power pin
36	LR1_DRV	O	Linear Regulators ranging form 1.2V to 5V and can be adjusted by external resistors
37	LR1_SEN	I	
38	LR2_DRV	O	
39	LR2_SEN	I	
40	DDRDET#	I	A signal to indicate type of DDRRAM that plugged- in; low means 2.6V for DDR and high means 1.8V for DDRII.
41	FAULT#	I	Fault event be monitored; the chip shut the ATX power supply down directly by control the PS_ON# signal as long as the fault events are triggered.
42	PS_IN#		Power on signal. Low active.
43	PW_BUT#	I	System PW_BUT for power sequence monitoring.
44	PS_OUT#	O	Pin to control ATX power supply.
45	DGND	P	Power ground.
46	PWR_OK	I	Power good input signal of ATX power supply.
47	A0	I	I2C address selecting pin.
48	D5VSB	P	Power pin.

*VRGOOD & TYPEDET# can endure 0-12V level voltage.

4. INTERNAL BLOCK DIAGRAM



5. I2C COMMUNICATION PROTOCOL

The W83303AD/AG serial protocol accepts byte write, byte read operation from the controller. For the byte write and byte read operations, the system controller can access individual indexed bytes. The byte write and byte read protocol is outlined in following table. Besides, the slave receiver address is 0101 1110(5Eh).

BYTE WRITE		BYTE READ	
BIT	**DESCRIPTION**	**BIT**	**DESCRIPTION**
1	Start	**1**	Start
2:8	Slave address – 7 bits	**2:8**	Slave address – 7 bits
9	Write	**9**	Write
10	Acknowledge from Slave	**10**	Acknowledge from slave
11:18	Command Code – 8 bits '1xxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	**11:18**	Command Code – 8 bits '1xxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	**19**	Acknowledge from slave
20:27	Data byte – 8 bits	**20**	Repeat start
28	Acknowledge from slave	**21:27**	Slave address – 7bits
29	Stop	**28**	Read
		29	Acknowledge from slave
		30:37	Data byte from slave – 8bits
		38	Not Acknowledge
		39	Stop

6. REGISTER DESCRIPTION

6.1 CR00 (5VUSB Setting Register, Default 0x00h, Read/Write)

BIT1	BIT0	SUPPORT ACPI STATE
0	1	S0, S3
0	0	S0, S3, S5
1	1	S0

6.2 CR01 (VPCI Voltage Setting Register, Default 0x00h, Read/Write)

Bit7~3: Reserved

BIT2	BIT1	BIT0	VAGP OUTPUT
0	0	0	1.50V
0	0	1	1.55V
0	1	0	1.60V
0	1	1	1.65V
1	0	0	1.70V
1	0	1	1.80V
1	1	0	1.90V
1	1	1	2.00V

6.3 CR02 (VRAM Voltage Setting Register, Default x000 0000 b, Read/Write)

Bit7 is reserved for signal DDRDET# Setting (Dynamic detect)

DDRDET#=H bit7=1 DDRII type, DDRDET#=L bit7=0 DDRI type.

Bit3,2, 1 and 0 are applied for DDRRAM output adjusting.

BIT7	BIT3	BIT2	BIT1	BIT0	VRAM OUTPUT
0	0	0	0	0	2.60V
0	0	0	0	1	2.50V
0	0	0	1	0	2.55V
0	0	0	1	1	2.65V
0	0	1	0	0	2.70V
0	0	1	0	1	2.80V
0	0	1	1	0	2.90V
0	0	1	1	1	3.00V
0	1	0	0	0	3.10V
0	1	0	0	1	3.20V

BIT7	BIT3	BIT2	BIT1	BIT0	VRAM OUTPUT
1	0	0	0	1	1.75V
1	0	0	1	0	1.85V
1	0	0	1	1	1.90V
1	0	1	0	0	1.95V
1	0	1	0	1	2.00V
1	0	1	1	0	2.05V
1	0	1	1	1	2.10V
1	1	0	0	0	2.20V
1	1	0	0	1	2.30V

6.4 CR03 (Linear Regulator 1,2 Voltage Setting Register, Default 0x00h, Read/Write)

VLR1: Bit2, 1 and 0 are applied for output voltage adjusting.

BIT2	BIT1	BIT0	PERCENTAGE OF VOLTAGE INCREASE
0	0	0	+0%
0	0	1	+2%
0	1	0	+4%
0	1	1	+8%
1	0	0	+12%
1	0	1	+16%

VLR2 : Bit2, 1 and 0 are applied for output voltage adjusting.

BIT6	BIT5	BIT4	PERCENTAGE OF VOLTAGE INCREASE
0	0	0	+0%
0	0	1	+2%
0	1	0	+4%
0	1	1	+8%
1	0	0	+12%
1	0	1	+16%

6.5 CR04 Chip ID

Power on default [7:0] = 1010,0001 b

Bit	Name	Read/Write	Description
7-0	CHIPID[7:0]	Read Only	Winbond Chip ID number. Read this register will return 0xa1h for W83303AD/AG.

6.6 CR05 (Linear-Under-Voltage Setting Register) default 0x07

Bit0, 1 and 2 are applied for Linear-Under-Voltage Protection functions enable/disable.

BIT0	1/0	Enable/disable VPCI LUV, default value=1
BIT1	1/0	Enable/disable VRAM LUV, default value=1
BIT2	1/0	Enable/disable Dual3.3V LUV, default value=1
BIT3	1/0	Enable/disable RSRMST# restart as release latching fault or LUV event Default value = 0 (disable)
BIT4	1/0	Enable/disable Power Button release latching fault event. Default value = 0 (disable)
BIT5	1/0	Enable/disable Power Button release latching LUV event. Default value = 0 (disable)

6.7 CR06 Version ID

Power on default [7:0] = 0000,0000 b

Bit	Name	Read/Write	Description
7-0	CHIPID[7:0]	Read Only	Winbond Version ID number. Read this register will return 0x00h for W83303AD/AG.

7. ELECTRICAL SPECIFICATION

7.1 AC CHARACTERISTICS

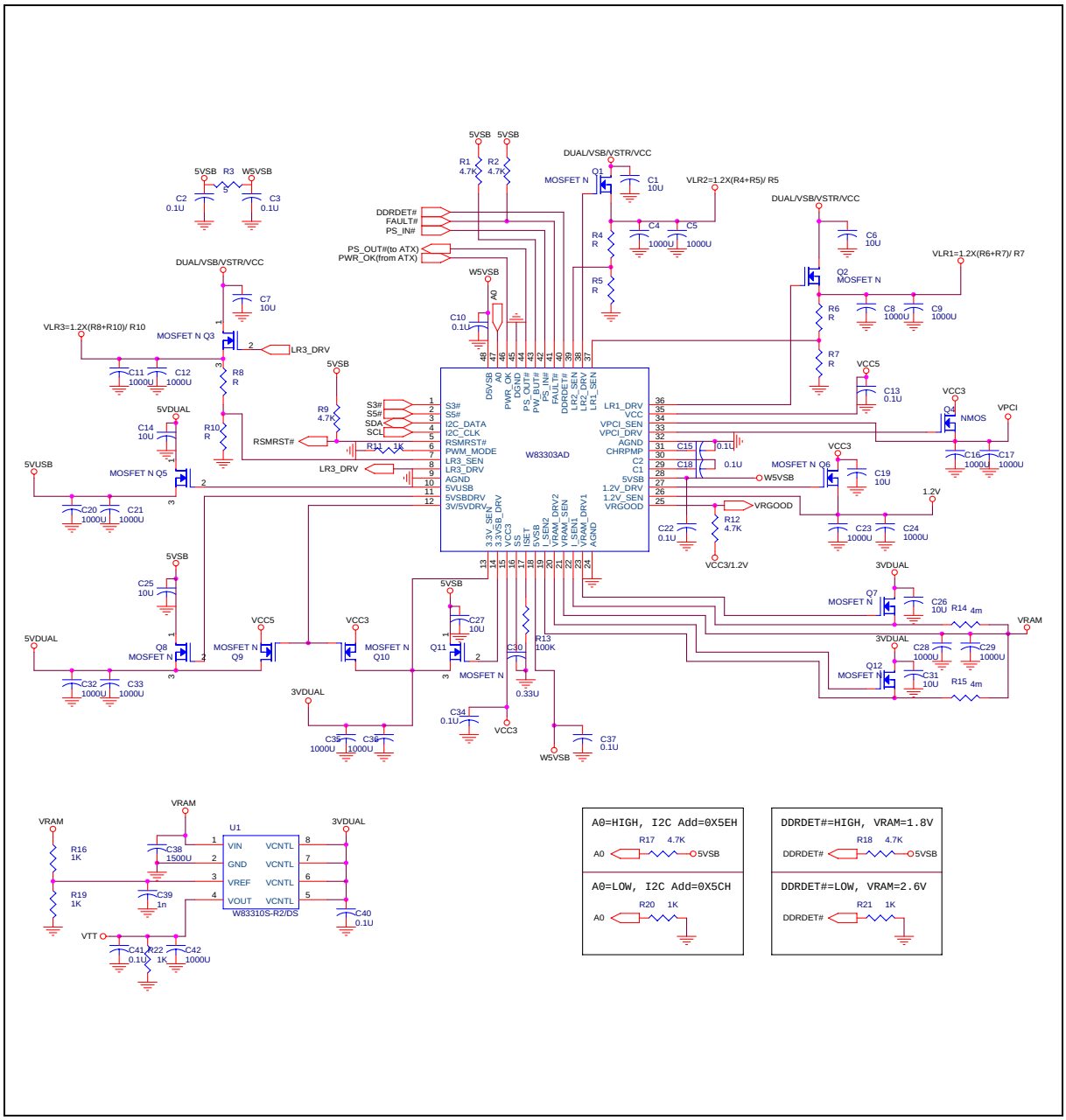
Vcc=5V ±5 %, T_A = 0℃ to +70℃						
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
VPCI Linear Regulator						
Nominal Output Voltage			1.50		V	CR01(bit2~0)=000
Regulation				4	%	
Under-Voltage Falling Threshold			70		%	
VPCI_DRV Output Voltage		8			V	I(VPCI_DRV) < 0.3mA
Vref Voltage Reference						
Nominal Output Voltage		1.152	1.2	1.248		Iload < 1mA
1.2V Linear Regulator						
Nominal Output Voltage		1.152	1.2	1.248	V	
VRGood delay			2		mS	After 1.2V_SEN>1.1V
VRAM Regulator						
Nominal Output Voltage			2.60		V	CR02(bit7)=0
Nominal Output Voltage			1.80		V	CR02(bit7)=1
Regulation				4	%	
Under-Voltage Falling Threshold			70		%	
MAX VRAM_DRV Output Voltage		8			V	I(VRAM_DRV) < 0.3mA
Increase percentage of Linear Regulator _1,2 output voltage (%)						
Nominal Output Voltage			0		%	
Nominal Output Voltage			2		%	
Nominal Output Voltage			4		%	
Nominal Output Voltage			8		%	
Nominal Output Voltage			12		%	
Nominal Output Voltage			16		%	
Soft Start Source current						
Soft start current			20		uA	

AC CHARACTERISTICS, continued

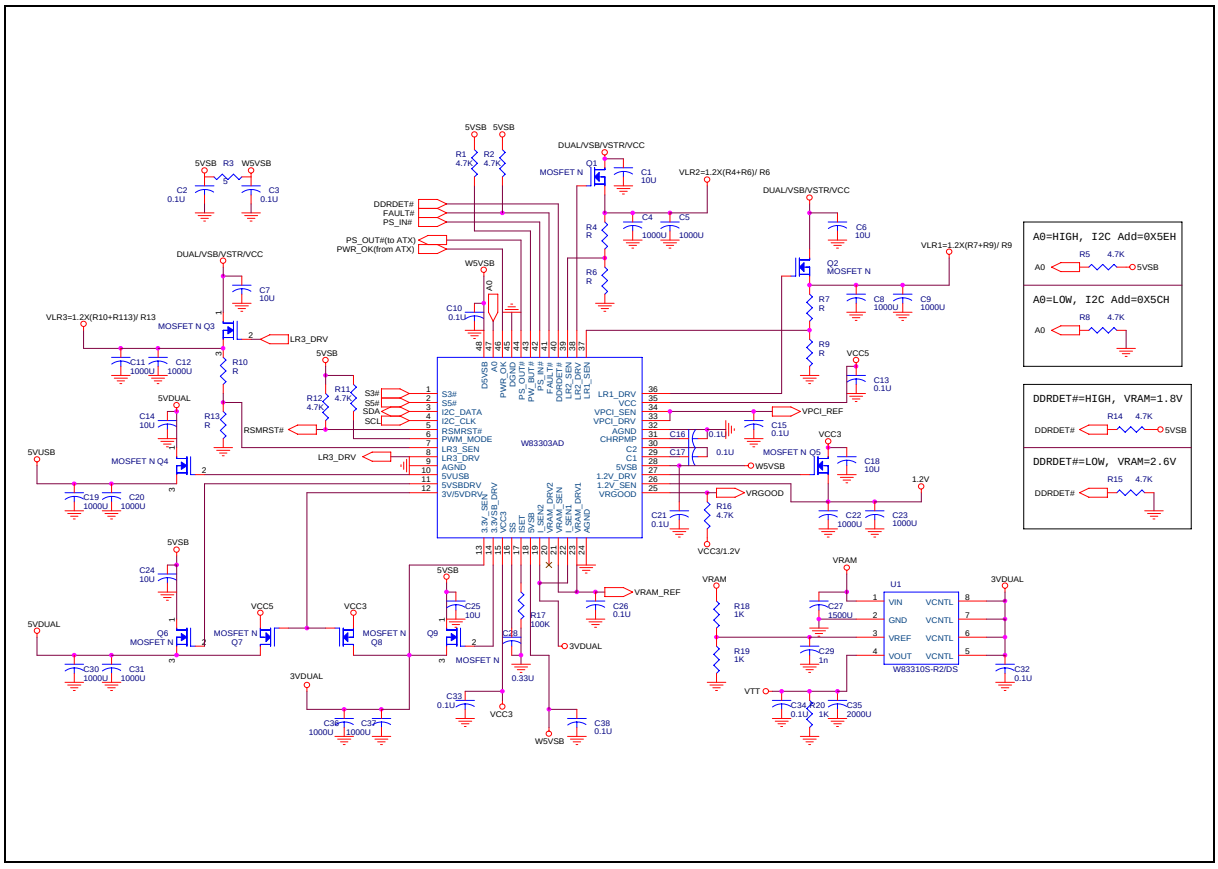
5VDUAL Switch Controller						
5VDRV Output High Voltage		9				Cap Loading
5VSBDRV Output High Voltage		9				Cap Loading
5VUSB Output High Voltage		9				Cap Loading
5VUSB SS Sourcing Current			2.5		uA	@ Soft-start
3.3VDUAL						
Under-Voltage Falling Threshold			70		%	
MAX 3VSBDRV Output Voltage		9			V	I(3VSBDRV) < 0.3mA
Charge Pump						
Charge Pump Frequency			200		KHz	
Charge Pump Voltage		9.5				

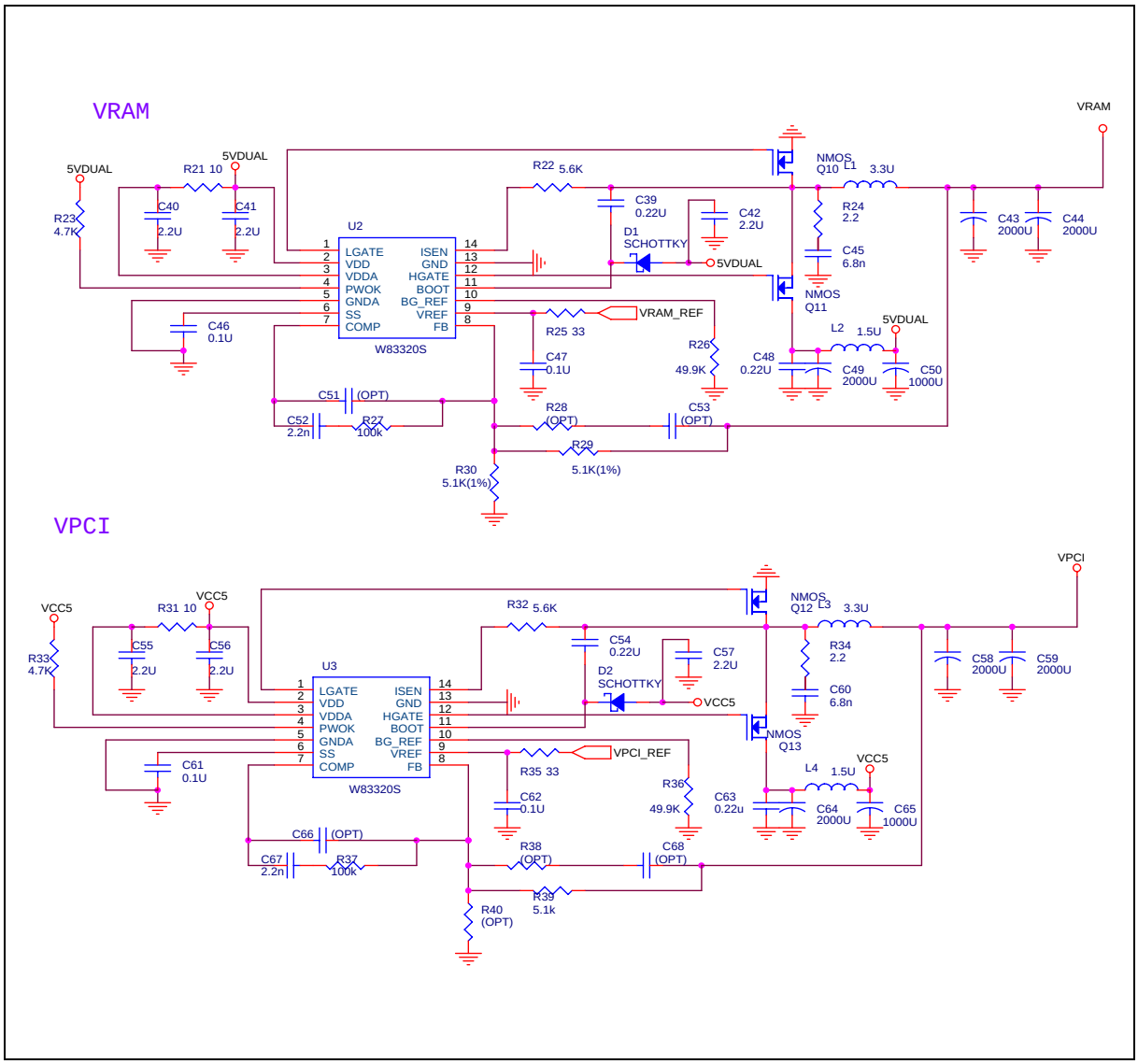
8. APPLICATION CIRCUIT

8.1 Linear Mode



8.2 PWM Mode


W83303AD
A0=HIGH, I2C Add=0X5EH
A0=LOW, I2C Add=0X5CH
DDRDET#=HIGH, VRAM=1.8V
DDRDET#=LOW, VRAM=2.6V
W83310S-R2/DS


VRAM
5VDUAL
R21 10
R23 4.7K
C40 2.2U
C41 2.2U
U2
LGATE
VDD
VDDA
PWOK
GNDA
SS
COMP
ISEN
GND
HGATE
BOOT
BG_REF
VREF
FB
W83320S
C46 0.1U
R22 5.6K
C39 0.22U
D1 SCHOTTKY
C42 2.2U
NMOS Q10
L1 3.3U
R24 2.2
C45 6.8n
NMOS Q11
C43 2000U
C44 2000U
VRAM
VRAM_REF
R25 33
C47 0.1U
R26 49.9K
L2 1.5U
C48 0.22U
C49 2000U
C50 1000U
C51 (OPT)
C52 2.2n
R27 100k
R28 (OPT)
C53 (OPT)
R29 5.1K(1%)
R30 5.1K(1%)
VPCI
VCC5
R31 10
R33 4.7K
C55 2.2U
C56 2.2U
U3
W83320S
C61 0.1U
R32 5.6K
C54 0.22U
D2 SCHOTTKY
C57 2.2U
NMOS Q12
L3 3.3U
R34 2.2
C60 6.8n
NMOS Q13
C58 2000U
C59 2000U
VPCI_REF
R35 33
C62 0.1U
R36 49.9K
L4 1.5U
C63 0.22u
C64 2000U
C65 1000U
C66 (OPT)
C67 2.2n
R37 100k
R38 (OPT)
C68 (OPT)
R39 5.1k
R40 (OPT)

9. ORDERING INSTRUCTION

PART NO.	PACKAGE	REMARKS
W83303AD	48-pin LQFP	
W83303AG	48-pin LQFP	Pb-free package

10. HOW TO READ THE TOP MARKING

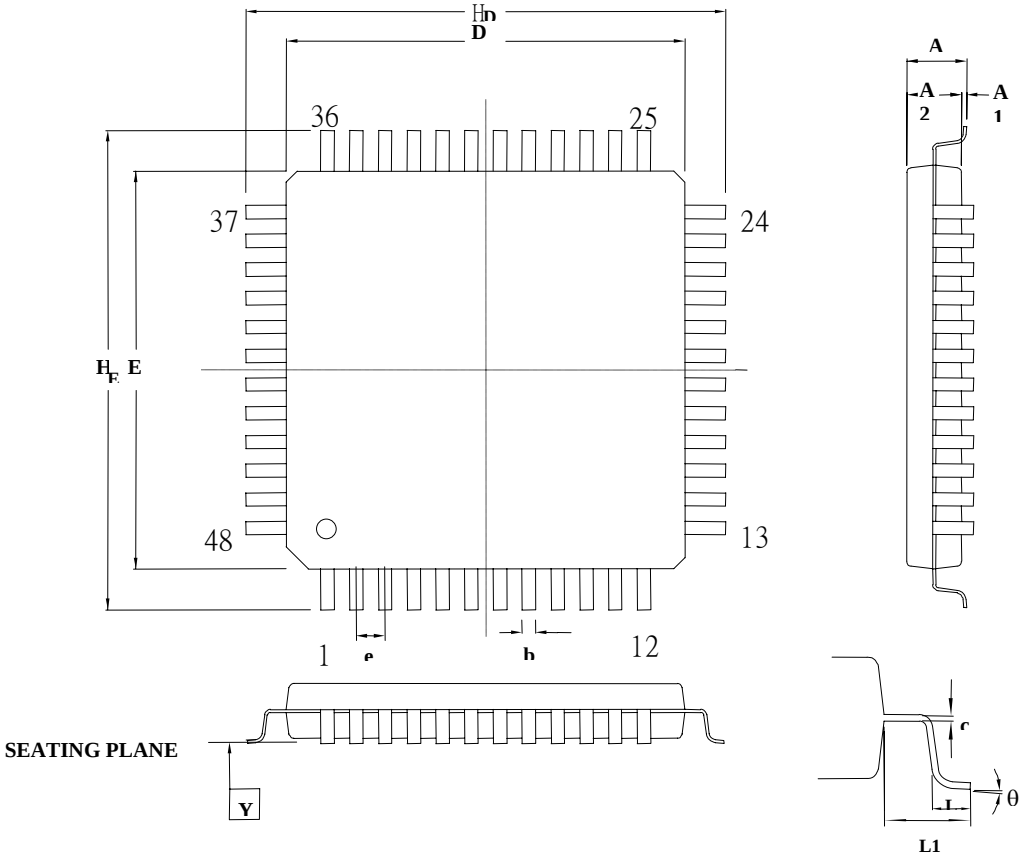




1st Line: Winbond Logo
2nd Line: Part No W83303AD, W83303AG (Pb-free package)
3rd Line: Wafer production serial number
4th Line: tracking code 410GBRA

410：Date code, 410 means package was made in '04 week 10
G：Assembly ID, G means GR, A means ASE…etc.
B：Chip Version, A means version A, B means version B
RA：Winbond internal use

11. PACKAGE DIMENSION



Controlling dimension: Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

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