NCP5424

Dual Synchronous Buck Controller with Input Current Sharing

The NCP5424 is a flexible dual N−Channel synchronous buck controller utilizing $V^{2™}$ control for fast transient response and excellent line and load regulation. This highly versatile controller can be configured as a single two phase output converter that draws programmable amounts of current from two different input voltages or all current from one supply. The NCP5424 can also be configured as two independent out−of−phase controllers.

Using the NCP5424 in a current sharing input configuration is ideal for applications where more power is required than is available from one supply, such as video cards or other plug−in boards. When configured as a dual output controller, the output of one controller can be divided down and used as the reference for the second controller. This tracking capability is useful in applications such as Double Data Rate (DDR) Memory power where the termination voltage must track VDD.

The NCP5424 provides a cycle−to−cycle current limit on Controller 2 allowing the system to handle transient overcurrent events and a hiccup mode overcurrent protection on Controller 1 allowing lossless short circuit protection. In addition, the NCP5424 provides Soft−Start, undervoltage lockout, and built−in adaptive FET nonoverlap time to prevent shoot through.

Features

- Hiccup Mode Current Limit (Controller 1)
- Cycle−to−Cycle Current Limit (Controller 2)
- Programmable Soft−Start
- 100% Duty Cycle for Enhanced Transient Response
- 150 kHz to 600 kHz Programmable Frequency Operation
- Switching Frequency Set by Single Resistor
- Out−Of−Phase Synchronization Between the Channels Reduces the Input Filter Requirement
- Undervoltage Lockout
- Pb−Free Packages are Available*

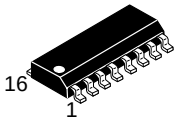
Applications

- Video Graphics Card
- DDR Memory
- High Current (Two−Phase) Power Supplies
- Dual Output DC−DC Converters

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

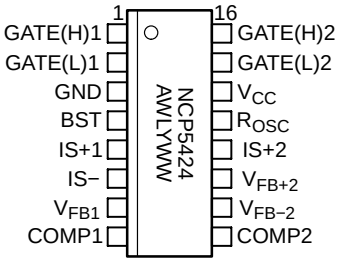
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SOIC−16
D SUFFIX
CASE 751B

PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCP5424D	SOIC−16	48 Units/Rail
NCP5424DG	SOIC−16 (Pb−Free)	48 Units/Rail
NCP5424DR2	SOIC−16	2500 Tape & Reel
NCP5424DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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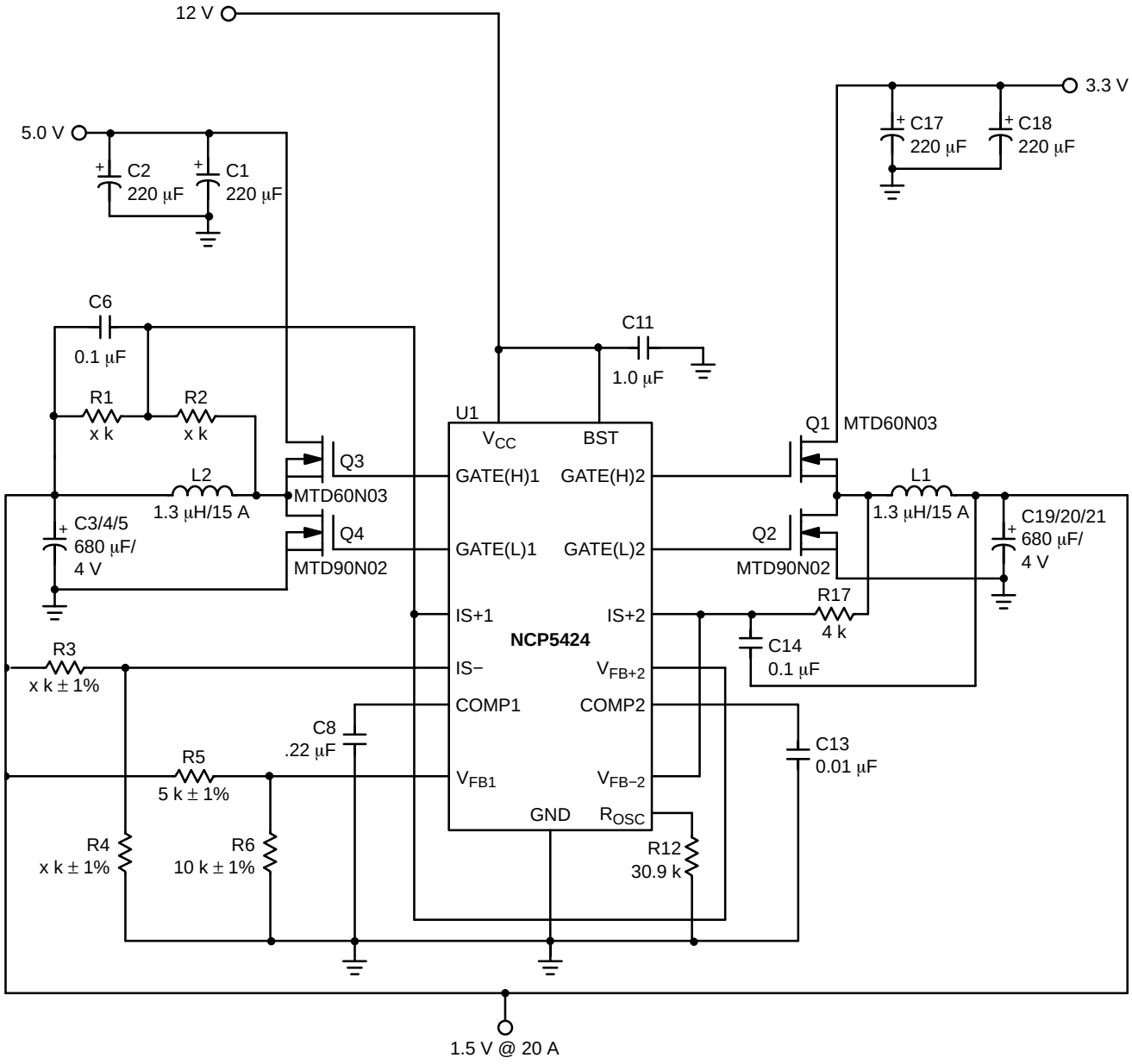


Figure 1. Two−Phase Buck Regulator Application, with Input Current Sharing

MAXIMUM RATINGS

Rating		Value	Unit
Operating Junction Temperature, T_J		150	°C
Storage Temperature Range, T_S		−65 to +150	°C
ESD Susceptibility (Human Body Model)		2.0	kV
Package Thermal Resistance, SOIC−16:	Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	28 115	°C/W °C/W
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
1. 60 second maximum above 183°C.

MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
V_{CC}	IC Power Input	16 V	−0.3 V	N/A	1.5 A peak, 200 mA DC
COMP1, COMP2	Compensation Capacitor for Channel 1 or 2	4.0 V	−0.3 V	1.0 mA	3.5 mA
V_{FB1}, V_{FB+2}, $V_{FB−2}$	Voltage Feedback Input for Channel 1 or 2	5.0 V	−0.3 V	1.0 mA	1.0 mA
BST	Power Input for GATE(H)1, 2	20 V	−0.3 V	N/A	1.5 A peak, 200 mA DC
R_{OSC}	Oscillator Resistor	4.0 V	−0.3 V	1.0 mA	1.0 mA
GATE(H)1, GATE(H)2	High−Side FET Driver for Channel 1 or 2	20 V	−0.3 V	1.5 A peak, 200 mA DC	1.5 A peak, 200 mA DC
GATE(L)1, GATE(L)2	Low−Side FET Driver for Channel 1 or 2	16 V	−0.3 V	1.5 A peak, 200 mA DC	1.5 A peak, 200 mA DC
GND	Ground	0 V	0 V	1.5 A peak, 200 mA DC	N/A
IS+1, IS+2	Positive Current Sense for Channel 1 or 2	6.0 V	−0.3 V	1.0 mA	1.0 mA
IS−	Negative Current Sense for Channels 1 and 2	6.0 V	−0.3 V	1.0 mA	1.0 mA

PACKAGE PIN DESCRIPTION

PIN #	SYMBOL	FUNCTION
1	GATE(H)1	High Side Switch FET driver pin for channel 1.
2	GATE(L)1	Low Side Synchronous FET driver pin for channel 1.
3	GND	Ground pin for all circuitry contained in the IC. This pin is internally bonded to the substrate of the IC.
4	BST	Power input for GATE(H)1 and GATE(H)2 pins.
5	IS+1	Positive input for channel 1 overcurrent comparator.
6	IS−	Negative input for channels 1 and 2 overcurrent comparator.
7	V_{FB1}	Error amplifier inverting input for channel 1.
8	COMP1	Channel 1 Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation. The same capacitor provides Soft−Start timing for channel 1. This pin also disables the channel 1 output when pulled below 0.3 V.
9	COMP2	Channel 2 Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation and Soft−Start timing for channel 2. Channel 2 output is disabled when this pin is pulled below 0.3 V.
10	$V_{FB−2}$	Error amplifier inverting input for channel 2.
11	V_{FB+2}	Error amplifier noninverting input for channel 2.
12	IS+2	Positive input for channel 2 overcurrent comparator.
13	R_{OSC}	Oscillator frequency pin. A resistor from this pin to ground sets the oscillator frequency.
14	V_{CC}	Input Power supply pin.
15	GATE(L)2	Low Side Synchronous FET driver pin for channel 2.
16	GATE(H)2	High Side Switch FET driver pin for channel 2.

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; R_{OSC} = 30.9 k, $C_{COMP1,2}$ = 0.1 μF, 10.8 V < V_{CC} < 13.2 V; 10.8 V < BST < 20 V, $C_{GATE(H)1,2} = C_{GATE(L)1,2}$ = 1.0 nF, V_{FB+2} = 1.0 V; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Error Amplifier					
V_{FB} Bias Current	V_{FBX} = 0 V	−	0.5	1.6	μA
$V_{FB1(2)}$ Input Range	Note 2	0	−	1.1	V
COMP1,2 Source Current	COMP1,2 = 1.2 V to 2.5 V; $V_{FB1(-2)}$ = 0.8 V	15	30	60	μA
COMP1,2 Sink Current	COMP1,2 = 1.2 V; $V_{FB1(-2)}$ = 1.2 V	15	30	60	μA
Reference Voltage 1(2)	COMP1 = V_{FB1}; COMP2 = V_{FB-2}	0.980	1.000	1.020	V
COMP1,2 Max Voltage	$V_{FB1(-2)}$ = 0.8 V	3.0	3.3	−	V
COMP1,2 Min Voltage	$V_{FB1(-2)}$ = 1.2 V	−	0.25	0.35	V
Open Loop Gain	−	−	95	−	dB
Unity Gain Band Width	−	−	40	−	kHz
PSRR @ 1.0 kHz	−	−	70	−	dB
Transconductance	−	−	32	−	mmho
Output Impedance	−	−	2.5	−	MΩ
Input Offset, Error Amp. 2	−	−3.0	0	3.0	mV
Error Amp. 2 Common Mode Range	Note 2	1.75	2.0	−	V
GATE(H) and GATE(L)					
High Voltage (AC)	Measure: V_{CC} − GATE(L)1,2; BST − GATE(H)1,2; Note 2	−	0	0.5	V
Low Voltage (AC)	Measure:GATE(L)1,2 or GATE(H)1,2; Note 2	−	0	0.5	V
Rise Time	1.0 V < GATE(L)1,2 < V_{CC} − 1.0 V 1.0 V < GATE(H)1,2 < BST − 1.0 V, BST ≤ 14 V	−	20	50	ns
Fall Time	V_{CC} − 1.0 > GATE(L)1,2 > 1.0 V BST − 1.0 > GATE(H)1,2 > 1.0 V, BST ≤ 14 V	−	15	50	ns
GATE(H) to GATE(L) Delay	GATE(H)1,2 < 2.0 V, GATE(L)1,2 > 2.0 V BST ≤ 14 V	20	40	70	ns
GATE(L) to GATE(H) Delay	GATE(L)1,2 < 2.0 V, GATE(H)1,2 > 2.0 V; BST ≤ 14 V	20	40	70	ns
GATE(H)1(2) and GATE(L)1(2) pull−down.	Resistance to GND Note 2	50	125	280	kΩ
PWM Comparator					
PWM Comparator Offset	$V_{FB1(-2)}$ = 0 V; Increase COMP1,2 until GATE(H)1,2 starts switching	0.30	0.40	0.50	V
Artificial Ramp	Duty cycle = 50%, Note 2	60	105	150	mV
Minimum Pulse Width	Note 2	−	−	300	ns

2. Guaranteed by design, not 100% tested in production.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; R_{OSC} = 30.9 k, $C_{COMP1,2}$ = 0.1 μF, 10.8 V < V_{CC} < 13.2 V; 10.8 V < BST < 20 V, $C_{GATE(H)1,2} = C_{GATE(L)1,2}$ = 1.0 nF, V_{FB+2} = 1.0 V; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Oscillator					
Switching Frequency	R_{OSC} = 61.9 k; Measure GATE(H)1; Note 3	112	150	188	kHz
Switching Frequency	R_{OSC} = 30.9 k; Measure GATE(H)1	250	300	350	kHz
Switching Frequency	R_{OSC} = 15.1 k; Measure GATE(H)1; Note 3	450	600	750	kHz
R_{OSC} Voltage	R_{OSC} = 30.9 k, Note 3	0.970	1.000	1.030	V
Phase Difference	–	–	180	–	°
Supply Currents					
V_{CC} Current	COMP1,2 = 0 V (No Switching)	–	13	17	mA
BST Current	COMP1,2 = 0 V (No Switching)	–	3.5	6.0	mA
Undervoltage Lockout					
Start Threshold	GATE(H) Switching; COMP1,2 charging	7.8	8.6	9.4	V
Stop Threshold	GATE(H) not switching; COMP1,2 discharging	7.0	7.8	8.6	V
Hysteresis	Start−Stop	0.5	0.8	1.5	V
Hiccup Mode Overcurrent Protection (Controller 1)					
OVC Comparator Offset Voltage	0 V < IS+ 1 < 5.5 V, 0 V < IS− < 5.5 V	55	70	85	mV
Discharge Threshold	–	0.20	0.25	0.30	V
IS+ 1 Bias Current	0 V < IS+ 1 < 5.5 V	−1.0	0.1	1.0	μA
IS− Bias Current	0 V < IS− < 5.5 V	−2.0	0.2	2.0	μA
OVC Common Mode Range	–	0	–	5.5	V
OVC Latch COMP1 Discharge Current	COMP1 = 1.0 V	2.0	5.0	8.0	μA
Cycle−to−Cycle Current Limit (Controller 2)					
OVC Comparator Offset Voltage	0 V < IS+ 2 < 5.5 V, 0 V < IS− < 5.5 V	55	70	85	mV
IS+ 2 Bias Current	0 V < IS+ 2 < 5.5 V	−1.0	0.1	1.0	μA
OVC Common Mode Range	–	0	–	5.5	V
OVC Latch COMP2 Discharge Current	COMP = 1.0 V	0.3	1.2	3.5	mA

3. Guaranteed by design, not 100% tested in production.

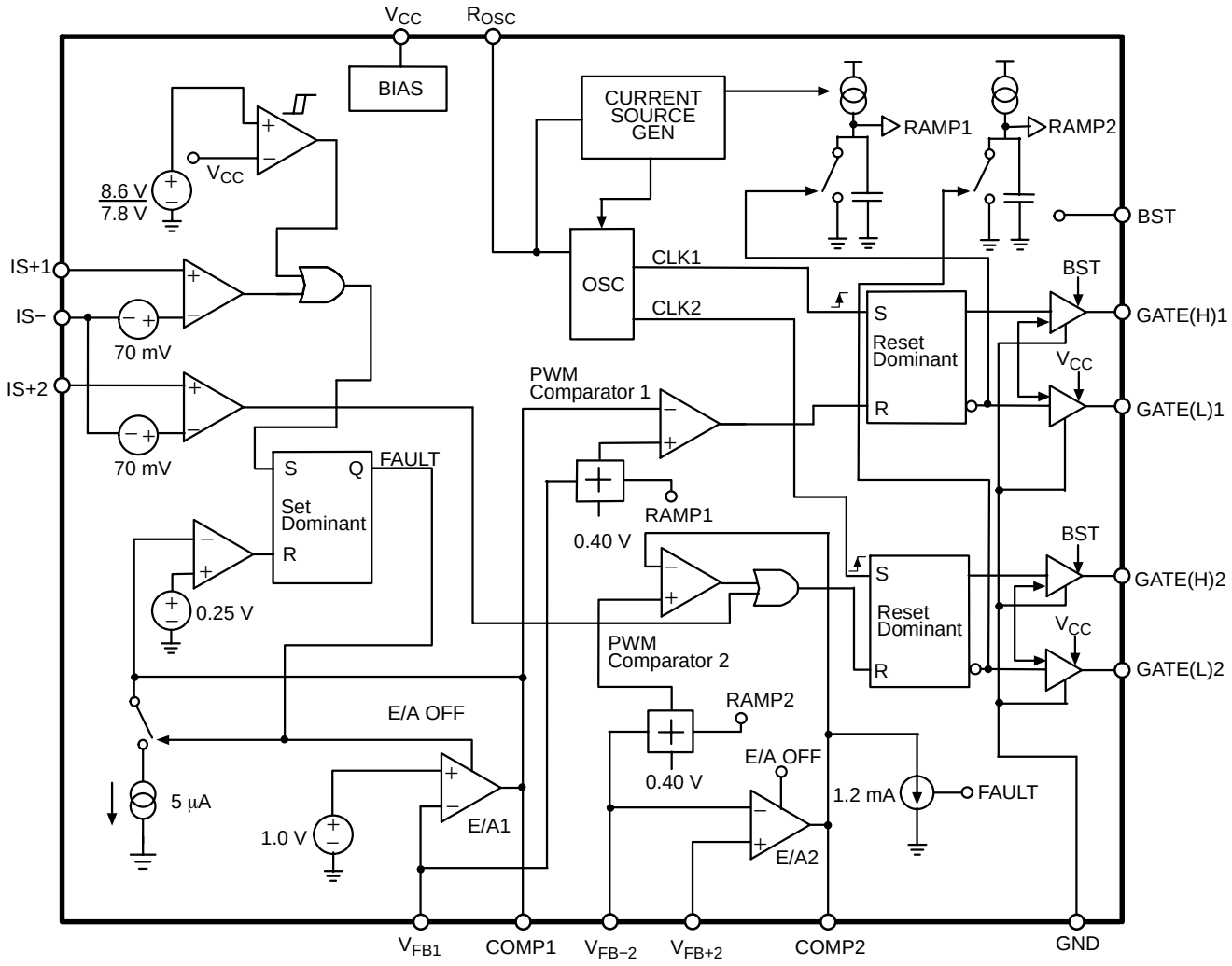


Figure 2. Block Diagram

APPLICATIONS INFORMATION

THEORY OF OPERATION

The NCP5424 is a dual output or single two−phase power supply controller that utilizes the V^2 control method. Two synchronous V^2 buck regulators can be built using a single controller or a single output converter that draws programmable amounts of current from two input voltages. The fixed−frequency architecture, driven from a common oscillator, ensures a 180° phase differential between channels.

V^2 Control Method

The V^2 method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The V^2 method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.

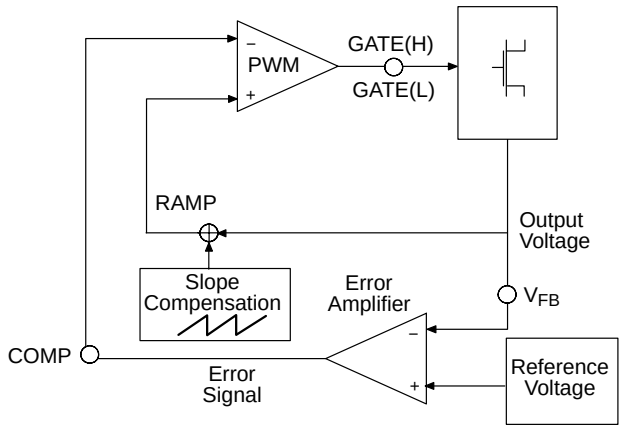


Figure 3. V^2 Control with Slope Compensation

The V^2 control method is illustrated in Figure 3. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch to 0% or 100% duty cycle as required.

A variation in line voltage changes the current ramp in the inductor, which causes the V^2 control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme offers the same advantages in line transient response.

A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction time to the output load step is not related to the crossover frequency of the error signal loop.

The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this ‘slow’ feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation is drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity particularly at higher duty cycle (above 50%).

Start Up

The NCP5424 features a programmable Soft−Start function, which is implemented through the Error Amplifier and the external Compensation Capacitor. This feature prevents stress to the power components and overshoot of the output voltage during start−up. As power is applied to the regulator, the NCP5424 Undervoltage Lockout circuit (UVL) monitors the IC’s supply voltage (V_{CC}). The UVL circuit resets an internal fault latch when the input voltage exceeds 8.6 volts. This fault latch disables the error amplifiers until it is reset. Once the amplifiers are enabled, they start charging the compensation capacitors with a 30 uA constant current that causes a linear voltage ramp. The output of the error amplifier is connected internally to the negative input of the PWM comparator. The comparator’s positive input is connected back to the feedback voltage pin through a 0.45−volt offset. With the feedback voltage starting at zero, the offset voltage forces the comparator high, which prevents resetting the RS latches that control the output drivers. Once the compensation capacitor voltage reaches 0.45 volts, the PWM comparator will switch and

allow a short PWM pulse. This pulse will gradually increase in width as the voltage ramp on the Compensation Capacitor continues to rise. This process will continue until the output voltage reaches the designed value set by the feed back resistors and the parts 1.0−volt reference voltage. Thus the user can determine both Soft−Start and power sequence functions by selecting the compensation capacitors and simply knowing that the amplifiers charge these capacitors with 30 uA and that the threshold for starting PWM pulses is 0.45 volts.

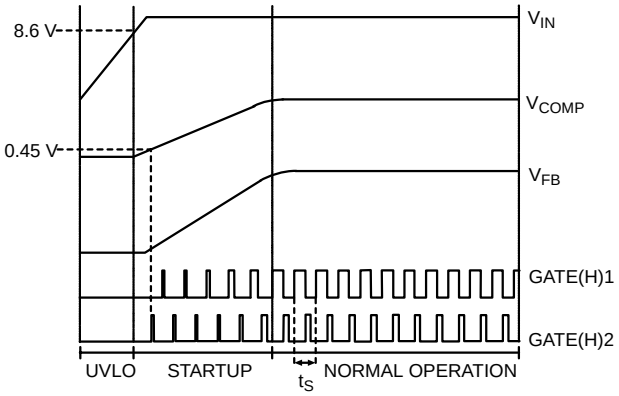


Figure 4. Idealized Waveforms

Normal Operation

During normal operation, the duty cycle of the gate drivers remains approximately constant as the V^2 control loop maintains the regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

Zero Current Start Up in Single Output Shared Input Current Applications

One problem that occurs with dual controllers when connected as a single output is that reverse currents can occur during zero load conditions. As the two controllers start up and start delivering current, if there is no load a reverse current will develop in the inductor of controller 2 that is equal and opposite the current in the controller 1 inductor. When the controller 2 starts to deliver power this reverse current will flow backwards through the top FET back into the supply. In the extreme this can cause the supply to over voltage and/or shut down. Fortunately, there are several ways to deal with this problem. One is to simply insure the part has a minimum load. Another is illustrated in Figure 5, where a diode and voltage divider biases the controller 2 Compensation Capacitor above the 0.45 V Soft−Start threshold, such that the controller starts switching without a soft−start delay. The effect of this is to eliminate the buildup of negative currents that arise during a long start interval where the bottom FET of controller 2 is on. For applications where there are two outputs, this problem can not occur.

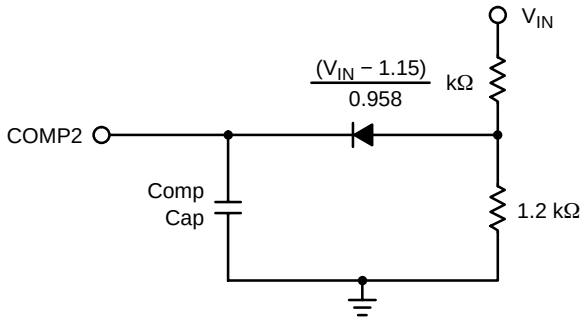


Figure 5. Preventing Reverse Current

Gate Charge Effect on Switching Times

When using the onboard gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading, according to the following graphs.

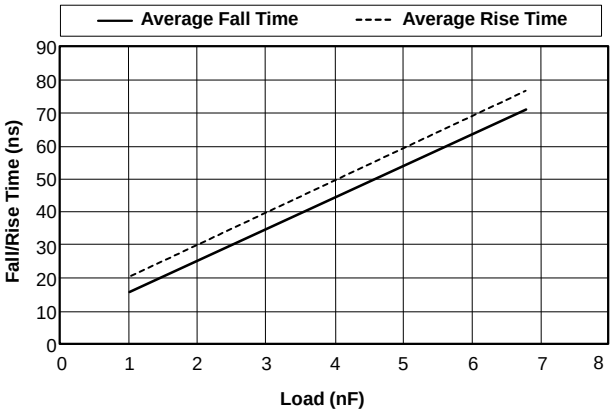


Figure 6. Average Rise and Fall Times

Transient Response

The 150 ns reaction time of the control loop provides fast transient response to any variations in input voltage and output current. Pulse−by−pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, several high frequency and bulk output capacitors are usually used.

Out−of−Phase Synchronization

In out−of−phase synchronization, the turn−on of the second channel is delayed by half the switching cycle. This delay is supervised by the oscillator, which supplies a clock signal to the second channel which is 180° out of phase with the clock signal of the first channel.

The advantages of out−of−phase synchronization are many. Since the input current pulses are interleaved with one another, the overlap time is reduced. The effect of this overlap reduction is to reduce the input filter requirement, allowing the use of smaller components. In addition, since peak current occurs during a shorter time period, emitted EMI is also reduced, thereby reducing shielding requirements.

Overvoltage Protection

Overvoltage Protection (OVP) is provided as a result of the normal operation of the V^2 control method and requires no additional external components. The control loop responds to an overvoltage condition within 150 ns, turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage preventing damage to the load. The regulator remains in this state until the overvoltage condition ceases.

Input Current Sharing

In contemporary high−end applications, part of a system may require more power than is available from one supply. The NCP5424 dual controller can address this requirement in two ways.

In many cases, it is sufficient to be able to set the input power sharing as a ratio so that one source always supplies a certain percentage of the total. This is achieved by having the Error Amplifier inputs from Slave side, Controller Two, brought to external pins so its' reference is available. Current information from the Master, Controller One, provides a reference for the Slave. Current information from the Slave is fed back to the error amplifier's inverting input. The Slave will try to adjust its current to match the current information fed to its reference input from the Master. If this information is 1/2 the voltage developed across the Master's output inductor, the Slave will run at half current and supply a percentage, nominally 33% in this case, of the total current.

In other applications however, the user may not only wish to draw a percentage of power from one source, but also may need to limit the power drawn from that source. The Slave has a Cycle−By−Cycle current limit. In this case, the Slave can be programmed to budget the maximum input power. For example, a designer may wish to draw equal amounts of power from two 5−volt sources, but only 2 amps are available from one of the supplies. In this case, the dual controller will draw equally from the two sources up to a total of 4 amps. At this point, the Slave controller goes into current limit and draws no more than its preset budget. The Master continues to supply the remaining output current up to the maximum that the application requires.

Current Limiting

The NCP5424 employs two types of current limits. Controller One has a Hiccup Mode Current Limit and Controller Two has Cycle−By−Cycle current limit. Any overcurrent condition on Controller One results in the immediate shutdown of both output phases. In a dual output application, independent current limits are not supported.

The NCP5424 has two current limiting amplifiers that have a built in 70 mV offset. These differential amplifiers have a common mode range from zero to 5.5 volts and low input current. They share a common negative input that in single output voltage application is not a limitation. However in dual output applications independent current limits are not supported.

Once a voltage greater than 70 mV is applied to the current limiting amplifier of Controller 2; it produces an output that, as shown in the block diagram, resets the output RS flip flop. This ends the PWM pulse for the particular cycle and in so doing, limits the energy delivered to the load on a cycle−by−cycle basis. One advantage of this current limiting scheme is that the NCP5424 will limit transient currents and will resume normal operation the cycle after the transient goes away.

A second benefit is that this action of limiting the PWM pulse width means that in an input power sharing application, one controller can be current limiting while the other supplies the remaining current needs.

The fault latch immediately turns off the error amplifier and discharges both COMP capacitors. The capacitor connected to COMP1 is discharged through a 5.0 μA current sink in order to provide timing for the reset cycle. When COMP1 has fallen below 0.25 V, a comparator resets the fault latch and error amplifier 1 begins to charge COMP1 with a 30 μA source current. When COMP1 exceeds the feedback voltage plus the PWM Comparator offset voltage, the normal switching cycle will resume. If the short circuit condition persists through the restart cycle, the overcurrent reset cycle will repeat itself until the short circuit is removed, resulting in small "hiccup" output pulses while the COMP capacitor charges and discharges. Please see the section titled "Current Sharing Compensation Capacitor Selection" for proper Comp capacitor selection.

Cycle−By−Cycle current limit controls the amount of current available from Controller 2. Controller 2 has a current limiting comparator that, by truncating the respective controller's PWM pulse width, limits the available current on a pulse−by−pulse basis. This comparator has a built in 70 mV offset that provides a reference for setting current limit.

Output Enable

On/Off control of the regulator outputs can be implemented by pulling the COMP pins low. The COMP pins must be driven below the 0.40 V PWM comparator offset voltage in order to disable the switching of the GATE drivers.

DESIGN GUIDELINES

Definition of the design specifications

The output voltage tolerance can be affected by any or all of the following:

1. buck regulator output voltage setpoint accuracy;
2. output voltage change due to discharging or charging of the bulk decoupling capacitors during a load current transient;
3. output voltage change due to the ESR and ESL of the bulk and high frequency decoupling capacitors, circuit traces, and vias;
4. output voltage ripple and noise.

Budgeting the tolerance is left to the designer who must consider all of the above effects and provide an output voltage that will meet the specified tolerance at the load.

The designer must also ensure that the regulator component temperatures are kept within the manufacturer's specified ratings at full load and maximum ambient temperature.

Selecting Feedback Divider Resistors

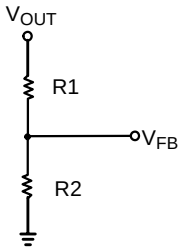


Figure 7. Selecting Feedback Divider Resistors

The feedback pins ($V_{FB1(2)}$) are connected to external resistor dividers to set the output voltages. The error amplifier is referenced to 1.0 V and the output voltage is determined by selecting resistor divider values. Resistor R1 is selected based on a design trade−off between efficiency and output voltage accuracy. The output voltage error can be estimated due to the bias current of the error amplifier neglecting resistor tolerance:

$$\text{Error\%} = \frac{1 \times 10^{-6} \times R1}{1} \times 100\%$$

R2 can be sized after R1 has been determined:

$$R2 = R1\left(\frac{V_{OUT}}{1} - 1\right)$$

Calculating Duty Cycle

The duty cycle of a buck converter (including parasitic losses) is given by the formula:

$$\text{Duty Cycle} = D = \frac{V_{OUT} + (V_{HFET} + V_L)}{V_{IN} + V_{LFET} - V_{HFET} - V_L}$$

where:

V_{OUT} = buck regulator output voltage;
V_{HFET} = high side FET voltage drop due to $R_{DS(ON)}$;
V_L = output inductor voltage drop due to inductor wire DC resistance;
V_{IN} = buck regulator input voltage;
V_{LFET} = low side FET voltage drop due to $R_{DS(ON)}$.

Selecting the Switching Frequency

Selecting the switching frequency is a trade−off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower frequency operation because a higher frequency results in lower efficiency due to MOSFET gate charge losses. Additionally, the use of smaller inductors at higher frequencies results in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents.

The value of the oscillator resistor is designed to be linearly related to the switching period. If the designer prefers not to use Figure 8 to select the necessary resistor, the following equation quite accurately predicts the proper resistance for room temperature conditions.

$$R_{OSC} = \frac{21700 - f_{SW}}{2.31 f_{SW}}$$

where:

R_{OSC} = oscillator resistor in kΩ;
f_{SW} = switching frequency in kHz.

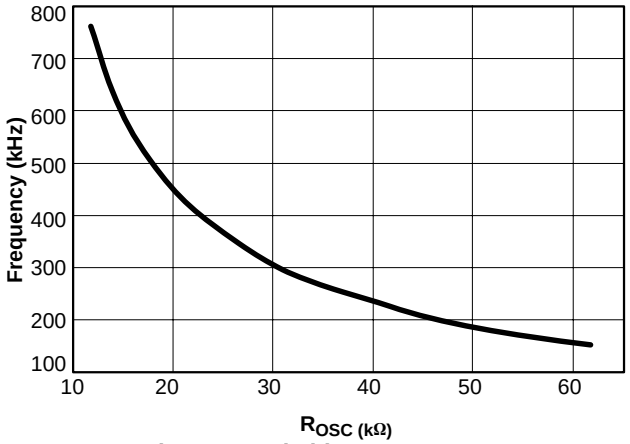


Figure 8. Switching Frequency

Selection of the Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. There are many factors to consider in selecting the inductor including cost, efficiency, EMI and ease of manufacture. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss.

There are a variety of materials and types of magnetic cores that could be used for this application. Among them are ferrites, molypermalloy cores (MPP), amorphous and powdered iron cores. Powdered iron cores are very

commonly used. Powdered iron cores are very suitable due to its high saturation flux density and have low loss at high frequencies, a distributed gap and exhibit very low EMI.

The minimum value of inductance which prevents inductor saturation or exceeding the rated FET current can be calculated as follows:

$$L_{MIN} = \frac{(V_{IN(MIN)} - V_{OUT})V_{OUT}}{f_{SW} \times V_{IN(MIN)} \times I_{SW(MAX)}}$$

where:

L_{MIN} = minimum inductance value;
$V_{IN(MIN)}$ = minimum design input voltage;
V_{OUT} = output voltage;
f_{SW} = switching frequency;
$I_{SW(MAX)}$ − maximum design switch current.

The inductor ripple current can then be determined:

$$\Delta I_L = \frac{V_{OUT} \times (1 - D)}{L \times f_{SW}}$$

where:

ΔI_L = inductor ripple current;
V_{OUT} = output voltage;
L = inductor value;
D = duty cycle.
f_{SW} = switching frequency

The designer can now verify if the number of output capacitors will provide an acceptable output voltage ripple (1.0% of output voltage is common). The formula below is used:

$$\Delta I_L = \frac{\Delta V_{OUT}}{ESR_{MAX}}$$

Rearranging we have:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_L}$$

where:

ESR_{MAX} = maximum allowable ESR;
$\Delta V_{OUT} = 1.0\% \times V_{OUT}$ = maximum allowable output voltage ripple (budgeted by the designer);
ΔI_L = inductor ripple current;
V_{OUT} = output voltage.

The number of output capacitors is determined by:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).

The designer must also verify that the inductor value yields reasonable inductor peak and valley currents (the inductor current is a triangular waveform):

$$I_{L(PEAK)} = I_{OUT} + \frac{\Delta I_L}{2}$$

where:

$I_{L(PEAK)}$ = inductor peak current;
I_{OUT} = load current;
ΔI_L = inductor ripple current.

$$I_{L(VALLEY)} = I_{OUT} - \frac{\Delta I_L}{2}$$

where:

$I_{L(VALLEY)}$ = inductor valley current.

Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$\Delta V_{OUT} = \Delta I_{OUT} \times \left(\frac{ESL}{\Delta t} + ESR + \frac{t_{TR}}{C_{OUT}}\right)$$

where:

$\Delta I_{OUT} / \Delta t$ = load current slew rate;
ΔI_{OUT} = load transient;
Δt = load transient duration time;
ESL = Maximum allowable ESL including capacitors, circuit traces, and vias;
ESR = Maximum allowable ESR including capacitors and circuit traces;
t_{TR} = output voltage transient response time.

The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

where:

ΔV_{ESR} = change in output voltage due to ESR (assigned by the designer)

Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).
ESR_{MAX} = maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$\Delta V_{ESR} = \Delta I_{OUT} \times ESR_{MAX}$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$ESL_{MAX} = \frac{\Delta V_{ESL} \times \Delta t}{\Delta I}$$

Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$L_{IN} = \frac{\Delta V}{(dI/dt)_{MAX}}$$

where:

L_{IN} = input inductor value;

ΔV = voltage seen by the input inductor during a full load swing;

$(dI/dt)_{MAX}$ = maximum allowable input current slew rate.

The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double−pole network with a slope of −2.0, a roll−off rate of −40 dB/dec, and a corner frequency:

$$f_C = \frac{1}{2\pi \times \sqrt{LC}}$$

where:

L = input inductor;

C = input capacitor(s).

SELECTION OF THE POWER FET

FET Basics

The use of a MOSFET as a power switch is compelled by two reasons: 1) *high input impedance*; and 2) *fast switching times*. The electrical characteristics of a MOSFET are considered to be nearly those of a perfect switch. Control and drive circuitry power is therefore reduced. Because the input impedance is so high, it is voltage driven. The input of the MOSFET acts as if it were a small capacitor, which the driving circuit must charge at turn on. The lower the drive impedance, the higher the rate of rise of V_{GS}, and the faster the turn−on time. Power dissipation in the switching MOSFET consists of 1) conduction losses, 2) leakage losses, 3) turn−on switching losses, 4) turn−off switching losses, and 5) gate−transitions losses. The latter three losses are proportional to frequency.

The most important aspect of FET performance is the Static Drain−To−Source On−Resistance ($R_{DS(ON)}$), which affects regulator efficiency and FET thermal management requirements. The On−Resistance determines the amount of current a FET can handle without excessive power dissipation that may cause overheating and potentially catastrophic failure. As the drain current rises, especially above the continuous rating, the On−Resistance also increases. Its positive temperature coefficient is between +0.6%/°C and +0.85%/°C. The higher the On−Resistance the larger the conduction loss is. Additionally, the FET gate charge should be low in order to minimize switching losses and reduce power dissipation.

Both logic level and standard FETs can be used.

Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail−to−rail due to overshoot caused by the capacitive load they present to the controller IC.

Selection of the Switching (Upper) FET

The designer must ensure that the total power dissipation in the FET switch does not cause the power component's junction temperature to exceed 150°C.

The maximum RMS current through the switch can be determined by the following formula:

$$I_{RMS(H)} = \sqrt{\frac{\left[I_{L(PEAK)}^2 + (I_{L(PEAK)} \times I_{L(VALLEY)}) + I_{L(VALLEY)}^2 \times D\right]}{3}}$$

where:

$I_{RMS(H)}$ = maximum switching MOSFET RMS current;

$I_{L(PEAK)}$ = inductor peak current;

$I_{L(VALLEY)}$ = inductor valley current;

D = duty cycle.

Once the RMS current through the switch is known, the switching MOSFET conduction losses can be calculated:

$$P_{RMS(H)} = I_{RMS(H)}^2 \times R_{DS(ON)}$$

where:

$P_{RMS(H)}$ = switching MOSFET conduction losses;

$I_{RMS(H)}$ = maximum switching MOSFET RMS current;

$R_{DS(ON)}$ = FET drain−to−source on−resistance

The upper MOSFET switching losses are caused during MOSFET switch−on and switch−off and can be determined by using the following formula:

$$P_{SWH} = P_{SWH(ON)} + P_{SWH(OFF)} = \frac{V_{IN} \times I_{OUT} \times (t_{RISE} + t_{FALL})}{6T}$$

where:

$P_{SWH(ON)}$ = upper MOSFET switch−on losses;

$P_{SWH(OFF)}$ = upper MOSFET switch−off losses;

V_{IN} = input voltage;

I_{OUT} = load current;

t_{RISE} = MOSFET rise time (from FET manufacturer's switching characteristics performance curve);

t_{FALL} = MOSFET fall time (from FET manufacturer's switching characteristics performance curve);

$T = 1/f_{SW}$ = period.

The total power dissipation in the switching MOSFET can then be calculated as:

$$P_{HFET(TOTAL)} = P_{RMS(H)} + P_{SWH(ON)} + P_{SWH(OFF)}$$

where:

$P_{HFET(TOTAL)}$ = total switching (upper) MOSFET losses;

$P_{RMS(H)}$ = upper MOSFET switch conduction Losses;

$P_{SWH(ON)}$ = upper MOSFET switch−on losses;

$P_{SWH(OFF)}$ = upper MOSFET switch−off losses;

Once the total power dissipation in the switching FET is known, the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + [P_{HFET(TOTAL)} \times R_{\theta JA}]$$

where:

T_J = FET junction temperature;

T_A = ambient temperature;

$P_{HFET(TOTAL)}$ = total switching (upper) FET losses;

$R_{\theta JA}$ = upper FET junction−to−ambient thermal resistance.

Selection of the Synchronous (Lower) FET

The switch conduction losses for the lower FET can be calculated as follows:

$$P_{RMS(L)} = I_{RMS}^2 \times R_{DS(ON)} = [I_{OUT} \times \sqrt{(1 - D)}]^2 \times R_{DS(ON)}$$

where:

$P_{RMS(L)}$ = lower MOSFET conduction losses;

I_{OUT} = load current;

D = Duty Cycle;

$R_{DS(ON)}$ = lower FET drain−to−source on−resistance.

The synchronous MOSFET has no switching losses, except for losses in the internal body diode, because it turns on into near zero voltage conditions. The MOSFET body diode will conduct during the non−overlap time and the resulting power dissipation (neglecting reverse recovery losses) can be calculated as follows:

$$P_{SWL} = V_{SD} \times I_{LOAD} \times \text{non−overlap time} \times f_{SW}$$

where:

P_{SWL} = lower FET switching losses;

V_{SD} = lower FET source−to−drain voltage;

I_{LOAD} = load current;

Non−overlap time = GATE(L)−to−GATE(H) or GATE(H)−to−GATE(L) delay (from NCP5424 data sheet Electrical Characteristics section);

f_{SW} = switching frequency.

The total power dissipation in the synchronous (lower) MOSFET can then be calculated as:

$$P_{LFET(TOTAL)} = P_{RMS(L)} + P_{SWL}$$

where:

$P_{LFET(TOTAL)}$ = Synchronous (lower) FET total losses;

$P_{RMS(L)}$ = Switch Conduction Losses;

P_{SWL} = Switching losses.

Once the total power dissipation in the synchronous FET is known the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + [P_{LFET(TOTAL)} \times R_{\theta JA}]$$

where:

T_J = MOSFET junction temperature;

T_A = ambient temperature;

$P_{LFET(TOTAL)}$ = total synchronous (lower) FET losses;

$R_{\theta JA}$ = lower FET junction−to−ambient thermal resistance.

Control IC Power Dissipation

The power dissipation of the IC varies with the MOSFETs used, V_{CC}, and the NCP5424 operating frequency. The average MOSFET gate charge current typically dominates the control IC power dissipation.

The IC power dissipation is determined by the formula:

$$P_{CONTROL(IC)} = I_{CC1}V_{CC1} + I_{BST}V_{BST} + P_{GATE(H)1} + P_{GATE(L)1} + P_{GATE(H)2} + P_{GATE(L)2}$$

where:

$P_{CONTROL(IC)}$ = control IC power dissipation;

I_{CC1} = IC quiescent supply current;

V_{CC1} = IC supply voltage;

$P_{GATE(H)}$ = upper MOSFET gate driver (IC) losses;

$P_{GATE(L)}$ = lower MOSFET gate driver (IC) losses.

The upper (switching) MOSFET gate driver (IC) losses are:

$$P_{GATE(H)} = Q_{GATE(H)} \times f_{SW} \times V_{BST}$$

where:

$P_{GATE(H)}$ = upper MOSFET gate driver (IC) losses;

$Q_{GATE(H)}$ = total upper MOSFET gate charge at V_{CC};

f_{SW} = switching frequency;

The lower (synchronous) MOSFET gate driver (IC) losses are:

$$P_{GATE(L)} = Q_{GATE(L)} \times f_{SW} \times V_{CC}$$

where:

$P_{GATE(L)}$ = lower MOSFET gate driver (IC) losses;

$Q_{GATE(L)}$ = total lower MOSFET gate charge at V_{CC};

f_{SW} = switching frequency;

The junction temperature of the control IC is primarily a function of the PCB layout, since most of the heat is removed through the traces connected to the pins of the IC.

Selection of the Current Sharing Ratio

When the two controllers are connected together as a single output two−phase Buck Converter, the two controllers are in a Master−Slave configuration. The Slave controller on the right side of Figure 1 tries to follow information provided by the Master controller, on the left. The circuit uses inductor current sensing, in which the parasitic resistance (LSR) of the controller's output chokes are used as a current sensing element. On the Slave side (Controller Two), both Error Amplifier inputs are brought to external pins so the reference is available. The RC network in parallel with the output inductor on the Master side (Controller One) generates the reference for the Slave. Current information from the Slave is fed back to the error amplifier's inverting input. In this configuration, the Slave tries to adjust its current to match the current information fed to its reference input from the Master Controller. In Figure 1, R1, R2 and C6 are used to generate the Slave's reference. R17 and C14 generate the Slave's inverting input signal. If 50−50 current sharing is needed, then only R2 and C6 are required to generate the reference signal. The values for both sides should be calculated with the following equation.

$$R = \frac{L}{C6 \cdot RL}$$

where:

L = Inductor value, both Controllers should use the same inductor.

RL = Internal resistance of L, from inductor data sheet.

C6 = Select a value such that R < 15 kΩ.

With the RC time constant selected to equal the L/R_L time constant, the voltage across the capacitor will be equal to the voltage drop across the internal resistance of the inductor. For proper sharing, the inductors on both sides should be the same.

If a ratio other than 50−50 is needed, the R and C values of the inverting signal filter are calculated using the previous equation. Since the reference signal has to be divided down to the proper ratio, R1 is required. Using the same capacitance value, the following equation is used to calculate the proper values for the reference filter.

$$R2 = \frac{R1(1 - Ratio)}{Ratio}$$

where:

R1 = Chosen Value, 10 kΩ is recommended.

$$Ratio = \frac{\%slave}{\%master}, \text{ input power ratio}$$

To ensure greater accuracy, the equivalent parallel resistance of R1 and R2 should be greater or equal to the value R17, the resistance value calculated for the inverting signal.

$$R17 \leq \frac{R1 \cdot R2}{R1 + R2}$$

R17 = The inverting signal filter resistance.

Current Sharing Errors

The three main errors in current sharing arise from board layout imbalances, inductor mismatch, and input offsets in the error amplifiers. The first two sources of error can be controlled through careful component selection and good layout practice. With a 4.0 mΩ inductor, for example, one mV of input offset error will represent .25 A of error. One way to diminish this effect is to use higher resistance inductors but the penalty is higher power losses in the inductors. Fortunately, the input offset of the NCP5424 is low so that this error term is reduced.

Current Sharing Compensation Capacitor Selection

The NCP5424 is designed for single and dual output applications. Therefore the IC needs two separate compensation capacitors for the dual output designs, which is not desirable for a single output design. With two compensation capacitors, a race condition between the master and slave controllers is created. During start−up or upon leaving Hiccup mode, the Master's Error Amplifier starts charging Comp1. When Comp1 reaches 0.40 V, both controllers begin to regulate the output. The Slave Controller voltage reference is generated externally by the Master's output, while the Master has an internal 1.0 V reference. Since Comp2 does not start charging until Comp1 reaches 0.40 V, the Slave's PWM inverting input is lower than its Vfb−2 input causing a reset of the Slave Controller output driver. Gate(L)2 turns on, sinking current from the output, while the Master's output driver is set turning Gate(H)1 on and sourcing current to the output (since its PWM inverting input is higher than its Vfb1 input). This condition will continue until Comp2's amplitude is equal to Comp1's. During this condition, the output voltage is being shorted to ground through the bottom FET, on the slave side. In hiccup mode, if this shoot−through current is large enough to develop 70 mV across L1, the Controllers will remain in hiccup mode even after the external load or short is removed. To avoid this condition, the Comp2 ramp's rise time is increased to minimize the shoot−through current. The value of the Comp2 capacitor is calculated by the following equations.

$$R_X = R_{L2} + R_{fet}$$

$$C13 = \frac{C8}{\frac{0.45 \cdot R_{L2}}{(0.07 \cdot 25\%) \cdot R_X} + 1}$$

where:

C8 = Comp1 capacitor value, 0.22 μF is suggested.

R_{L2} = Inductor parasitic resistance (LSR), see inductor's data sheet.

R_{fet} = $R_{DS(on)}$ of the Slave's lower FET, see data sheet.

A good rule of thumb is a 20 to 1 ratio between Comp1 and Comp2. If Soft−Start rise time is not an issue, a 0.22 μF

capacitor on the Comp1 pin and a 0.01 μF capacitor on the Comp2 pin in suggested.

Selecting Current Sharing Current Limit

In a two−phase single output application, there are two different current limit options. The Master (Controller One) current limit can be set equal to the Slave (Controller Two) which brings both controllers into Hiccup Mode during an overcurrent condition. The second option is to set Slave current limit lower than that of the Master, which limits the Slave's input power when its limit is reached, while the output voltage remains in regulation. Both Master and Slave will go into hiccup mode if the Master's limit is reached. During Cycle−By−Cycle current limit, the Slave's operating frequency will decrease in half, due to pulse skipping, resulting in phase overlap. This overlap will increase the output voltage ripple.

Exceeding 70 mV between the IS+ and IS− pins trips the current limits. A divided down V_{out} signal is used to generate the IS− reference, and inductor sensing of the controllers output chokes provide the output current information to IS+X pin. The inductor sensing is achieved by placing a series RC in parallel with the output choke. With the RC time constant selected to equal the L/R_L time constant, the voltage across the capacitor will be equal to the voltage drop across the internal resistance of the inductor.

The resistance of the output choke (LSR) must be known to calculate the overcurrent trip point. The voltage drop across the inductor at overcurrent is calculated as follows:

$$V_L = R_L \cdot I_{out} \quad \text{(eq. 1)}$$

where:

V_L = Voltage drop across the inductor,

R_L = LSR of the inductor,

I_{out} = Output current trip point for one phase.

For Hiccup Mode only, both sensing networks should have the identical values.

If the inductor selected has a 5.0 mΩ LSR and the current limit is 10 A through one of the phases, then the analog signal will be 50 mV. Since this value is less than 70 mV, then the IS− divider, R3 and R4 in Figure 1, must scale down the V_{out} by 20 mV, thus placing a 20 mV offset across the IS− and IS+x pin at no load and allowing the Controllers to trip into current limit with only 50 mV across the inductor. In this case, the RC values are calculated using the following equation:

$$R_{RC} = \frac{L}{C_{RC} \cdot R_L} \quad \text{(eq. 2)}$$

L = Inductor value, both Controllers should have the same value.

R_L = Internal resistance of L, see data sheet.

C_{RC} = Chosen value, 0.1 μF will make R a reasonable value.

And the IS− divider value can be selected with this equation.

$$R3 = \left(\frac{V_{out}}{V_{out} - V_{os}} - 1\right) \cdot R4 \quad \text{(eq. 3)}$$

where:

V_{out} = Output regulated voltage.

V_{os} = Offset voltage, example above was 20 mV.

R4 = Chosen value, 10 KΩ is a good choice.

If V_{os} is larger than 70 mV, then the current signal from the output chokes must be divided down. For example, if the inductor's LSR is equal to 8.0 mΩ and the current limit is 15 A, then the current signal is 120 mV, which is almost twice the comparator's offset (70 mV). This signal can be divided down by adding a resistor (R1) in parallel with the capacitor (C6) in the inductor sensing network, see Figure 1. The divider R1 and R2 can be set to equal value to divide the current signal in half and equation (3) should be used to select the proper voltage divider. Notice that the divider R1 and R2, divides down the voltage applied to the capacitor C_{RC} by a factor of 2. This divides the voltage across the output inductor's LSR by a factor of two and results in twice the current limit. This scaling technique is another way the current limit may be set so that virtually any current limit may be obtained.

To ensure accuracy, the equivalent parallel resistance of R1 and R2 should be greater or equal to the value R_{RC}, the resistance value calculated from equation (2). If Hiccup Mode is used, then both sensing network values must be equal.

If Cycle−by−Cycle is desired, then equation (1), (2) and (3) should be used to select the Slave's inductor sensing network for the desired current limit and equation (4) should be used to raise the Master's current limit, Hiccup Mode, above the Slave's limit.

$$R2 = \frac{R1(1 - Ratio)}{Ratio} \quad \text{(eq. 4)}$$

where:

R1 = Chosen value, 10 KΩ is recommended,

$Ratio = \frac{I_{slave.limit}}{I_{master.limit}}$, Master's and Slave's current limit ratio.

To ensure greater accuracy, the equivalent parallel resistance of R1 and R2 should be greater or equal to the value R_{RC}, value calculated from equation (2).

$$R_{RC} \leq \frac{R1 \cdot R2}{R1 + R2} \quad \text{(eq. 5)}$$

Current Sensing

The current supplied to the load can be sensed easily using the IS+ and IS− pins for the output. These pins sense a voltage, proportional to the output current, and compare it to a fixed internal voltage threshold. When the differential voltage exceeds 70 mV, the internal overcurrent protection system goes into hiccup mode. Two methods for sensing the current are available.

Sense Resistor. A sense resistor can be added in series with the inductor. When the voltage drop across the sense resistor exceeds the internal voltage threshold of 70 mV, a fault condition is set.

The sense resistor is selected according to:

$$R_{SENSE} = \frac{0.070\ V}{I_{LIMIT}}$$

In a high current supply, the sense resistor will be a very low value, typically less than 10 mΩ. Such a resistor can be either a discrete component or a PCB trace. The resistance value of a discrete component can be more precise than a PCB trace, but the cost is also greater.

Setting the current limit using an external sense resistor is very precise because all the values can be designed to specific tolerances. However, the disadvantage of using a sense resistor is its additional constant power loss and heat generation.

Inductor ESR. Another means of sensing current is to use the intrinsic resistance of the inductor. A model of an inductor reveals that the windings of an inductor have an effective series resistance (ESR).

The voltage drop across the inductor ESR can be measured with a simple parallel circuit: an RC integrator. If the value of R_{S1} and C are chosen such that:

$$\frac{L}{ESR} = R_{S1}C$$

then the voltage measured across the capacitor C will be:

$$V_C = ESR \times I_{LIM}$$

Selecting Components. Select the capacitor C first. A value of 0.1 μF is recommended. The value of R_{S1} can be selected according to:

$$R_{S1} = \frac{1}{ESR \times C}$$

Typical values for inductor ESR range in the low m; consult manufacturer's datasheet for specific details.

Selection of components at these values will result in a current limit of:

$$I_{LIM} = \frac{0.070\ V}{ESR}$$

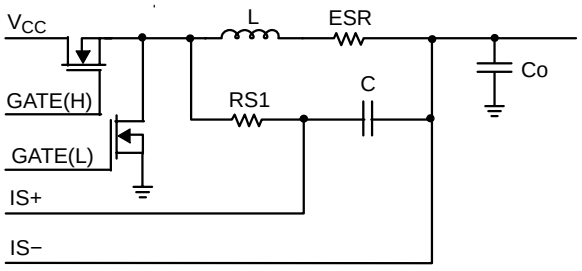


Figure 9. Inductor ESR Current Sensing

Given an ESR value of 3.5 mΩ, the current limit becomes 20 A. If an increased current limit is required, a resistor divider can be added.

The advantages of setting the current limit by using the winding resistance of the inductor are that efficiency is maximized and heat generation is minimized. The tolerance of the inductor ESR must be factored into the design of the current limit. Finally, one or two more components are required for this approach than with resistor sensing.

Adding External Slope Compensation

Today's voltage regulators are expected to meet very stringent load transient requirements. One of the key factors in achieving tight dynamic voltage regulation is low ESR. Low ESR at the regulator output results in low output voltage ripple. The consequence is, however, that very little voltage ramp exists at the control IC feedback pin (V_{FB}), resulting in increased regulator sensitivity to noise and the potential for loop instability. In applications where the internal slope compensation is insufficient, the performance of the NCP5424−based regulator can be improved through the addition of a fixed amount of external slope compensation at the output of the PWM Error Amplifier (the COMP pin) during the regulator off−time. Referring to Figure 8, the amount of voltage ramp at the COMP pin is dependent on the gate voltage of the lower (synchronous) FET and the value of resistor divider formed by R1and R2.

$$V_{SLOPECOMP} = V_{GATE(L)} \times \left(\frac{R2}{R1 + R2}\right) \times \left(1 - e^{\frac{-t}{\tau}}\right)$$

where:

$V_{SLOPECOMP}$ = amount of slope added;
$V_{GATE(L)}$ = lower MOSFET gate voltage;
R1, R2 = voltage divider resistors;
$t = t_{ON}$ or t_{OFF} (switch off−time);
τ = RC constant determined by C1 and the parallel combination of R1, R2 neglecting the low driver output impedance.

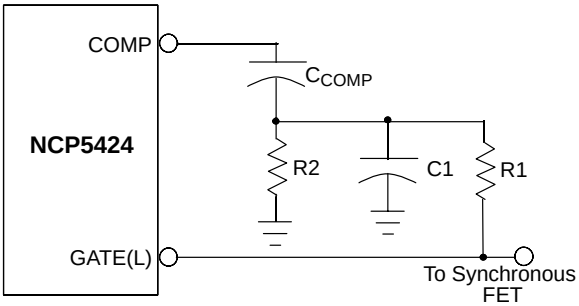


Figure 10. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of Each On−Time Cycle

The artificial voltage ramp created by the slope compensation scheme results in improved control loop stability provided that the RC filter time constant is smaller than the off−time cycle duration (time during which the lower MOSFET is conducting). It is important that the series combination of R1 and R2 is high enough in resistance to avoid loading the GATE(L) pin. Also, C1 should be very small (less than a few nF) to avoid heating the part.

EMI MANAGEMENT

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

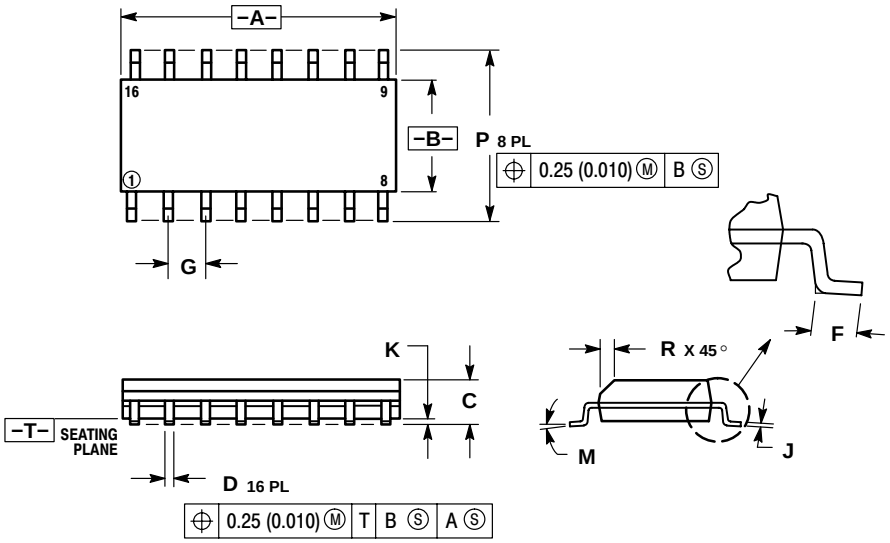
LAYOUT GUIDELINES

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the NCP5424.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double−sided PCB's a single ground plane (usually the bottom) is recommended.
5. Even though double sided PCB's are usually sufficient for a good layout, four−layer PCB's are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layers for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The MOSFET gate traces to the IC must be short, straight, and wide as possible.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching MOSFET as close to the input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the COMP capacitor as close as possible to the COMP pin.
12. Connect the filter components of the following pins: $R_{OSC,}$ V_{FB}, V_{OUT}, and COMP to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.
13. Place the V_{CC} bypass capacitors as close as possible to the IC.
14. Place the R_{OSC} resistor as close as possible to the R_{OSC} pin.
15. Include provisions for 100−100pF capacitor across each resistor of the feedback network to improve noise immunity and add COMP.
16. Assign the output with lower duty cycle to channel 2, which has better noise immunity.

PACKAGE DIMENSIONS

SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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