

**Quad Digitally Controlled (XDCP™) Potentiometers**

**FEATURES**

- Four potentiometers in one package
- 64 resistor taps per potentiometer
- 2-wire serial interface
- Wiper resistance, 40Ω typical at 5V
- Four nonvolatile data registers for each pot
- Nonvolatile storage of wiper position
- Standby current < 1μA max (total package)
- V<sub>CC</sub> = 2.7V to 5.5V operation  
V<sub>+</sub> = 2.7V to 5.5V  
V<sub>-</sub> = -2.7V to -5.5V
- 10kΩ, 2.5kΩ end to end resistances
- High reliability
  - Endurance—100,000 data changes per bit per register
  - Register data retention—100 years
- 24 Ld SOIC, 24 Ld TSSOP, 24 Ld PDIP packages
- Pb-free plus anneal available (RoHS compliant)

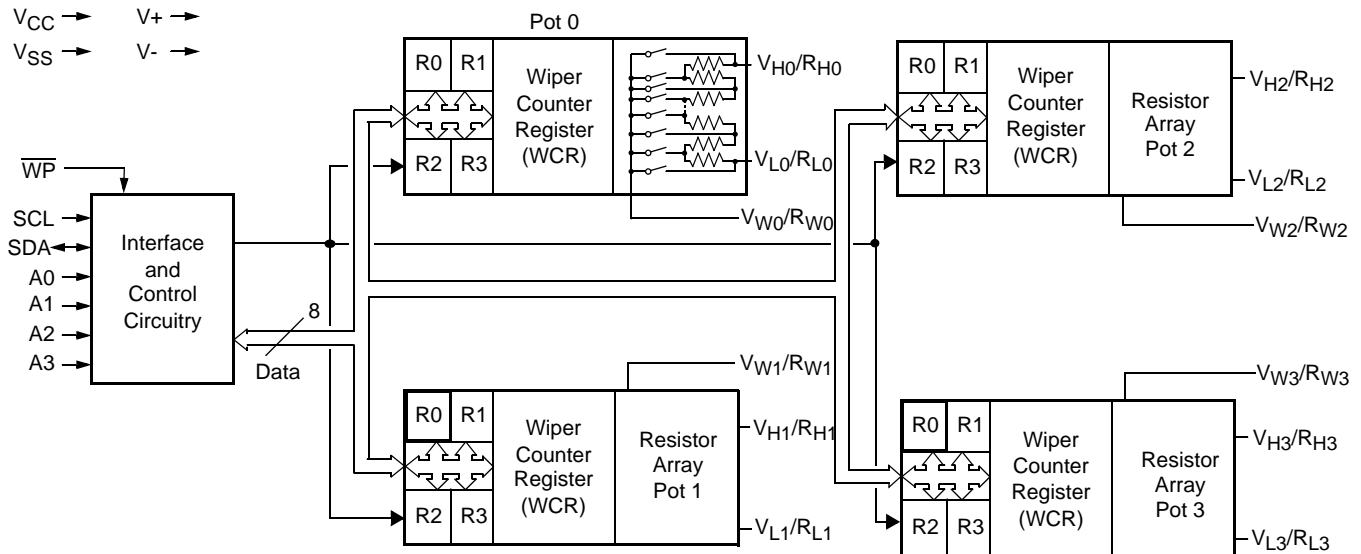
**DESCRIPTION**

The X9408 integrates four digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

The digital controlled potentiometer is implemented using 63 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-wire bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four non-volatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array though the switches. Powerup recalls the contents of the default data register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

**BLOCK DIAGRAM**



**Ordering Information**

| PART NUMBER              | PART MARKING | V <sub>CC</sub> LIMITS (V) | POTENTIOMETER ORGANIZATION (kΩ) | TEMP RANGE (°C)               | PACKAGE                                     |                               |
|--------------------------|--------------|----------------------------|---------------------------------|-------------------------------|---|-------------------------------|
| X9408YP24                |              | 5 ±10%                     | 2.5                             | 0 to 70                       | 24 Ld PDIP                                  |                               |
| X9408YS24*               |              |                            |                                 | 0 to 70                       | 24 Ld SOIC (300 mil)                        |                               |
| X9408YS24I*              |              |                            |                                 | -40 to 85                     | 24 Ld SOIC (300 mil)                        |                               |
| X9408YV24*               | X9408YV      |                            |                                 | 0 to 70                       | 24 Ld TSSOP (4.4mm)                         |                               |
| X9408YV24Z* (Note)       | X9408YV Z    |                            |                                 | 0 to 70                       | 24 Ld TSSOP (4.4mm) (Pb-free)               |                               |
| X9408YV24I*              | X9408YV I    |                            |                                 | -40 to 85                     | 24 Ld TSSOP (4.4mm)                         |                               |
| X9408YV24IZ* (Note)      | X9408YV Z I  |                            |                                 | -40 to 85                     | 24 Ld TSSOP (4.4mm) (Pb-free)               |                               |
| X9408WP24                |              |                            | 2.7 to 5.5                      | 10                            | 0 to 70                                     | 24 Ld PDIP                    |
| X9408WP24I               |              |                            |                                 |                               | -40 to 85                                   | 24 Ld PDIP                    |
| X9408WS24*               | X9408WS      |                            |                                 |                               | 0 to 70                                     | 24 Ld SOIC (300 mil)          |
| X9408WS24I*              | X9408WS I    |                            |                                 |                               | -40 to 85                                   | 24 Ld SOIC (300 mil)          |
| X9408WV24*               | X9408WV      |                            |                                 |                               | 0 to 70                                     | 24 Ld TSSOP (4.4mm)           |
| X9408WV24Z* (Note)       | X9408WV Z    |                            |                                 |                               | 0 to 70                                     | 24 Ld TSSOP (4.4mm) (Pb-free) |
| X9408WV24I*              | X9408WV I    |                            |                                 |                               | -40 to 85                                   | 24 Ld TSSOP (4.4mm)           |
| X9408WV24IZ* (Note)      | X9408WV Z I  | -40 to 85                  |                                 | 24 Ld TSSOP (4.4mm) (Pb-free) |   |                               |
| X9408YP24I-2.7           |              | 2.5                        |                                 | 2.5                           | -40 to 85                                   | 24 Ld PDIP                    |
| X9408YS24-2.7*           |              |                            |                                 |                               | 0 to 70                                     | 24 Ld SOIC (300 mil)          |
| X9408YS24I-2.7*          |              |                            |                                 |                               | -40 to 85                                   | 24 Ld SOIC (300 mil)          |
| X9408YV24-2.7*           | X9408YV F    |                            |                                 |                               | 0 to 70                                     | 24 Ld TSSOP (4.4mm)           |
| X9408YV24Z-2.7* (Note)   | X9408YV Z F  |                            |                                 |                               | 0 to 70                                     | 24 Ld TSSOP (4.4mm) (Pb-free) |
| X9408YV24I-2.7*          | X9408YV G    |                            |                                 |                               | -40 to 85                                   | 24 Ld TSSOP (4.4mm)           |
| X9408YV24IZ-2.7T1 (Note) | X9408YV Z G  |                            | -40 to 85                       |                               | 24 Ld TSSOP (4.4mm) Tape and Reel (Pb-free) |                               |
| X9408WP24-2.7            |              |                            | 10                              | 10                            | 0 to 70                                     | 24 Ld PDIP                    |
| X9408WP24I-2.7           |              |                            |                                 |                               | -40 to 85                                   | 24 Ld PDIP                    |
| X9408WS24-2.7*           | X9408WS F    |                            |                                 |                               | 0 to 70                                     | 24 Ld SOIC (300 mil)          |
| X9408WS24I-2.7*          | X9408WS G    |                            |                                 |                               | -40 to 85                                   | 24 Ld SOIC (300 mil)          |
| X9408WSI-2.7             |              |                            |                                 |                               | -40 to 85                                   | 24 Ld SOIC (300 mil)          |
| X9408WV24-2.7*           | X9408WV F    |                            |                                 |                               | 0 to 70                                     | 24 Ld TSSOP (4.4mm)           |
| X9408WV24Z-2.7* (Note)   | X9408WV Z F  |                            |                                 |                               | 0 to 70                                     | 24 Ld TSSOP (4.4mm) (Pb-free) |
| X9408WV24I-2.7*          | X9408WV G    | -40 to 85                  |                                 | 24 Ld TSSOP (4.4mm)           |   |                               |
| X9408WV24IZ-2.7* (Note)  | X9408WV Z G  | -40 to 85                  |                                 | 24 Ld TSSOP (4.4mm) (Pb-free) |   |                               |

\*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**PIN DESCRIPTIONS**

**Host Interface Pins**

**Serial Clock (SCL)**

The SCL input is used to clock data into and out of the X9408.

**Serial Data (SDA)**

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

**Device Address (A<sub>0</sub> - A<sub>3</sub>)**

The address inputs are used to set the least significant 4 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9408. A maximum of 16 devices may occupy the 2-wire serial bus.

**Potentiometer Pins**

**V<sub>H</sub>/R<sub>H</sub> (V<sub>H0</sub>/R<sub>H0</sub> - V<sub>H3</sub>/R<sub>H3</sub>), V<sub>L</sub>/R<sub>L</sub> (V<sub>L0</sub>/R<sub>L0</sub> - V<sub>L3</sub>/R<sub>L3</sub>)**

The V<sub>H</sub>/R<sub>H</sub> and V<sub>L</sub>/R<sub>L</sub> inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

**V<sub>W</sub>/R<sub>W</sub> (V<sub>W0</sub>/R<sub>W0</sub> - V<sub>W3</sub>/R<sub>W3</sub>)**

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

**Hardware Write Protect Input ( $\overline{WP}$ )**

The  $\overline{WP}$  pin when low prevents nonvolatile writes to the Data Registers.

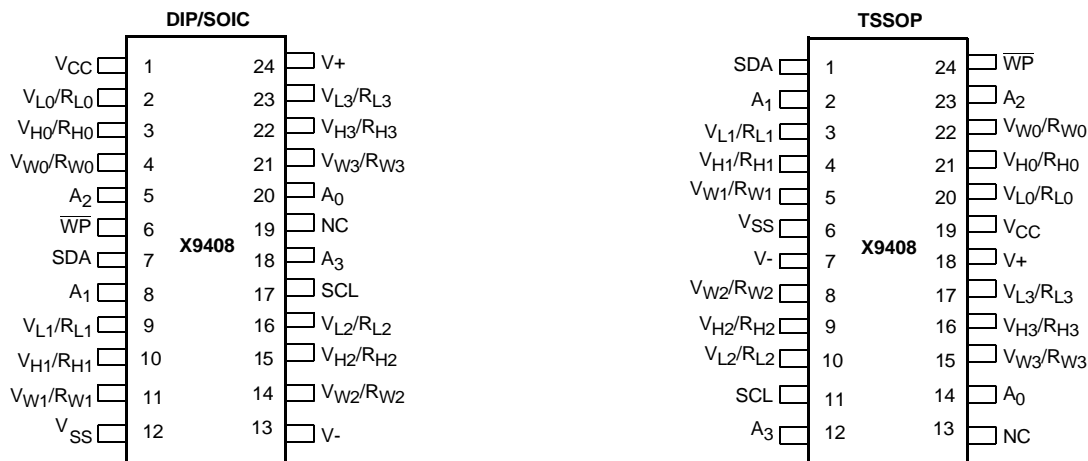
**Analog Supplies V+, V-**

The Analog Supplies V+, V- are the supply voltages for the XDCP analog section.

**PIN NAMES**

| Symbol   | Description                                 |
|--|---|
| SCL  | Serial Clock                                |
| SDA  | Serial Data                                 |
| A0-A3  | Device Address                              |
| V <sub>H0</sub> /R <sub>H0</sub> - V <sub>H3</sub> /R <sub>H3</sub> ,<br>V <sub>L0</sub> /R <sub>L0</sub> - V <sub>L3</sub> /R <sub>L3</sub> | Potentiometer Pins<br>(terminal equivalent) |
| V <sub>W0</sub> /R <sub>W0</sub> - V <sub>W3</sub> /R <sub>W3</sub>  | Potentiometer Pins<br>(wiper equivalent)    |
| $\overline{WP}$  | Hardware Write Protection                   |
| V+, V-   | Analog Supplies                             |
| V <sub>CC</sub>  | System Supply Voltage                       |
| V <sub>SS</sub>  | System Ground                               |
| NC   | No Connection                               |

**PIN CONFIGURATION**



**PRINCIPLES OF OPERATION**

The X9408 is a highly integrated microcircuit incorporating four resistor arrays and their associated registers and counters and the serial interface logic providing direct communication between the host and the XDCP potentiometers.

**Serial Interface**

The X9408 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9408 will be considered a slave device in all applications.

**Clock and Data Conventions**

Data states on the SDA line can change only during SCL LOW periods ( $t_{LOW}$ ). SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

**Start Condition**

All commands to the X9408 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH ( $t_{HIGH}$ ). The X9408 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

**Stop Condition**

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

**Acknowledge**

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9408 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9408 will respond with a final acknowledge.

**Array Description**

The X9408 is comprised of four resistor arrays. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer ( $R_H$  and  $R_L$  inputs).

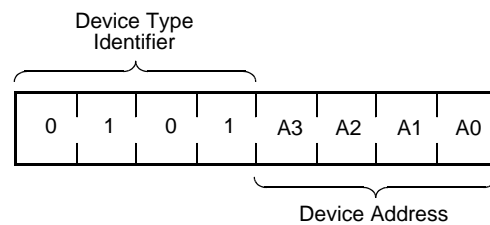
At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper ( $R_W$ ) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The six bits of the WCR are decoded to select, and enable, one of sixty-four switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated Data Registers into the WCR. These Data Registers and the WCR can be read and written by the host system.

**Device Addressing**

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (refer to Figure 1 below). For the X9408 this is fixed as 0101[B].

**Figure 1. Slave Address**

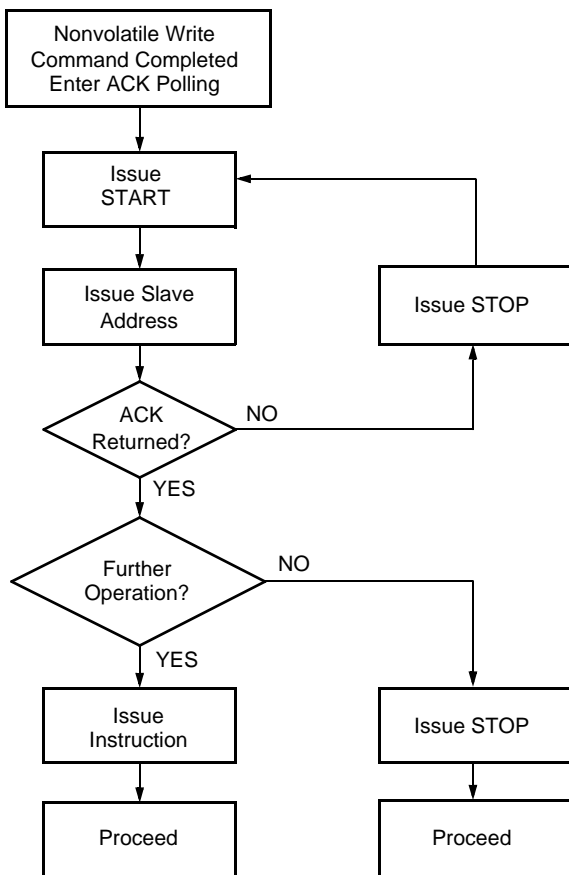


The next four bits of the slave address are the device address. The physical device address is defined by the state of the  $A_0 - A_3$  inputs. The X9408 compares the serial data stream with the address input state; a successful compare of all four address bits is required for the X9408 to respond with an acknowledge. The  $A_0 - A_3$  inputs can be actively driven by CMOS input signals or tied to  $V_{CC}$  or  $V_{SS}$ .

**Acknowledge Polling**

The disabling of the inputs, during the internal Nonvolatile write operation, can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9408 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9408 is still busy with the write operation no ACK will be returned. If the X9408 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

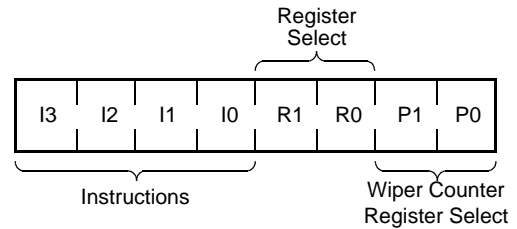
**Flow 1. ACK Polling Sequence**



**Instruction Structure**

The next byte sent to the X9408 contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of the two pots and when applicable they point to one of four associated registers. The format is shown below in Figure 2.

**Figure 2. Instruction Byte Format**

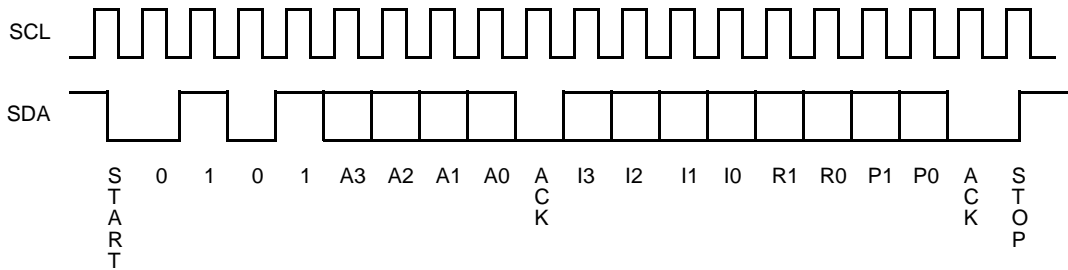


The four high order bits define the instruction. The next two bits (R1 and R0) select one of the four registers that is to be acted upon when a register oriented instruction is issued. The last bits (P1, P0) select which one of the four potentiometers is to be affected by the instruction.

Four of the nine instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 3. These two-byte instructions exchange data between the Wiper Counter Register and one of the Data Registers. A transfer from a Data Register to a Wiper Counter Register is essentially a write to a static RAM. The response of the wiper to this action will be delayed  $t_{WRL}$ . A transfer from the Wiper Counter Register (current wiper position), to a data register is a write to nonvolatile memory and takes a minimum of  $t_{WR}$  to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or it may occur globally, wherein the transfer occurs between all of the potentiometers and one of their associated registers.

Four instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9408; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are: Read Wiper Counter Register (read the current wiper position of the selected pot), Write Wiper Counter Register (change current wiper position of the selected pot), Read Data Register (read the contents of the selected nonvolatile register) and Write Data Register (write a new value to the selected Data Register). The sequence of operations is shown in Figure 4.

Figure 3. Two-Byte Instruction Sequence



The Increment/Decrement command is different from the other commands. Once the command is issued and the X9408 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (HIGH) while SDA is HIGH, the selected wiper will

move one resistor segment towards the  $R_H$  terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the  $R_L$  terminal. A detailed illustration of the sequence and timing for this operation are shown in Figures 5 and 6 respectively.

Table 1. Instruction Set

| Instruction  | Instruction Set |                |                |                |                |                |                |                | Operation   |
|--|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---|
|  | I <sub>3</sub>  | I <sub>2</sub> | I <sub>1</sub> | I <sub>0</sub> | R <sub>1</sub> | R <sub>0</sub> | P <sub>1</sub> | P <sub>0</sub> |   |
| Read Wiper Counter Register                          | 1               | 0              | 0              | 1              | 0              | 0              | P <sub>1</sub> | P <sub>0</sub> | Read the contents of the Wiper Counter Register pointed to by P <sub>1</sub> - P <sub>0</sub>   |
| Write Wiper Counter Register                         | 1               | 0              | 1              | 0              | 0              | 0              | P <sub>1</sub> | P <sub>0</sub> | Write new value to the Wiper Counter Register pointed to by P <sub>1</sub> - P <sub>0</sub>   |
| Read Data Register                                   | 1               | 0              | 1              | 1              | R <sub>1</sub> | R <sub>0</sub> | P <sub>1</sub> | P <sub>0</sub> | Read the contents of the Data Register pointed to by P <sub>1</sub> - P <sub>0</sub> and R <sub>1</sub> - R <sub>0</sub>  |
| Write Data Register                                  | 1               | 1              | 0              | 0              | R <sub>1</sub> | R <sub>0</sub> | P <sub>1</sub> | P <sub>0</sub> | Write new value to the Data Register pointed to by P <sub>1</sub> - P <sub>0</sub> and R <sub>1</sub> - R <sub>0</sub>  |
| XFR Data Register to Wiper Counter Register          | 1               | 1              | 0              | 1              | R <sub>1</sub> | R <sub>0</sub> | P <sub>1</sub> | P <sub>0</sub> | Transfer the contents of the Data Register pointed to by P <sub>1</sub> - P <sub>0</sub> and R <sub>1</sub> - R <sub>0</sub> to its associated Wiper Counter Register |
| XFR Wiper Counter Register to Data Register          | 1               | 1              | 1              | 0              | R <sub>1</sub> | R <sub>0</sub> | P <sub>1</sub> | P <sub>0</sub> | Transfer the contents of the Wiper Counter Register pointed to by P <sub>1</sub> - P <sub>0</sub> to the Data Register pointed to by R <sub>1</sub> - R <sub>0</sub>  |
| Global XFR Data Registers to Wiper Counter Registers | 0               | 0              | 0              | 1              | R <sub>1</sub> | R <sub>0</sub> | 0              | 0              | Transfer the contents of the Data Registers pointed to by R <sub>1</sub> - R <sub>0</sub> of all four pots to their respective Wiper Counter Registers                |
| Global XFR Wiper Counter Registers to Data Register  | 1               | 0              | 0              | 0              | R <sub>1</sub> | R <sub>0</sub> | 0              | 0              | Transfer the contents of both Wiper Counter Registers to their respective Data Registers pointed to by R <sub>1</sub> - R <sub>0</sub> of all four pots               |
| Increment/Decrement Wiper Counter Register           | 0               | 0              | 1              | 0              | 0              | 0              | P <sub>1</sub> | P <sub>0</sub> | Enable Increment/decrement of the Wiper Counter Register pointed to by P <sub>1</sub> - P <sub>0</sub>  |

Note: (7) 1/0 = data is one or zero

Figure 4. Three-Byte Instruction Sequence

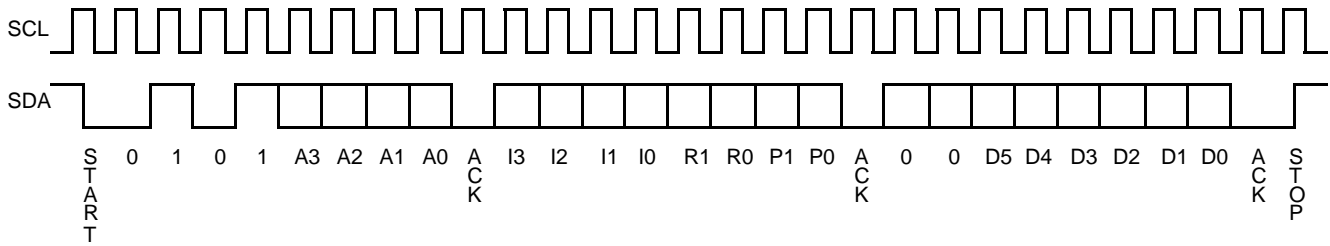


Figure 5. Increment/Decrement Instruction Sequence

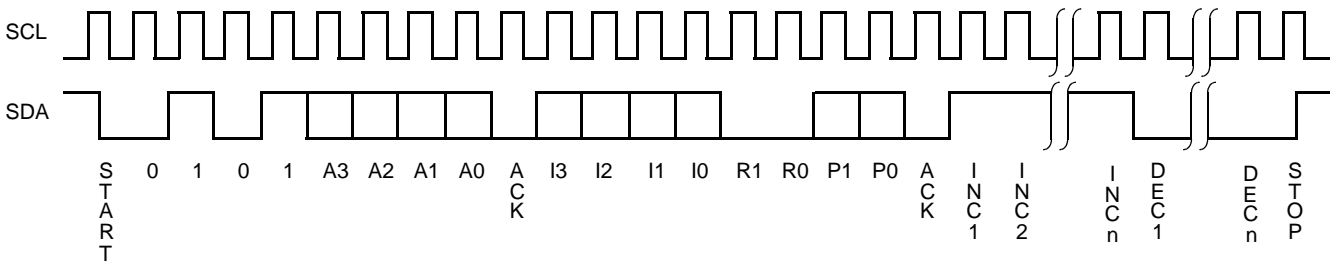


Figure 6. Increment/Decrement Timing Limits

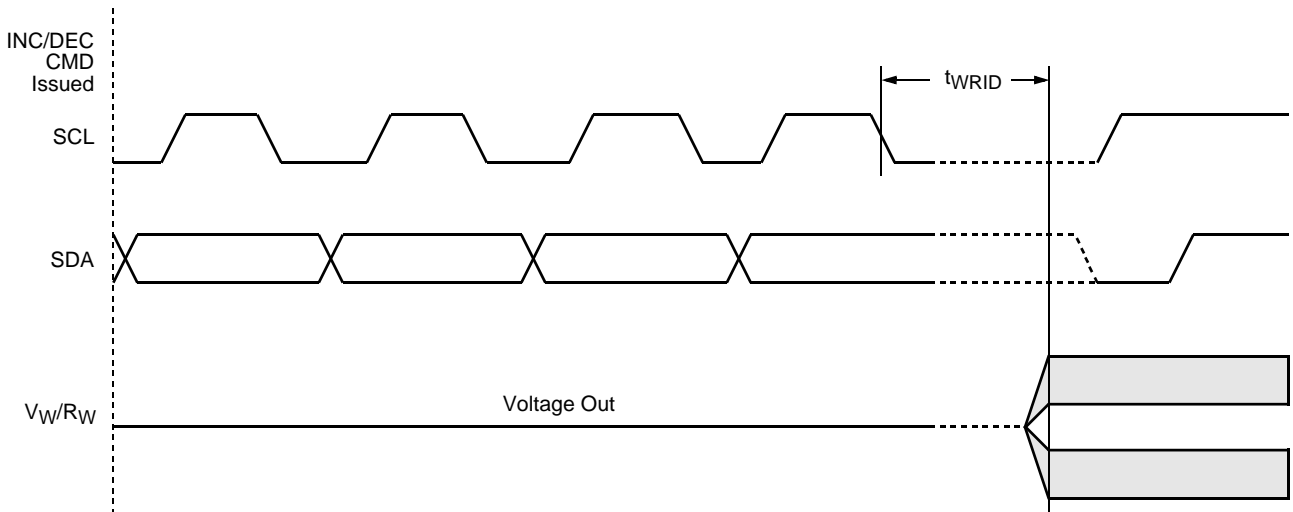


Figure 7. Acknowledge Response from Receiver

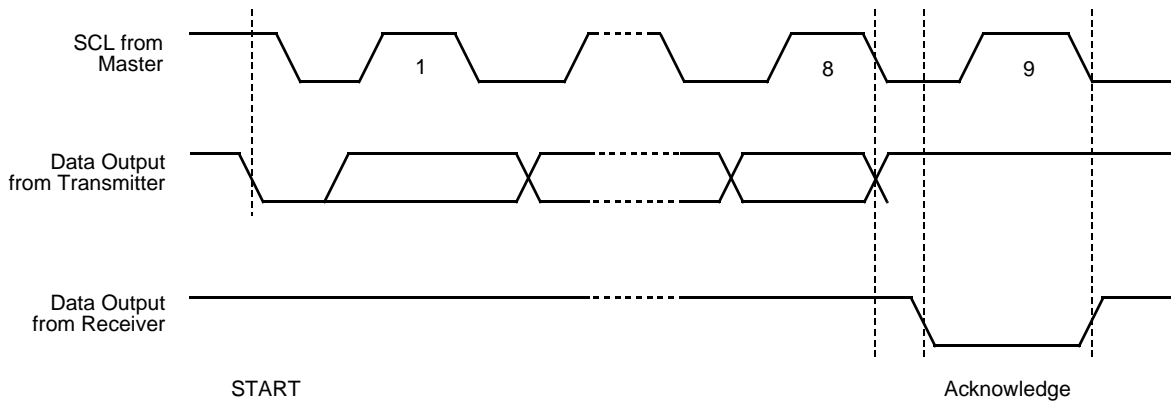
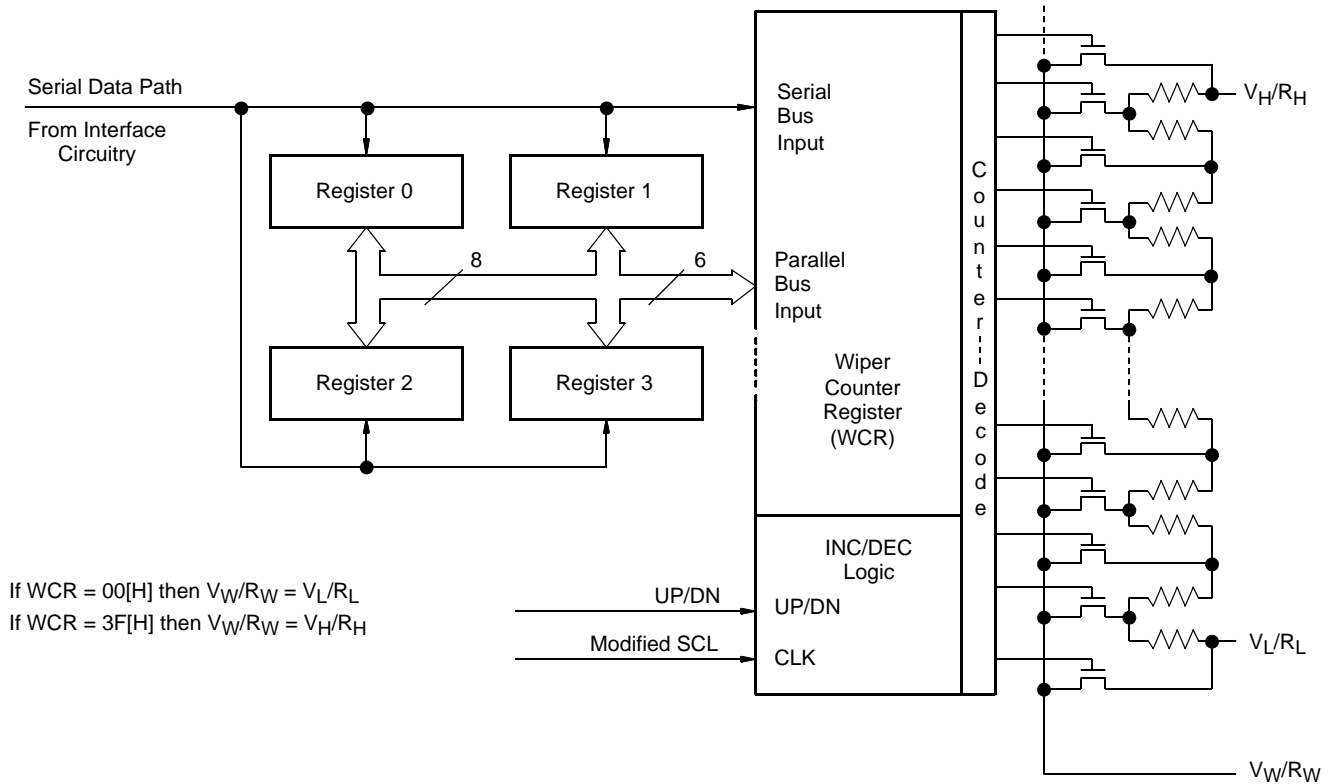


Figure 8. Detailed Potentiometer Block Diagram





**DETAILED OPERATION**

All XDCP potentiometers share the serial interface and share a common architecture. Each potentiometer has a Wiper Counter Register and four Data Registers. A detailed discussion of the register organization and array operation follows.

**Wiper Counter Register**

The X9408 contains four Wiper Counter Registers, one for each XDCP potentiometer. The Wiper Counter Register can be envisioned as a 6-bit parallel and serial load counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/ Decrement instruction. Finally, it is loaded with the contents of its data register zero (DR0) upon power-up.

The WCR is a volatile register; that is, its contents are lost when the X9408 is powered-down. Although the register is automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

**Data Registers**

Each potentiometer has four nonvolatile Data Registers. These can be read or written directly by the host and data can be transferred between any of the four Data Registers and the WCR. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could possibly store system parameters or user preference data.

**Register Descriptions**

**Data Registers, (6-Bit), Nonvolatile**

|       |    |    |       |    |    |
|-------|----|----|-------|----|----|
| D5    | D4 | D3 | D2    | D1 | D0 |
| NV    | NV | NV | NV    | NV | NV |
| (MSB) |    |    | (LSB) |    |    |

Four 6-bit Data Registers for each XDCP. (sixteen 6-bit registers in total).

- {D5~D0}: These bits are for general purpose not volatile data storage or for storage of up to four different wiper values. The contents of Data Register 0 are automatically moved to the wiper counter register on power-up.

**Wiper Counter Register, (6-Bit), Volatile**

|       |     |     |       |     |     |
|-------|-----|-----|-------|-----|-----|
| WP5   | WP4 | WP3 | WP2   | WP1 | WP0 |
| V     | V   | V   | V     | V   | V   |
| (MSB) |     |     | (LSB) |     |     |

One 6-bit Wiper Counter Register for each XDCP. (Four 6-bit registers in total.)

- {D5~D0}: These bits specify the wiper position of the respective XDCP. The Wiper Counter Register is loaded on power-up by the value in Data Register 0. The contents of the WCR can be loaded from any of the other Data Register or directly. The contents of the WCR can be saved in a DR.

**Instruction Format**

- Notes:** (1) "MACK"/"SACK": stands for the acknowledge sent by the master/slave.  
 (2) "A3 ~ A0": stands for the device addresses sent by the master.  
 (3) "X": indicates that it is a "0" for testing purpose but physically it is a "don't care" condition.  
 (4) "I": stands for the increment operation, SDA held high during active SCL phase (high).  
 (5) "D": stands for the decrement operation, SDA held low during active SCL phase (high).

**Read Wiper Counter Register (WCR)**

| S<br>T<br>A<br>R<br>T | device type identifier |   |   |   | device addresses |    |    |    | S<br>A<br>C<br>K | instruction opcode |   |   |   | WCR addresses |   |    |    | S<br>A<br>C<br>K | wiper position (sent by slave on SDA) |   |    |    |    |    |    | M<br>A<br>C<br>K | S<br>T<br>O<br>P |    |
|-----------------------|------------------------|---|---|---|------------------|----|----|----|------------------|--------------------|---|---|---|---------------|---|----|----|------------------|---------------------------------------|---|----|----|----|----|----|------------------|------------------|----|
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 0 | 0 | 1 | 0             | 0 | P1 | P0 |                  | 0                                     | 0 | W5 | W4 | W3 | W2 | W1 |                  |                  | W0 |
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 0 | 0 | 1 | 0             | 0 | P1 | P0 |                  | 0                                     | 0 | W5 | W4 | W3 | W2 | W1 | W0               |                  |    |

**Write Wiper Counter Register (WCR)**

| S<br>T<br>A<br>R<br>T | device type identifier |   |   |   | device addresses |    |    |    | S<br>A<br>C<br>K | instruction opcode |   |   |   | WCR addresses |   |    |    | S<br>A<br>C<br>K | wiper position (sent by master on SDA) |   |    |    |    |    |    | S<br>A<br>C<br>K | S<br>T<br>O<br>P |    |
|-----------------------|------------------------|---|---|---|------------------|----|----|----|------------------|--------------------|---|---|---|---------------|---|----|----|------------------|--|---|----|----|----|----|----|------------------|------------------|----|
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 0 | 1 | 0 | 0             | 0 | P1 | P0 |                  | 0                                      | 0 | W5 | W4 | W3 | W2 | W1 |                  |                  | W0 |
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 0 | 1 | 0 | 0             | 0 | P1 | P0 |                  | 0                                      | 0 | W5 | W4 | W3 | W2 | W1 | W0               |                  |    |

**Read Data Register (DR)**

| S<br>T<br>A<br>R<br>T | device type identifier |   |   |   | device addresses |    |    |    | S<br>A<br>C<br>K | instruction opcode |   |   |   | DR and WCR addresses |    |    |    | S<br>A<br>C<br>K | wiper position/data (sent by slave on SDA) |   |    |    |    |    |    | M<br>A<br>C<br>K | S<br>T<br>O<br>P |    |
|-----------------------|------------------------|---|---|---|------------------|----|----|----|------------------|--------------------|---|---|---|----------------------|----|----|----|------------------|--|---|----|----|----|----|----|------------------|------------------|----|
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 0 | 1 | 1 | R1                   | R0 | P1 | P0 |                  | 0  | 0 | W5 | W4 | W3 | W2 | W1 |                  |                  | W0 |
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 0 | 1 | 1 | R1                   | R0 | P1 | P0 |                  | 0  | 0 | W5 | W4 | W3 | W2 | W1 | W0               |                  |    |

**Write Data Register (DR)**

| S<br>T<br>A<br>R<br>T | device type identifier |   |   |   | device addresses |    |    |    | S<br>A<br>C<br>K | instruction opcode |   |   |   | DR and WCR addresses |    |    |    | S<br>A<br>C<br>K | wiper position/data (sent by master on SDA) |   |    |    |    |    |    | S<br>A<br>C<br>K | S<br>T<br>O<br>P | HIGH-VOLTAGE WRITE CYCLE |    |
|-----------------------|------------------------|---|---|---|------------------|----|----|----|------------------|--------------------|---|---|---|----------------------|----|----|----|------------------|---|---|----|----|----|----|----|------------------|------------------|--------------------------|----|
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 1 | 0 | 0 | R1                   | R0 | P1 | P0 |                  | 0   | 0 | W5 | W4 | W3 | W2 | W1 |                  |                  |                          | W0 |
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 1 | 0 | 0 | R1                   | R0 | P1 | P0 |                  | 0   | 0 | W5 | W4 | W3 | W2 | W1 | W0               |                  |                          |    |

**XFR Data Register (DR) to Wiper Counter Register (WCR)**

| S<br>T<br>A<br>R<br>T | device type identifier |   |   |   | device addresses |    |    |    | S<br>A<br>C<br>K | instruction opcode |   |   |   | DR and WCR addresses |    |    |    | S<br>A<br>C<br>K | S<br>T<br>O<br>P |
|-----------------------|------------------------|---|---|---|------------------|----|----|----|------------------|--------------------|---|---|---|----------------------|----|----|----|------------------|------------------|
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 1 | 0 | 1 | R1                   | R0 | P1 | P0 |                  |                  |
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 1 | 0 | 1 | R1                   | R0 | P1 | P0 |                  |                  |

**Write Wiper Counter Register (WCR) to Data Register (DR)**

| S<br>T<br>A<br>R<br>T | device type identifier |   |   |   | device addresses |    |    |    | S<br>A<br>C<br>K | instruction opcode |   |   |   | DR and WCR addresses |    |    |    | S<br>A<br>C<br>K | S<br>T<br>O<br>P | HIGH-VOLTAGE WRITE CYCLE |
|-----------------------|------------------------|---|---|---|------------------|----|----|----|------------------|--------------------|---|---|---|----------------------|----|----|----|------------------|------------------|--------------------------|
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 1 | 1 | 0 | R1                   | R0 | P1 | P0 |                  |                  |                          |
|                       | 0                      | 1 | 0 | 1 | A3               | A2 | A1 | A0 |                  | 1                  | 1 | 1 | 0 | R1                   | R0 | P1 | P0 |                  |                  |                          |

**Increment/Decrement Wiper Counter Register (WCR)**

|                       |                        |   |   |   |                  |   |   |   |                  |                    |   |   |   |               |   |   |   |                  |   |     |   |   |   |   |                  |
|-----------------------|------------------------|---|---|---|------------------|---|---|---|------------------|--------------------|---|---|---|---------------|---|---|---|------------------|---|-----|---|---|---|---|------------------|
| S<br>T<br>A<br>R<br>T | device type identifier |   |   |   | device addresses |   |   |   | S<br>A<br>C<br>K | instruction opcode |   |   |   | WCR addresses |   |   |   | S<br>A<br>C<br>K | increment/decrement (sent by master on SDA) |     |   |   |   |   | S<br>T<br>O<br>P |
|                       | 0                      | 1 | 0 | 1 | A                | A | A | A |                  | 0                  | 0 | 1 | 0 | 0             | 0 | P | P |                  | I/D   | I/D | . | . | . | . |                  |

**Global XFR Data Register (DR) to Wiper Counter Register (WCR)**

|                       |                        |   |   |   |                  |   |   |   |                  |                    |   |   |   |              |   |   |   |                  |                  |
|-----------------------|------------------------|---|---|---|------------------|---|---|---|------------------|--------------------|---|---|---|--------------|---|---|---|------------------|------------------|
| S<br>T<br>A<br>R<br>T | device type identifier |   |   |   | device addresses |   |   |   | S<br>A<br>C<br>K | instruction opcode |   |   |   | DR addresses |   |   |   | S<br>A<br>C<br>K | S<br>T<br>O<br>P |
|                       | 0                      | 1 | 0 | 1 | A                | A | A | A |                  | 0                  | 0 | 0 | 1 | R            | R | 0 | 0 |                  |                  |

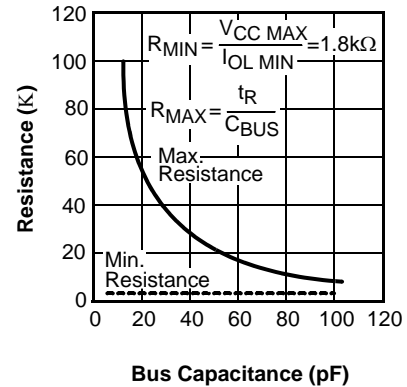
**Global XFR Wiper Counter Register (WCR) to Data Register (DR)**

|                       |                        |   |   |   |                  |   |   |   |                  |                    |   |   |   |              |   |   |   |                  |                  |                             |
|-----------------------|------------------------|---|---|---|------------------|---|---|---|------------------|--------------------|---|---|---|--------------|---|---|---|------------------|------------------|-----------------------------|
| S<br>T<br>A<br>R<br>T | device type identifier |   |   |   | device addresses |   |   |   | S<br>A<br>C<br>K | instruction opcode |   |   |   | DR addresses |   |   |   | S<br>A<br>C<br>K | S<br>T<br>O<br>P | HIGH-VOLTAGE<br>WRITE CYCLE |
|                       | 0                      | 1 | 0 | 1 | A                | A | A | A |                  | 1                  | 0 | 0 | 0 | R            | R | 0 | 0 |                  |                  |                             |

**SYMBOL TABLE**

| WAVEFORM | INPUTS                      | OUTPUTS                       |
|----------|-----------------------------|-------------------------------|
|          | Must be steady              | Will be steady                |
|          | May change from Low to High | Will change from Low to High  |
|          | May change from High to Low | Will change from High to Low  |
|          | Don't Care: Changes Allowed | Changing: State Not Known     |
|          | N/A                         | Center Line is High Impedance |

**Guidelines for Calculating Typical Values of Bus Pull-Up Resistors**



**ABSOLUTE MAXIMUM RATINGS**

Temperature under bias ..... -65°C to +135°C  
 Storage temperature ..... -65°C to +150°C  
 Voltage on SDA, SCL or any address  
 input with respect to V<sub>SS</sub>..... -1V to +7V  
 Voltage on V+ (referenced to V<sub>SS</sub>)..... 10V  
 Voltage on V- (referenced to V<sub>SS</sub>).....-10V  
 (V+) - (V-) ..... 12V  
 Any V<sub>H</sub>/R<sub>H</sub>, V<sub>L</sub>/R<sub>L</sub>, V<sub>W</sub>/R<sub>W</sub> ..... V- to V+  
 Lead temperature (soldering, 10s) ..... 300°C  
 I<sub>W</sub> (10s) ..... ±6mA

**COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

| Temp       | Min.  | Max.  |
|------------|-------|-------|
| Commercial | 0°C   | +70°C |
| Industrial | -40°C | +85°C |

| Device    | Supply Voltage (V <sub>CC</sub> ) Limits |
|-----------|--|
| X9408     | 5V ± 10%                                 |
| X9408-2.7 | 2.7V to 5.5V                             |

**ANALOG CHARACTERISTICS** (Over recommended operating conditions unless otherwise stated.)

| Symbol   | Parameter  | Limits    |          |      |                   | Test Condition   |
|--|--|-----------|----------|------|-------------------|--|
|  |  | Min.      | Typ.     | Max. | Unit              |  |
| R <sub>TOTAL</sub>                             | End to end resistance tolerance  | -20       |          | +20  | %                 |  |
|  | Power rating   |           |          | 50   | mW                | 25°C, each pot   |
| I <sub>W</sub>                                 | Wiper current  | -3        |          | +3   | mA                |  |
| R <sub>W</sub>                                 | Wiper resistance   |           | 150      | 250  | Ω                 | I <sub>W</sub> = ± 1mA @ V+, V- = ±3V  |
|  |  |           | 40       | 100  | Ω                 | I <sub>W</sub> = ± 1mA @ V+, V- = ±5V  |
| V <sub>V+</sub>                                | Voltage on V+ pin  | X9408     | +4.5     | +5.5 | V                 |  |
|  |  | X9408-2.7 | +2.7     | +5.5 |                   |  |
| V <sub>V-</sub>                                | Voltage on V- pin  | X9408     | -5.5     | -4.5 | V                 |  |
|  |  | X9408-2.7 | -5.5     | -2.7 |                   |  |
| V <sub>TERM</sub>                              | Voltage on any V <sub>H</sub> /R <sub>H</sub> , V <sub>L</sub> /R <sub>L</sub> or V <sub>W</sub> /R <sub>W</sub> pin | V-        |          | V+   | V                 |  |
|  | Noise  |           | -120     |      | dBV               | Ref: 1kHz  |
|  | Resolution   |           | 1.6      |      | %                 | See Note 4   |
|  | Absolute linearity <sup>(1)</sup>  | -1        |          | +1   | MI <sup>(3)</sup> | $V(V_{wn}/R_{wn})_{(actual)} - V(V_{wn}/R_{wn})_{(expected)}$ <sup>(4)</sup> |
|  | Relative linearity <sup>(2)</sup>  | -0.2      |          | +0.2 | MI <sup>(3)</sup> | $V(V_{w(n+1)}/R_{w(n+1)}) - [V(V_{w(n)}/R_{w(n)}) + MI]$ <sup>(4)</sup>      |
|  | Temperature coefficient of R <sub>TOTAL</sub>  |           | ±300     |      | ppm/°C            | See Note 4   |
|  | Ratiometric Temperature Coefficient  |           |          | 20   | ppm/°C            | See Note 4   |
| C <sub>H</sub> /C <sub>L</sub> /C <sub>W</sub> | Potentiometer Capacitances   |           | 10/10/25 |      | pF                | See Macro model  |
| I <sub>AL</sub>                                | V <sub>H</sub> /R <sub>H</sub> , V <sub>L</sub> /R <sub>L</sub> , V <sub>W</sub> /R <sub>W</sub> Leakage Current     |           | 0.1      | 10   | μA                | V <sub>IN</sub> = V- to V+. Device is in Stand-by mode.                      |

**D.C. OPERATING CHARACTERISTICS** (Over the recommended operating conditions unless otherwise specified.)

| Symbol           | Parameter  | Limits                |      |                       |      | Test Conditions   |
|------------------|--|-----------------------|------|-----------------------|------|---|
|                  |  | Min.                  | Typ. | Max.                  | Unit |   |
| I <sub>CC1</sub> | V <sub>CC</sub> supply current (nonvolatile write)       |                       |      | 1                     | mA   | f <sub>SCL</sub> = 400kHz, SDA = Open, Other Inputs = V <sub>SS</sub> |
| I <sub>CC2</sub> | V <sub>CC</sub> supply current (move wiper, write, read) |                       |      | 100                   | μA   | f <sub>SCL</sub> = 400kHz, SDA = Open, Other Inputs = V <sub>SS</sub> |
| I <sub>SB</sub>  | V <sub>CC</sub> current (standby)                        |                       |      | 1                     | μA   | SCL = SDA = V <sub>CC</sub> , Addr. = V <sub>SS</sub>                 |
| I <sub>LI</sub>  | Input leakage current                                    |                       |      | 10                    | μA   | V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>                  |
| I <sub>LO</sub>  | Output leakage current                                   |                       |      | 10                    | μA   | V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>                 |
| V <sub>IH</sub>  | Input HIGH voltage                                       | V <sub>CC</sub> × 0.7 |      | V <sub>CC</sub> + 0.5 | V    |   |
| V <sub>IL</sub>  | Input LOW voltage  | -0.5                  |      | V <sub>CC</sub> × 0.1 | V    |   |
| V <sub>OL</sub>  | Output LOW voltage                                       |                       |      | 0.4                   | V    | I <sub>OL</sub> = 3mA   |

- Notes:** (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.  
 (2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.  
 (3) MI = RTOT / 63 or [V(V<sub>H</sub>/R<sub>H</sub>) - V(V<sub>L</sub>/R<sub>L</sub>)] / 63, single pot

**ENDURANCE AND DATA RETENTION**

| Parameter         | Min.    | Unit                              |
|-------------------|---------|-----------------------------------|
| Minimum endurance | 100,000 | Data changes per bit per register |
| Data retention    | 100     | years                             |

**CAPACITANCE**

| Symbol                          | Test  | Max. | Unit | Test Condition        |
|---------------------------------|---|------|------|-----------------------|
| C <sub>I/O</sub> <sup>(4)</sup> | Input/output capacitance (SDA)              | 8    | pF   | V <sub>I/O</sub> = 0V |
| C <sub>IN</sub> <sup>(4)</sup>  | Input capacitance (A0, A1, A2, A3, and SCL) | 6    | pF   | V <sub>IN</sub> = 0V  |

**POWER-UP TIMING**

| Symbol  | Parameter                                 | Min. | Max. | Unit   |
|---|---|------|------|--------|
| t <sub>PUR</sub> <sup>(5)</sup>               | Power-up to initiation of read operation  |      | 1    | ms     |
| t <sub>PUW</sub> <sup>(5)</sup>               | Power-up to initiation of write operation |      | 5    | ms     |
| t <sub>R</sub> V <sub>CC</sub> <sup>(6)</sup> | V <sub>CC</sub> Power-up Ramp             | 0.2  | 50   | V/msec |

**Power-up Requirements** (Power-up sequencing can affect correct recall of the wiper registers)

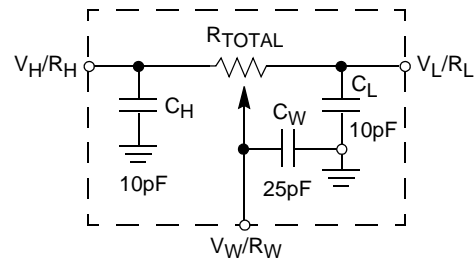
The preferred power-on sequence is as follows: First V<sub>-</sub>, then V<sub>CC</sub> and V<sub>+</sub>, and then the potentiometer pins, V<sub>H</sub>/R<sub>H</sub>, V<sub>L</sub>/R<sub>L</sub>, and V<sub>W</sub>/R<sub>W</sub>. Voltage should not be applied to the potentiometer pins before V<sub>+</sub> or V<sub>-</sub> is applied. The V<sub>CC</sub> ramp rate specification should be met, and any glitches or slope changes in the V<sub>CC</sub> line should be held to <100mV if possible. If V<sub>CC</sub> powers down, it should be held below 0.1V for more than 1 second before powering up again in order for proper wiper register recall. Also, V<sub>CC</sub> should not reverse polarity by more than 0.5V. Recall of wiper position will not be complete until V<sub>CC</sub>, V<sub>+</sub> and V<sub>-</sub> reach their final value.

- Notes:** (4) This parameter is periodically sampled and not 100% tested  
 (5) t<sub>PUR</sub> and t<sub>PUW</sub> are the delays required from the time the third (last) power supply (V<sub>CC</sub>, V<sub>+</sub> or V<sub>-</sub>) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.  
 (6) This is not a tested or guaranteed parameter and should only be used as a guidance.

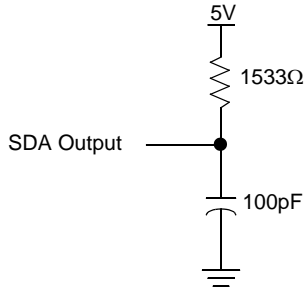
**A.C. TEST CONDITIONS**

|                               |  |
|-------------------------------|--|
| Input pulse levels            | $V_{CC} \times 0.1$ to $V_{CC} \times 0.9$ |
| Input rise and fall times     | 10ns                                       |
| Input and output timing level | $V_{CC} \times 0.5$                        |

**Circuit #3 SPICE Macro Model**



**EQUIVALENT A.C. LOAD CIRCUIT**



**AC TIMING (over recommended operating condition)**

| Symbol       | Parameter   | Min. | Max. | Unit |
|--------------|---|------|------|------|
| $f_{SCL}$    | Clock frequency                                       |      | 400  | kHz  |
| $t_{CYC}$    | Clock cycle time                                      | 2500 |      | ns   |
| $t_{HIGH}$   | Clock high time                                       | 600  |      | ns   |
| $t_{LOW}$    | Clock low time  | 1300 |      | ns   |
| $t_{SU:STA}$ | Start setup time                                      | 600  |      | ns   |
| $t_{HD:STA}$ | Start hold time                                       | 600  |      | ns   |
| $t_{SU:STO}$ | Stop setup time                                       | 600  |      | ns   |
| $t_{SU:DAT}$ | SDA data input setup time                             | 100  |      | ns   |
| $t_{HD:DAT}$ | SDA data input hold time                              | 30   |      | ns   |
| $t_R$        | SCL and SDA rise time                                 |      | 300  | ns   |
| $t_F$        | SCL and SDA fall time                                 |      | 300  | ns   |
| $t_{AA}$     | SCL low to SDA data output valid time                 |      | 900  | ns   |
| $t_{DH}$     | SDA Data output hold time                             | 50   |      | ns   |
| $T_I$        | Noise suppression time constant at SCL and SDA inputs | 50   |      | ns   |
| $t_{BUF}$    | Bus free time (prior to any transmission)             | 1300 |      | ns   |
| $t_{SU:WPA}$ | $\overline{WP}$ , A0, A1, A2 and A3 setup time        | 0    |      | ns   |
| $t_{HD:WPA}$ | $\overline{WP}$ , A0, A1, A2 and A3 hold time         | 0    |      | ns   |

**HIGH-VOLTAGE WRITE CYCLE TIMING**

| Symbol   | Parameter  | Typ. | Max. | Unit |
|----------|--|------|------|------|
| $t_{WR}$ | High-voltage write cycle time (store instructions) | 5    | 10   | ms   |

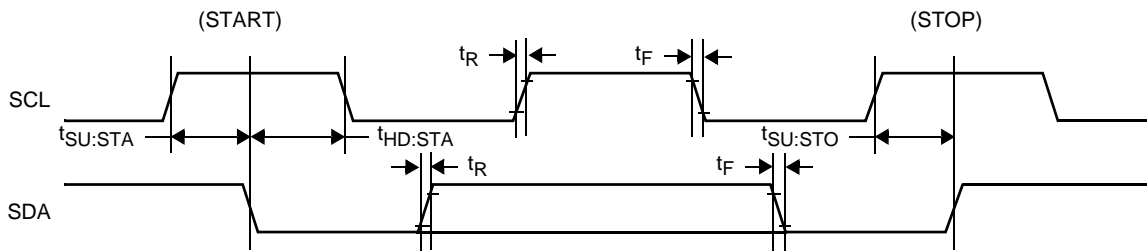
**XDCP TIMING**

| Symbol     | Parameter   | Min. | Max. | Unit          |
|------------|---|------|------|---------------|
| $t_{WRPO}$ | Wiper response time after the third (last) power supply is stable                 |      | 10   | $\mu\text{s}$ |
| $t_{WRL}$  | Wiper response time after instruction issued (all load instructions)              |      | 10   | $\mu\text{s}$ |
| $t_{WRID}$ | Wiper response time from an active SCL/SCK edge (increment/decrement instruction) |      | 10   | $\mu\text{s}$ |

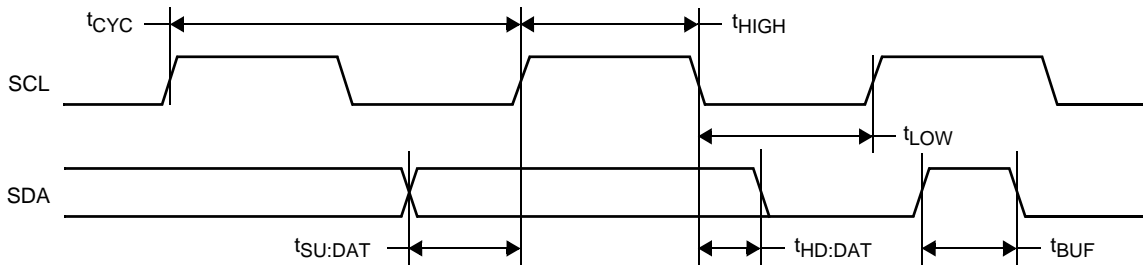
**Notes:** (9) A device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

**TIMING DIAGRAMS**

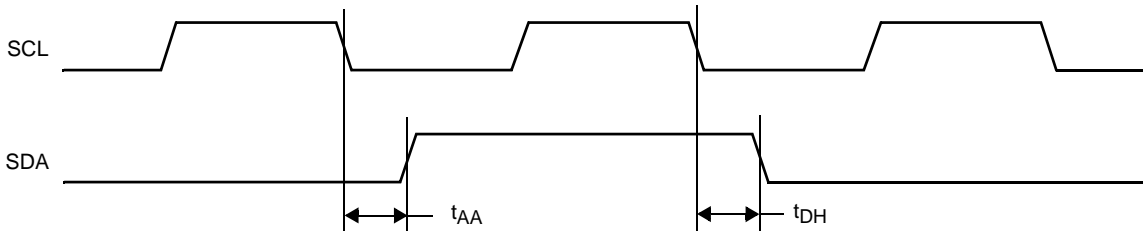
**START and STOP Timing**



**Input Timing**

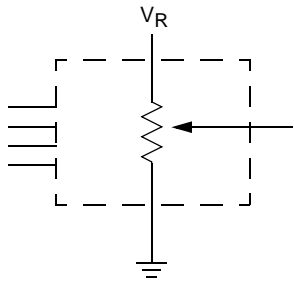


**Output Timing**

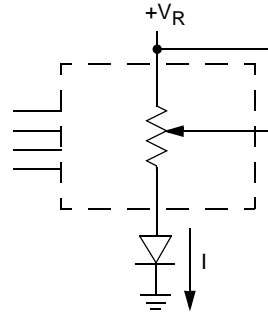


APPLICATIONS INFORMATION

Basic Configurations of Electronic Potentiometers



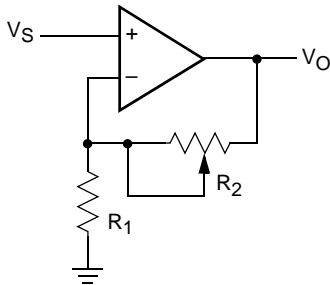
Three terminal Potentiometer;  
Variable voltage divider



Two terminal Variable Resistor;  
Variable current

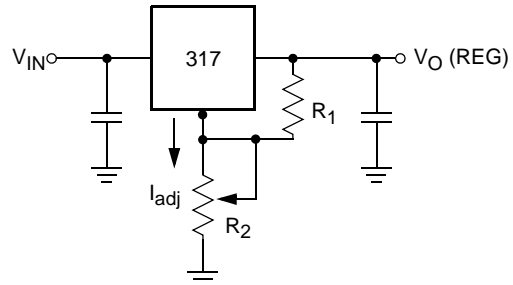
Application Circuits

Noninverting Amplifier



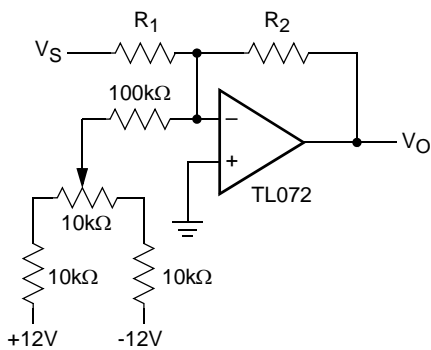
$$V_O = (1 + R_2/R_1)V_S$$

Voltage Regulator

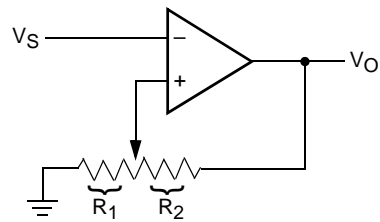


$$V_O (REG) = 1.25V (1 + R_2/R_1) + I_{adj} R_2$$

Offset Voltage Adjustment



Comparator with Hysteresis



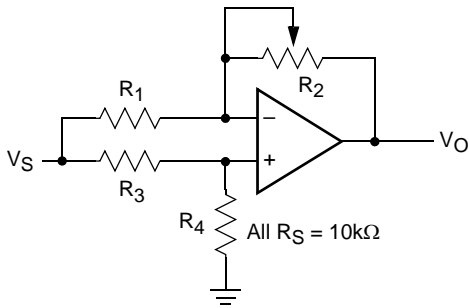
$$V_{UL} = \{R_1/(R_1 + R_2)\} V_O(\max)$$

$$V_{LL} = \{R_1/(R_1 + R_2)\} V_O(\min)$$



Application Circuits (continued)

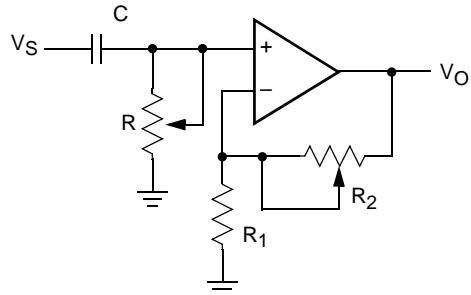
Attenuator



$$V_O = G V_S$$

$$-1/2 \leq G \leq +1/2$$

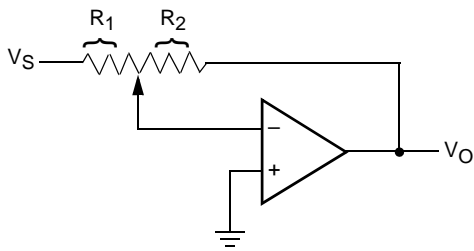
Filter



$$G_O = 1 + R_2/R_1$$

$$f_c = 1/(2\pi RC)$$

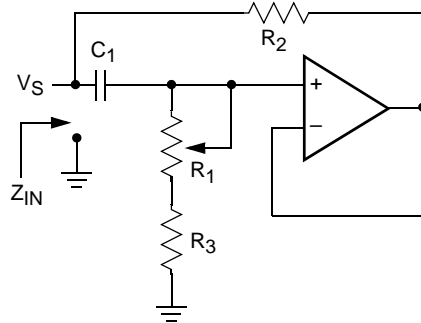
Inverting Amplifier



$$V_O = G V_S$$

$$G = -R_2/R_1$$

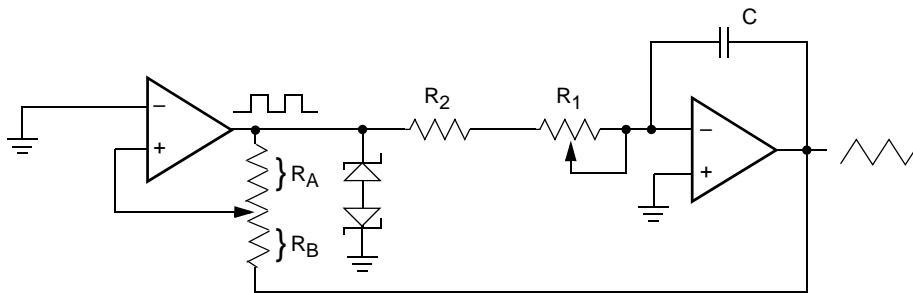
Equivalent L-R Circuit



$$Z_{IN} = R_2 + s R_2 (R_1 + R_3) C_1 = R_2 + s L_{eq}$$

$$(R_1 + R_3) \gg R_2$$

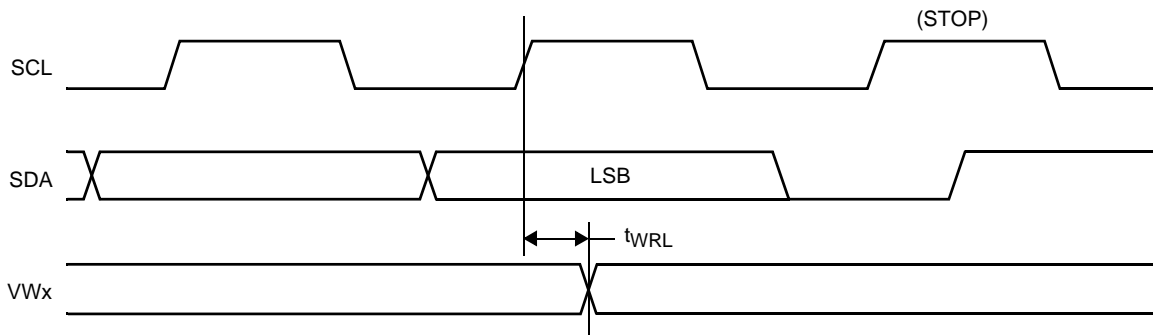
Function Generator



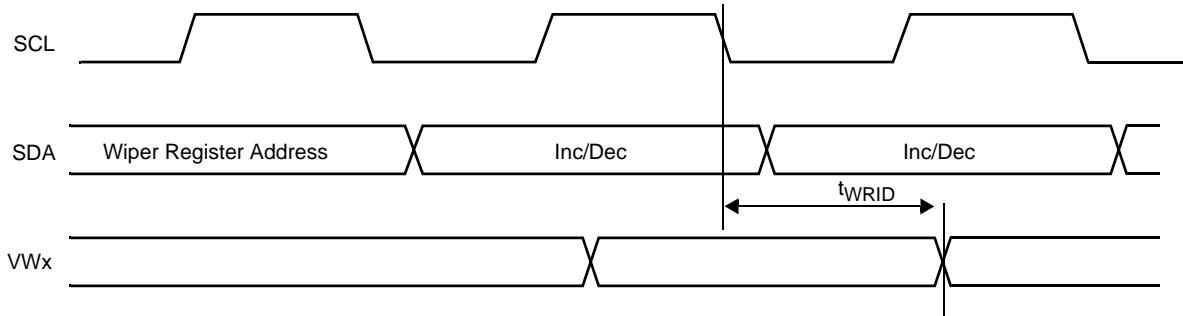
$$\text{frequency} \propto R_1, R_2, C$$

$$\text{amplitude} \propto R_A, R_B$$

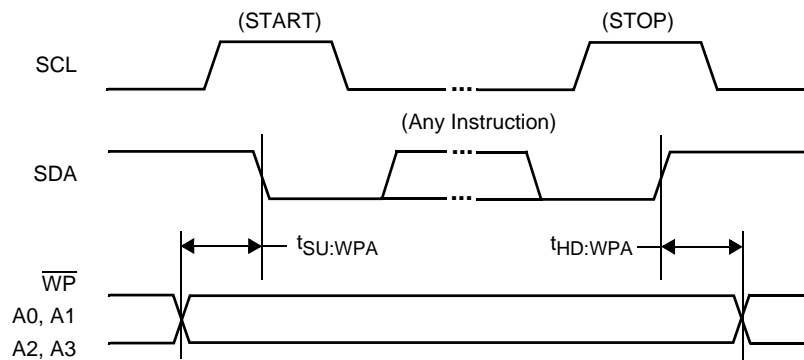
**XDCP Timing (for All Load Instructions)**



**XDCP Timing (for Increment/Decrement Instruction)**

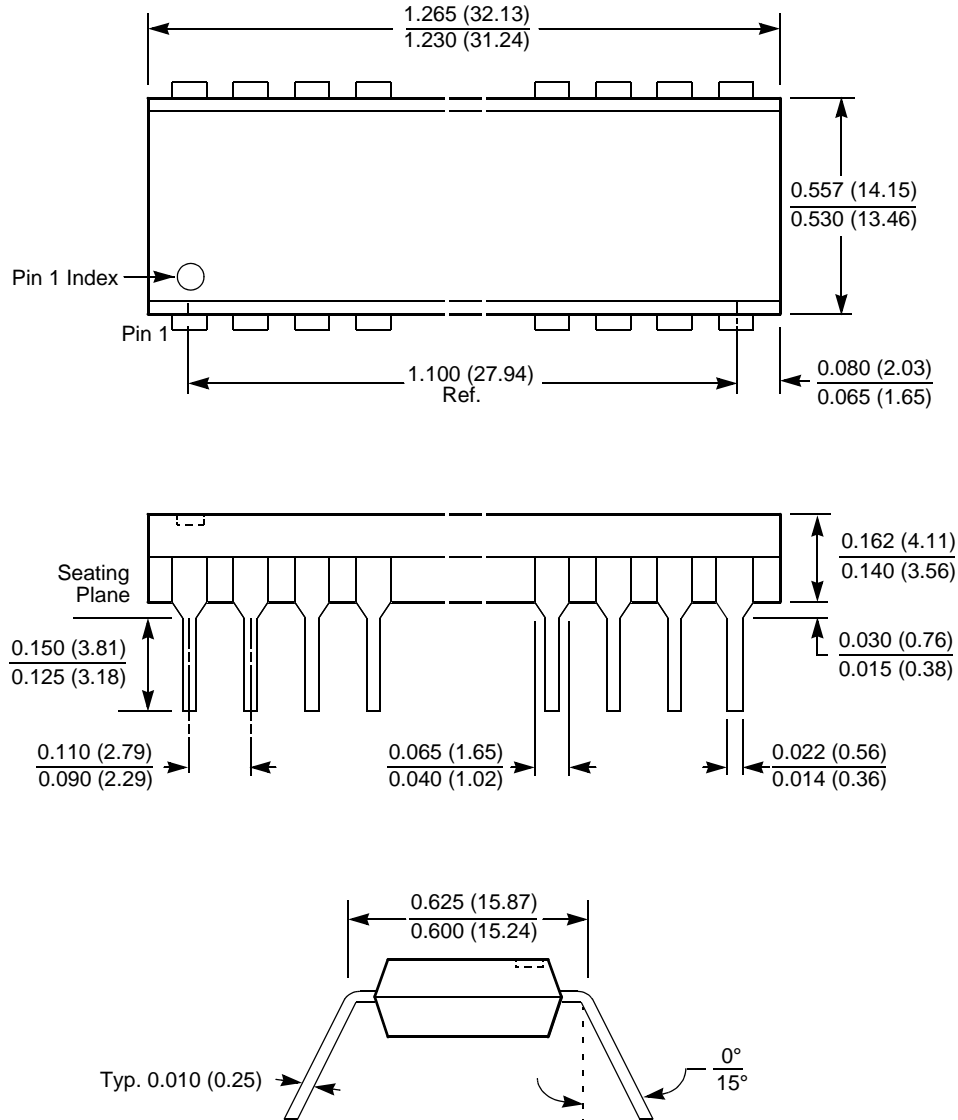


**Write Protect and Device Address Pins Timing**



PACKAGING INFORMATION

24-Lead Plastic Dual In-Line Package Type P

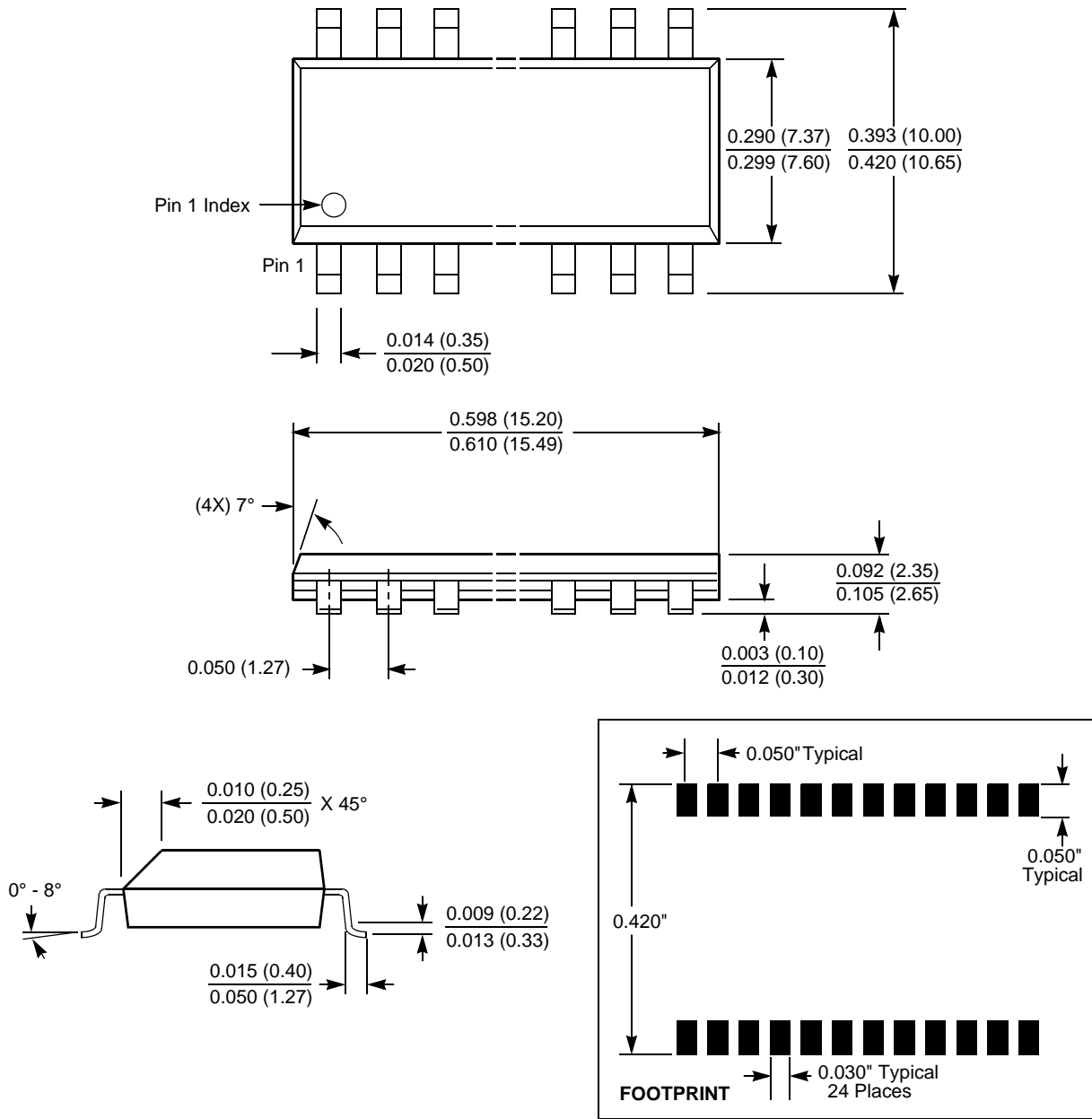


NOTE:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

PACKAGING INFORMATION

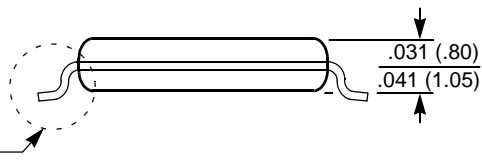
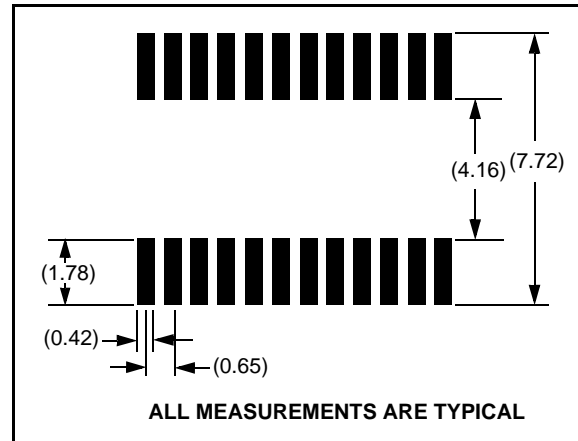
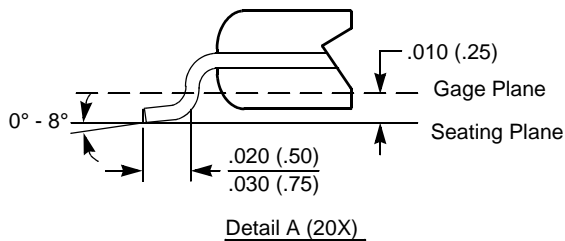
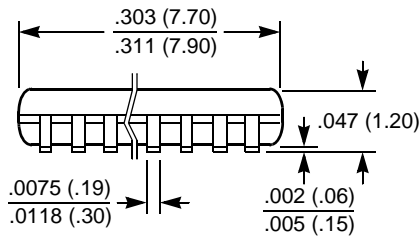
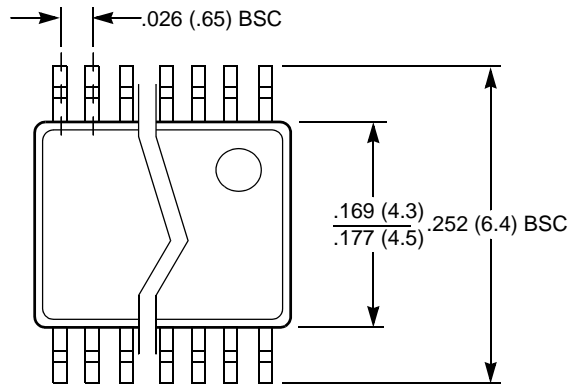
24-Lead Plastic Small Outline Gull Wing Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

24-Lead Plastic, TSSOP Package Type V



See Detail "A"

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)