



REVISION HISTORY

| <u>Revision</u> | <u>Description</u> | <u>Issue Date</u> |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|
| Rev. 1.0 | Initial Issue | Jul.25.2004 |
| Rev. 1.1 | Adding PKG type : 32 P-DIP Revised Test Condition of I _{SB1} /I _{DR} | May.14.2007 |
| Rev. 1.2 | Deleted L Spec. Added SL Spec. Revised V _{TERM} to V _{T1} and V _{T2} Revised Test Condition of I _{CC} | Nov.8.2007 |
| Rev. 1.3 | Revised I _{SB1} /I _{DR} | Mar.21.2008 |
| Rev. 1.4 | Adding PKG type : 44 TSOP-II | Jul.14.2008 |
| Rev. 1.5 | Added I _{SB1} /I _{DR} values when T _A = 25°C and T _A = 40°C Revised <u>FEATURES & ORDERING INFORMATION</u> <u>Lead free and green package available to Green package available</u> Added packing type in <u>ORDERING INFORMATION</u> Deleted T _{SOLDER} in <u>ABSOLUTE MAXIMUM RATINGS</u> | Mar.30.2009 |
| Rev. 1.6 | Added PKG type : 32 TSOP-II | Jun.22.2009 |
| Rev. 1.7 | Deleted PKG type : 32 TSOP-II | Jul.17.2009 |
| Rev. 1.8 | Revised <u>PACKAGE OUTLINE DIMENSION</u> in page 10/11/12/13 | May.7.2010 |
| Rev. 1.9 | Revised <u>ORDERING INFORMATION</u> in page 15 Revised <u>PACKAGE OUTLINE DIMENSION</u> in page 9 | Aug.30.2010 |
| Rev. 1.10 | Added PKG type : 32 TSOP-II | Nov.1.2010 |
| Rev. 1.11 | Revised <u>ORDERING INFORMATION</u> in page 16 | Mar.9.2011 |
| Rev. 1.12 | Deleted PKG type : 44 TSOP-II | Feb.21.2012 |

FEATURES

- Fast access time : 45/55/70ns
- Low power consumption:
 Operating current : 40/30/20mA (TYP.)
 Standby current : 2 μ A (TYP.) LL-version
 1 μ A (TYP.) SL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 32-pin 450 mil SOP
 32-pin 8mm x 20mm TSOP-I
 32-pin 8mm x 13.4mm STSOP
 36-ball 6mm x 8mm TFBGA
 32-pin 600 mil P-DIP
 32-pin 400 mil TSOP-II

GENERAL DESCRIPTION

The LY62L5128 is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

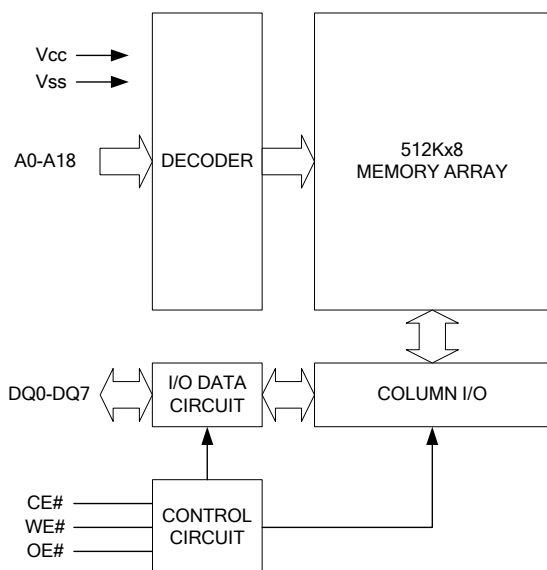
The LY62L5128 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L5128 operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed | Power Dissipation | |
|----------------|-----------------------|------------|------------|-----------------------------|---------------------|
| | | | | Standby(Isb1,TYP.) | Operating(Icc,TYP.) |
| LY62L5128 | 0 ~ 70°C | 2.7 ~ 3.6V | 45/55/70ns | 2 μ A(LL)/1 μ A(SL) | 40/30/20mA |
| LY62L5128(E) | -20 ~ 80°C | 2.7 ~ 3.6V | 45/55/70ns | 2 μ A(LL)/1 μ A(SL) | 40/30/20mA |
| LY62L5128(I) | -40 ~ 85°C | 2.7 ~ 3.6V | 45/55/70ns | 2 μ A(LL)/1 μ A(SL) | 40/30/20mA |

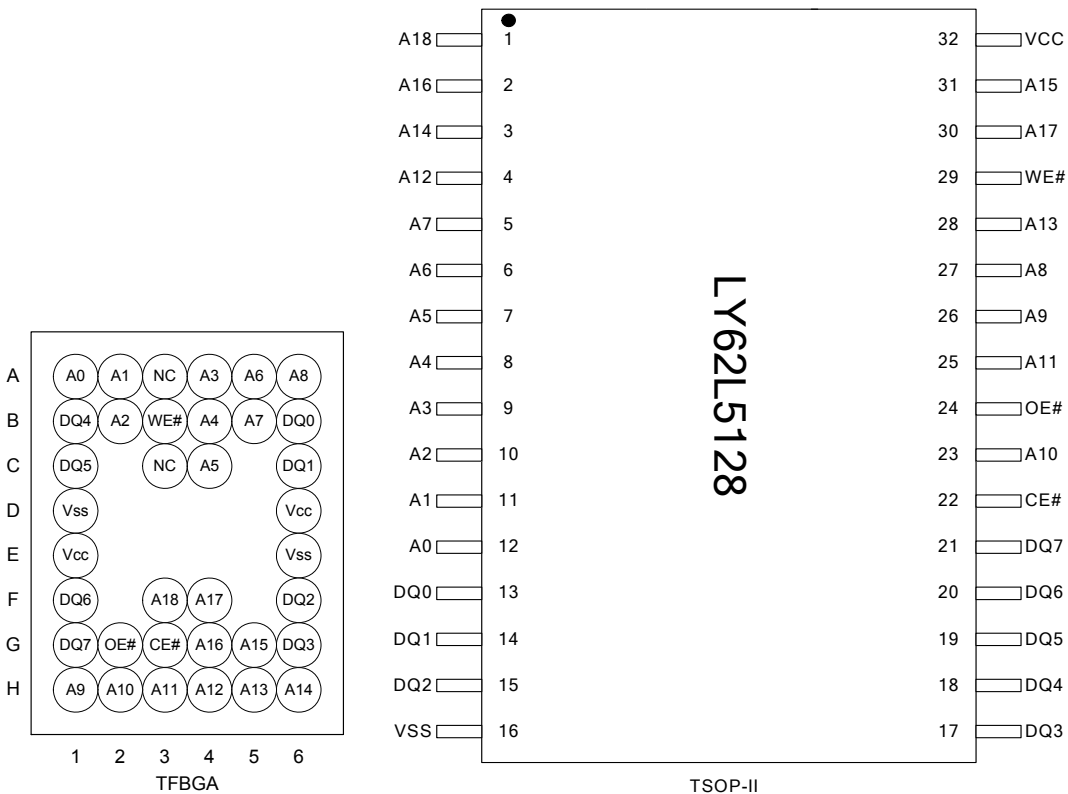
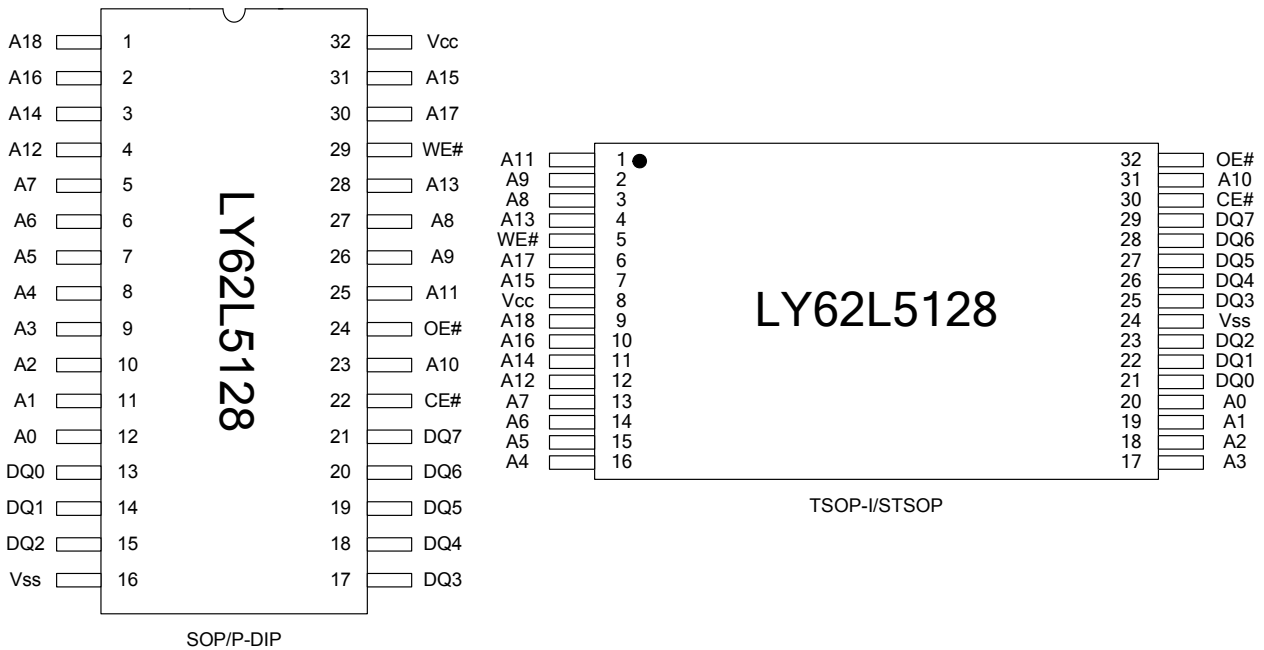
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|-----------|---------------------|
| A0 - A18 | Address Inputs |
| DQ0 - DQ7 | Data Inputs/Outputs |
| CE# | Chip Enable Inputs |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| Vcc | Power Supply |
| Vss | Ground |
| NC | No Connection |

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYMBOL | RATING | UNIT |
|------------------------------------------|------------------|--------------------|------|
| Voltage on Vcc relative to Vss | V _{T1} | -0.5 to 4.6 | V |
| Voltage on any other pin relative to Vss | V _{T2} | -0.5 to Vcc+0.5 | V |
| Operating Temperature | T _A | 0 to 70(C grade) | °C |
| | | -20 to 80(E grade) | |
| | | -40 to 85(I grade) | |
| Storage Temperature | T _{STG} | -65 to 150 | °C |
| Power Dissipation | P _D | 1 | W |
| DC Output Current | I _{OUT} | 50 | mA |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

| MODE | CE# | OE# | WE# | I/O OPERATION | SUPPLY CURRENT |
|----------------|-----|-----|-----|------------------|------------------------------------|
| Standby | H | X | X | High-Z | I _{SB} , I _{SB1} |
| Output Disable | L | H | H | High-Z | I _{CC} , I _{CC1} |
| Read | L | L | H | D _{OUT} | I _{CC} , I _{CC1} |
| Write | L | X | L | D _{IN} | I _{CC} , I _{CC1} |

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. ⁴ | MAX. | UNIT | | |
|----------------------------------------|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-------------------|----------------------|------|----|----|
| Supply Voltage | V _{CC} | | 2.7 | 3.0 | 3.6 | V | | |
| Input High Voltage | V _{IH} ¹ | | 2.2 | - | V _{CC} +0.3 | V | | |
| Input Low Voltage | V _{IL} ² | | - 0.2 | - | 0.6 | V | | |
| Input Leakage Current | I _{LI} | V _{CC} ≥ V _{IN} ≥ V _{SS} | - 1 | - | 1 | μA | | |
| Output Leakage Current | I _{LO} | V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled | - 1 | - | 1 | μA | | |
| Output High Voltage | V _{OH} | I _{OH} = -1mA | 2.2 | 2.7 | - | V | | |
| Output Low Voltage | V _{OL} | I _{OL} = 2mA | - | - | 0.4 | V | | |
| Average Operating Power supply Current | I _{CC} | Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA Other pins at V _{IL} or V _{IH} | - 45 | - | 40 | 50 | mA | |
| | | | - 55 | - | 30 | 40 | mA | |
| | | | - 70 | - | 20 | 30 | mA | |
| | I _{CC1} | Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V,, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V | - | 4 | 5 | mA | | |
| Standby Power Supply Current | I _{SB} | CE# = V _{IH} or CE2 = V _{IL} , other pins at V _{IL} or V _{IH} | - | 0.3 | 1.25 | mA | | |
| | I _{SB1} | CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Others at 0.2V or V _{CC} - 0.2V | LL | - | 2 | 15 | μA | |
| | | | LLE/LLI | - | 2 | 20 | μA | |
| | | | SL ^{*5} | 25°C | - | 1 | 3 | μA |
| | | | SLE ^{*5} | | - | 1 | 3 | μA |
| | | | SLI ^{*5} | 40°C | - | 1 | 3 | μA |
| | | | SL | | - | 1 | 10 | μA |
| SLE/SLI | - | 1 | 12 | μA | | | | |

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

| PARAMETER | SYMBOL | MIN. | MAX | UNIT |
|--------------------------|------------------|------|-----|------|
| Input Capacitance | C _{IN} | - | 6 | pF |
| Input/Output Capacitance | C _{I/O} | - | 8 | pF |

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

| | |
|------------------------------------------|---------------------------------------------------------------------------|
| Input Pulse Levels | 0.2V to V _{CC} - 0.2V |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA |

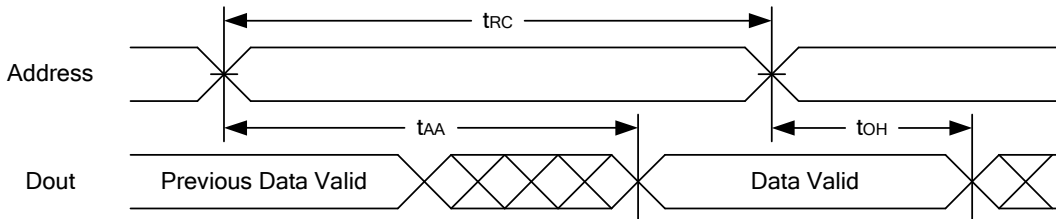
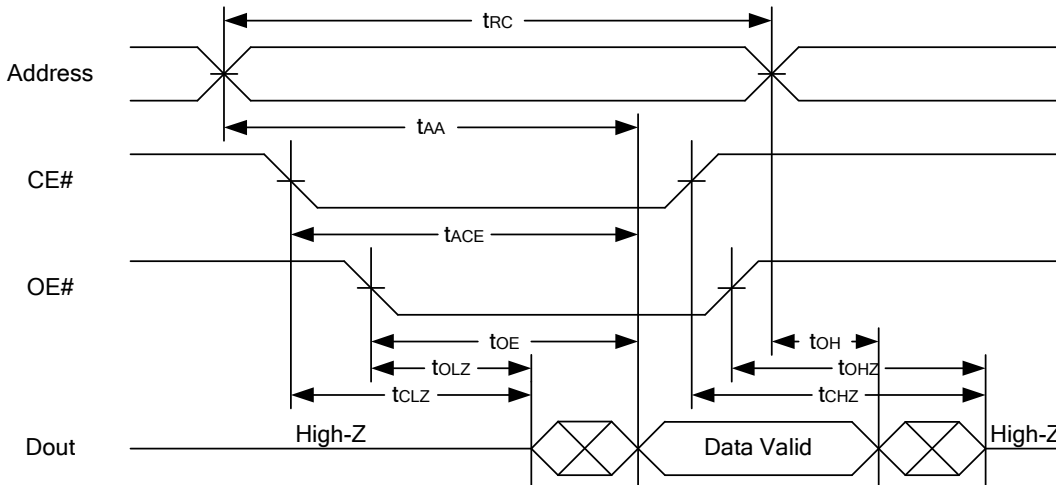
AC ELECTRICAL CHARACTERISTICS
(1) READ CYCLE

| PARAMETER | SYM. | LY62L5128-45 | | LY62L5128-55 | | LY62L5128-70 | | UNIT |
|------------------------------------|--------------------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | t _{RC} | 45 | - | 55 | - | 70 | - | ns |
| Address Access Time | t _{AA} | - | 45 | - | 55 | - | 70 | ns |
| Chip Enable Access Time | t _{ACE} | - | 45 | - | 55 | - | 70 | ns |
| Output Enable Access Time | t _{OE} | - | 25 | - | 30 | - | 35 | ns |
| Chip Enable to Output in Low-Z | t _{CLZ} * | 10 | - | 10 | - | 10 | - | ns |
| Output Enable to Output in Low-Z | t _{OLZ} * | 5 | - | 5 | - | 5 | - | ns |
| Chip Disable to Output in High-Z | t _{CHZ} * | - | 15 | - | 20 | - | 25 | ns |
| Output Disable to Output in High-Z | t _{OHZ} * | - | 15 | - | 20 | - | 25 | ns |
| Output Hold from Address Change | t _{OH} | 10 | - | 10 | - | 10 | - | ns |

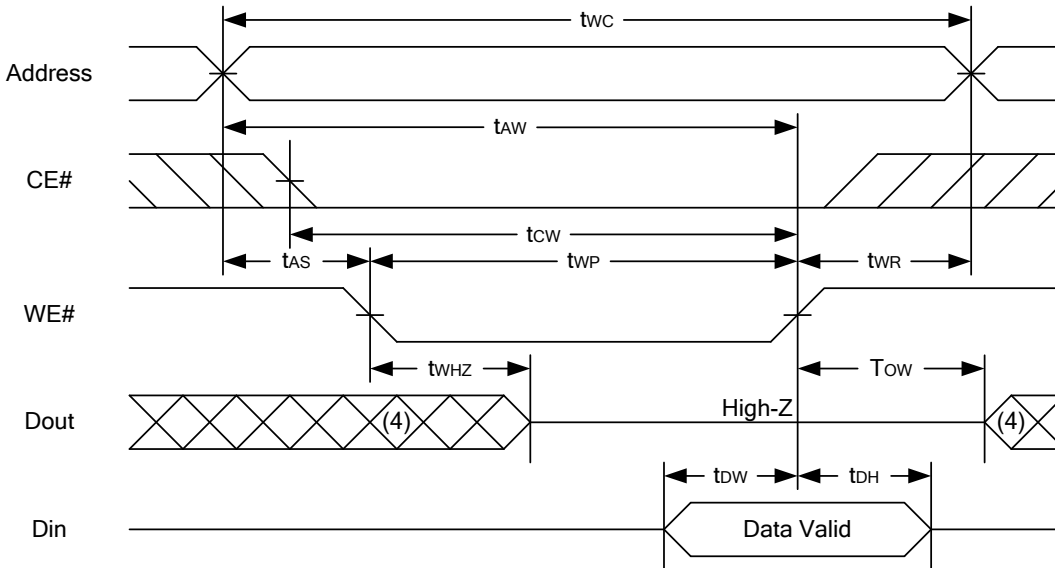
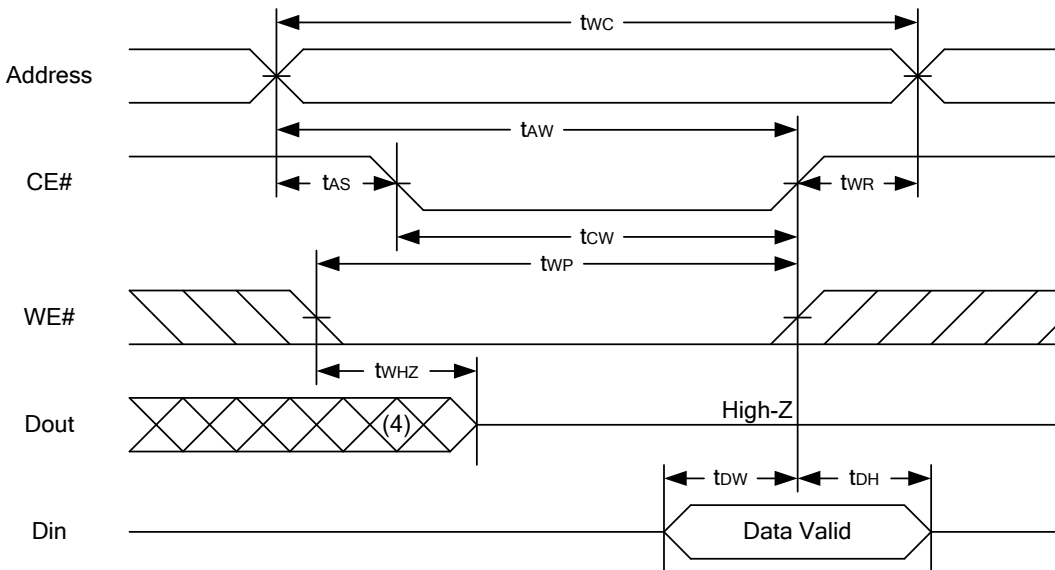
(2) WRITE CYCLE

| PARAMETER | SYM. | LY62L5128-45 | | LY62L5128-55 | | LY62L5128-70 | | UNIT |
|----------------------------------|--------------------|--------------|------|--------------|------|--------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Write Cycle Time | t _{WC} | 45 | - | 55 | - | 70 | - | ns |
| Address Valid to End of Write | t _{AW} | 40 | - | 50 | - | 60 | - | ns |
| Chip Enable to End of Write | t _{CW} | 40 | - | 50 | - | 60 | - | ns |
| Address Set-up Time | t _{AS} | 0 | - | 0 | - | 0 | - | ns |
| Write Pulse Width | t _{WP} | 35 | - | 45 | - | 55 | - | ns |
| Write Recovery Time | t _{WR} | 0 | - | 0 | - | 0 | - | ns |
| Data to Write Time Overlap | t _{DW} | 20 | - | 25 | - | 30 | - | ns |
| Data Hold from End of Write Time | t _{DH} | 0 | - | 0 | - | 0 | - | ns |
| Output Active from End of Write | t _{OW} * | 5 | - | 5 | - | 5 | - | ns |
| Write to Output in High-Z | t _{WHZ} * | - | 15 | - | 20 | - | 25 | ns |

*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS
READ CYCLE 1 (Address Controlled) (1,2)

READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

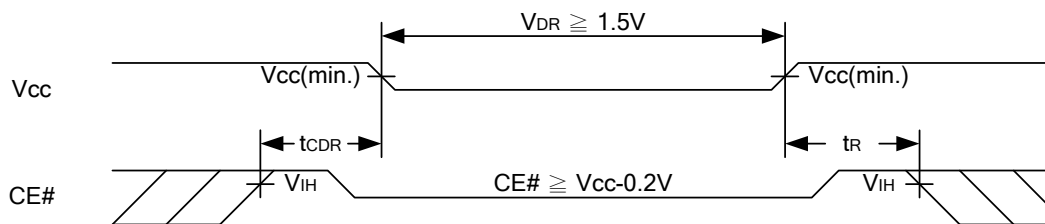
WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)

WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)

Notes :

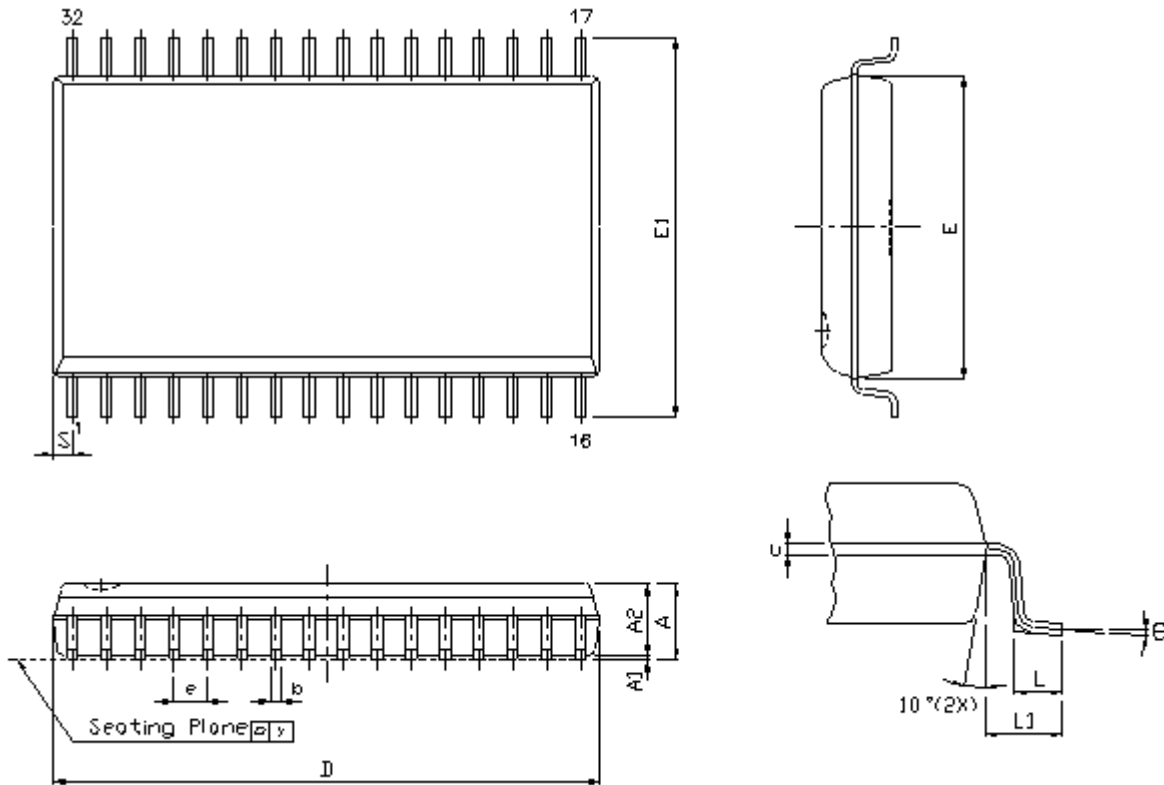
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

DATA RETENTION CHARACTERISTICS

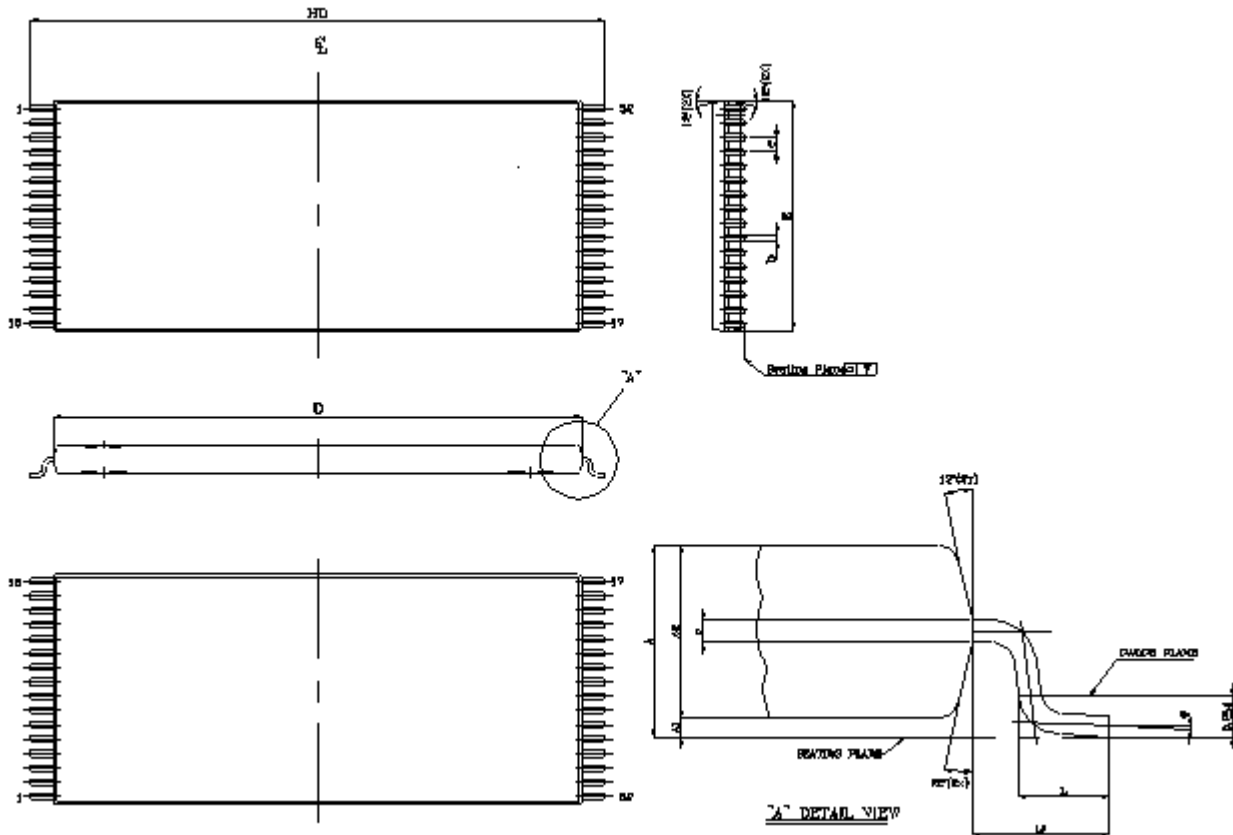
| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT | | |
|-------------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------|------------------|------|------|------|-----|----|
| V _{CC} for Data Retention | V _{DR} | CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V | 1.5 | - | 3.6 | V | | |
| Data Retention Current | I _{DR} | V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V | LL | - | 1.0 | 12 | μA | |
| | | | LLE/LLI | - | 1.0 | 16 | μA | |
| | | | SL | 25°C | - | 0.5 | 2.5 | μA |
| | | | SLE | 40°C | - | 0.5 | 2.5 | μA |
| | | | SLI | | - | 0.5 | 2.5 | μA |
| | | | SL | - | 0.5 | 8 | μA | |
| SLE/SLI | - | 0.5 | 10 | μA | | | | |
| Chip Disable to Data Retention Time | t _{CDR} | See Data Retention Waveforms (below) | 0 | - | - | ns | | |
| Recovery Time | t _R | | t _{RC*} | - | - | ns | | |

 t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM


PACKAGE OUTLINE DIMENSION
32 pin 450 mil SOP Package Outline Dimension


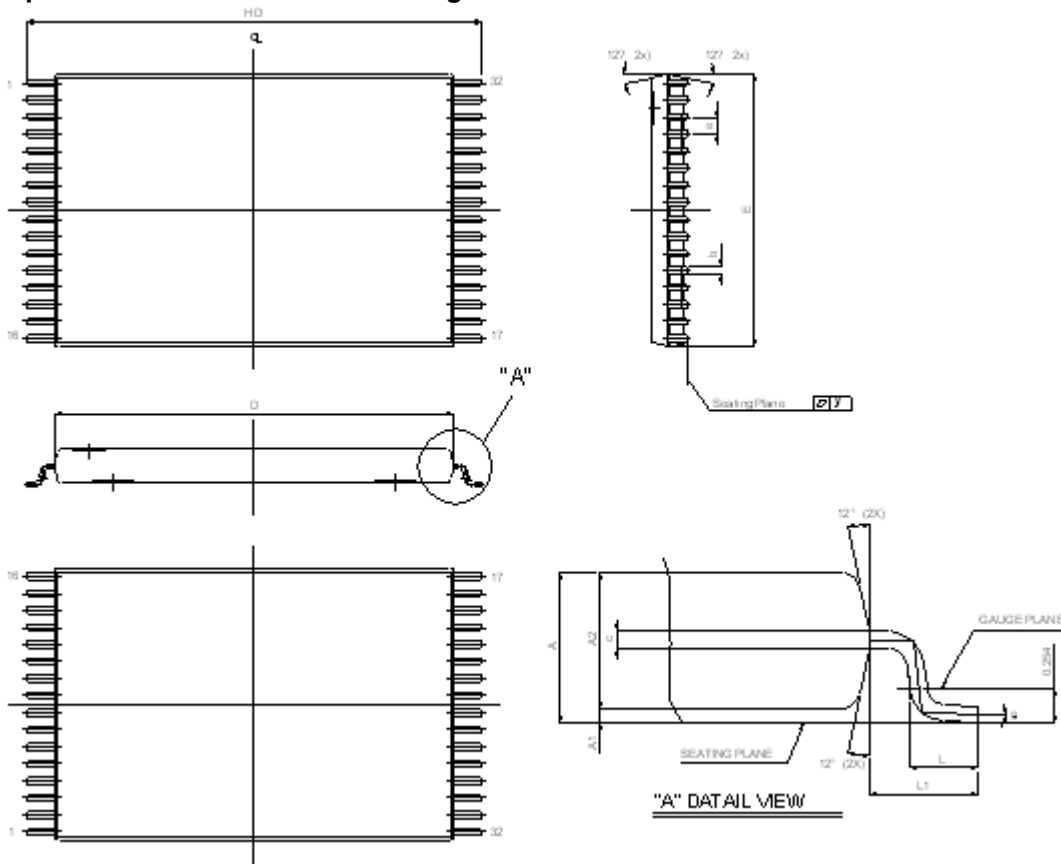
| SYM. | UNIT | INCH.(BASE) | MM(REF) |
|------|------|-------------|--------------|
| A | | 0.120(MAX) | 3.048(MAX) |
| A1 | | 0.004(MIN) | 0.102(MIN) |
| A2 | | 0.116(MAX) | 2.946(MAX) |
| b | | 0.016(TYP) | 0.406(TYP) |
| c | | 0.008(TYP) | 0.203(TYP) |
| D | | 0.817(MAX) | 20.75(MAX) |
| E | | 0.445±0.006 | 11.303±0.152 |
| E1 | | 0.555±0.025 | 14.097±0.635 |
| e | | 0.050(TYP) | 1.270(TYP) |
| L | | 0.033±0.017 | 0.838±0.432 |
| L1 | | 0.055±0.008 | 1.397±0.203 |
| S | | 0.026(MAX) | 0.660(MAX) |
| y | | 0.004(MAX) | 0.101(MAX) |
| Θ | | 0° -10° | 0° -10° |

32 pin 8mm x 20mm TSOP-I Package Outline Dimension


| SYM. | UNIT | INCH(BASE) | MM(REF) |
|------|------|---------------|--------------|
| A | | 0.047 (MAX) | 1.20 (MAX) |
| A1 | | 0.004 ±0.002 | 0.10 ±0.05 |
| A2 | | 0.039 ±0.002 | 1.00 ±0.05 |
| b | | 0.009 ±0.002 | 0.22 ±0.05 |
| c | | 0.006 ±0.002 | 0.155 ±0.055 |
| D | | 0.724 ±0.008 | 18.40 ±0.20 |
| E | | 0.315 ±0.008 | 8.00 ±0.20 |
| e | | 0.020 (TYP) | 0.50 (TYP) |
| HD | | 0.787 ±0.008 | 20.00 ±0.20 |
| L | | 0.024 ±0.004 | 0.60 ±0.10 |
| L1 | | 0.0315 ±0.004 | 0.08 ±0.10 |
| y | | 0.003 (MAX) | 0.08 (MAX) |
| Θ | | 0°~5° | 0°~5° |



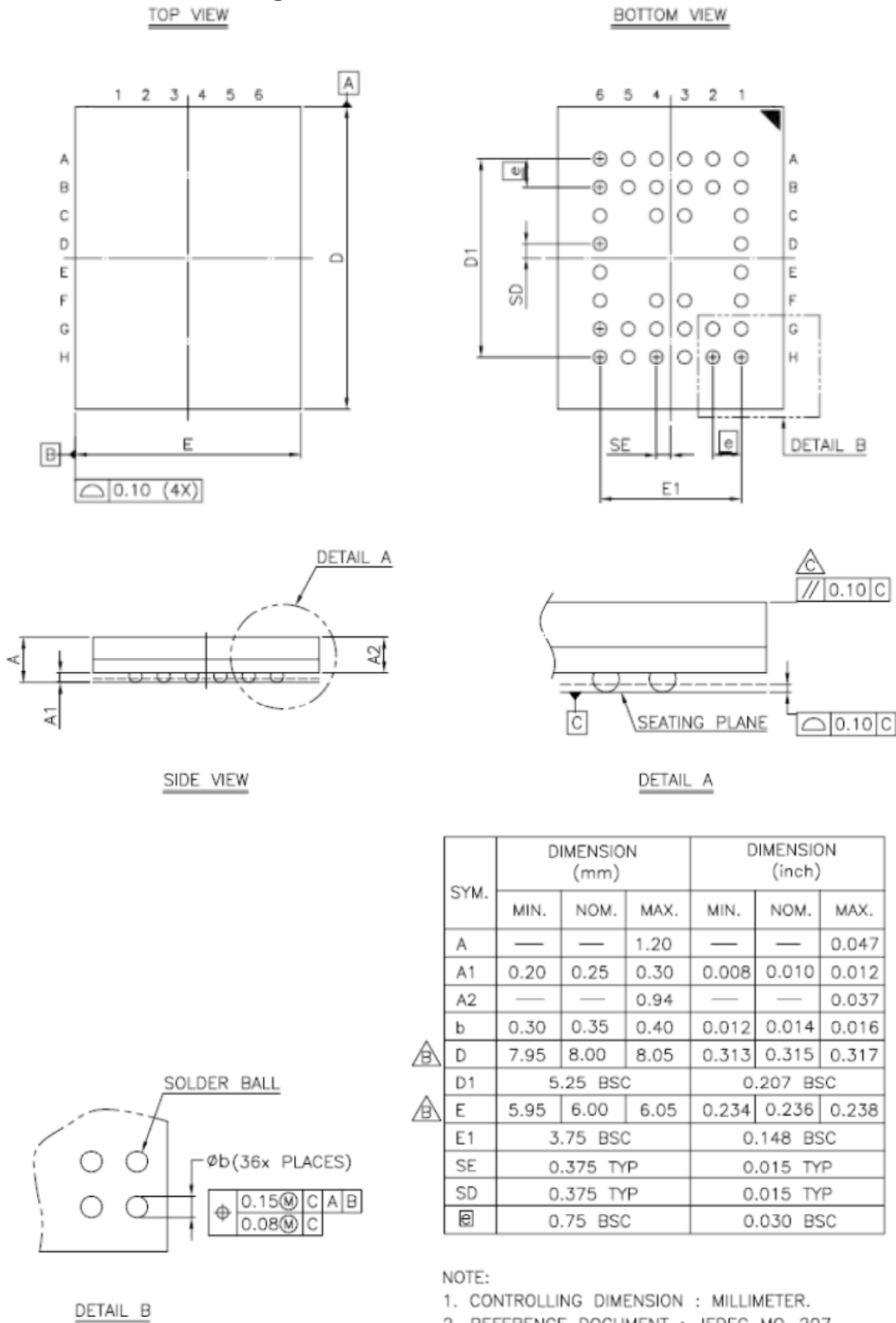
32 pin 8mm x 13.4mm STSOP Package Outline Dimension

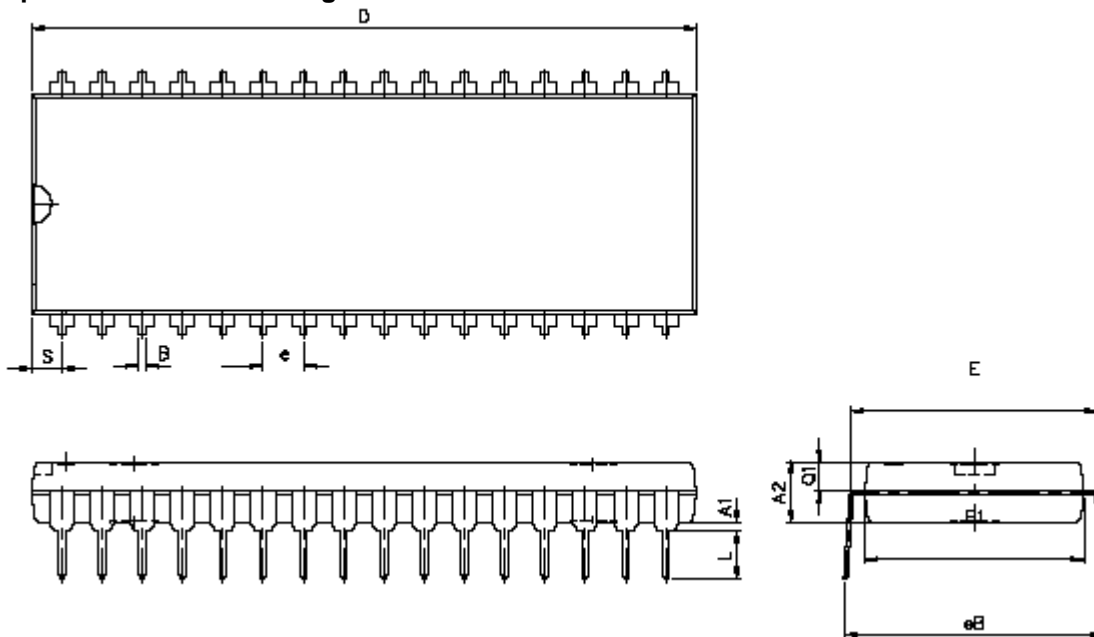


| SYM. | UNIT | |
|------|--------------|--------------|
| | INCH(BASE) | MM(REF) |
| A | 0.049 (MAX) | 1.25 (MAX) |
| A1 | 0.004 ±0.002 | 0.10 ±0.05 |
| A2 | 0.039 ±0.002 | 1.00 ±0.05 |
| b | 0.009 ±0.002 | 0.22 ±0.05 |
| c | 0.006 ±0.002 | 0.155 ±0.055 |
| D | 0.465 ±0.008 | 11.80 ±0.20 |
| E | 0.315 ±0.008 | 8.00 ±0.20 |
| e | 0.020 (TYP) | 0.50 (TYP) |
| HD | 0.528±0.008 | 13.40 ±0.20. |
| L | 0.02 ±0.008 | 0.50 ±0.20 |
| L1 | 0.031 ±0.005 | 0.8 ±0.125 |
| y | 0.003 (MAX) | 0.076 (MAX) |
| Θ | 0°~5° | 0°~5° |



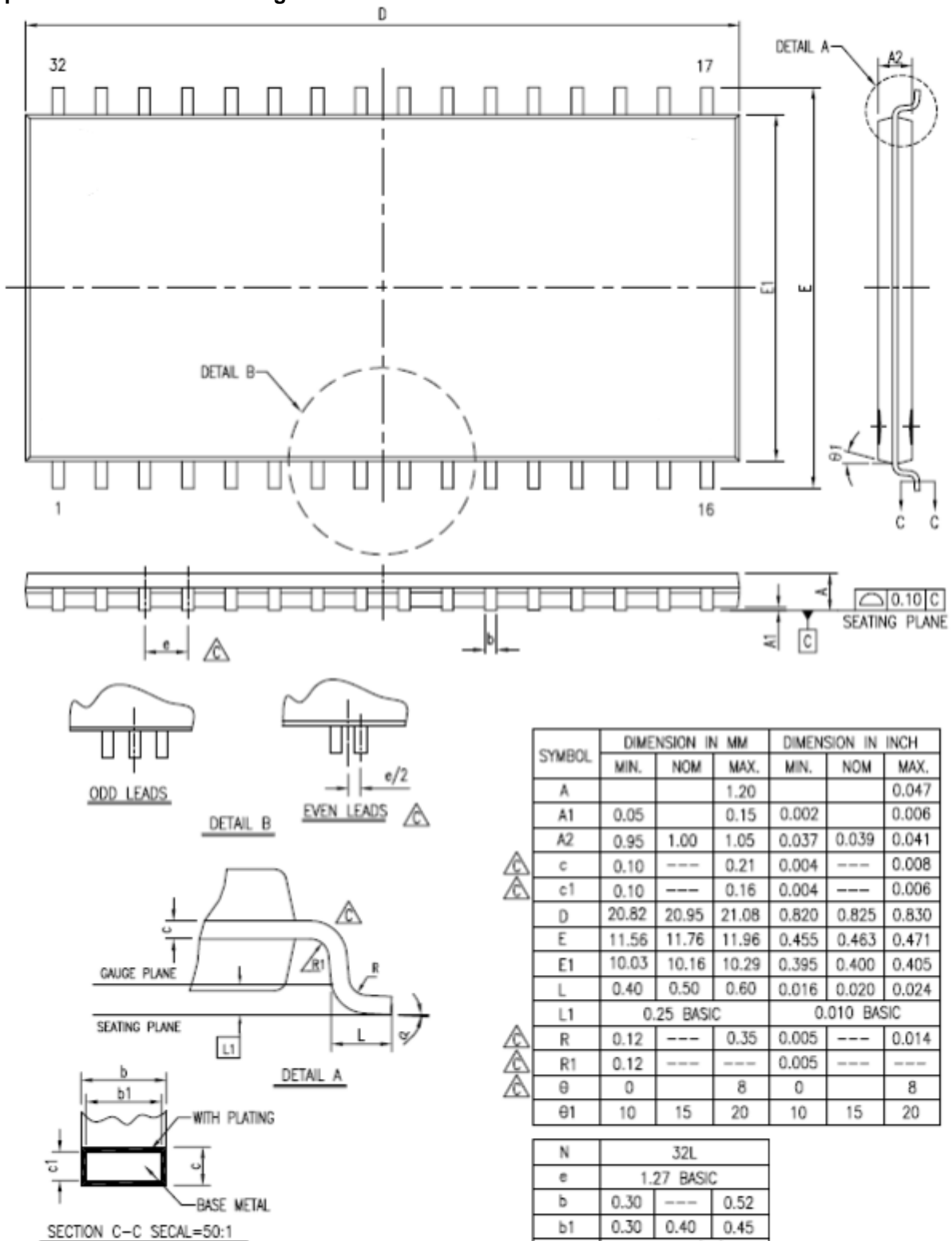
36 ball 6mm x 8mm TFBGA Package Outline Dimension



32 pin 600 mil P-DIP Package Outline Dimension


| SYM. | UNIT | INCH(BASE) | MM(REF) |
|------|------|-------------|---------------|
| A1 | | 0.015(MIN) | 0.381(MIN) |
| A2 | | 0.155±0.005 | 3.937±0.127 |
| B | | 0.018±0.005 | 0.457±0.127 |
| D | | 1.650±0.01 | 41.910±0.254 |
| E | | 0.600±0.010 | 15.240±0.254 |
| E1 | | 0.545±0.005 | 13.843±0.127 |
| e | | 0.100(TYP) | 2.540(TYP) |
| eB | | 0.650±0.020 | 16.510±0.508. |
| L | | 0.158±0.043 | 4.013±1.092 |
| S | | 0.075±0.010 | 1.905±0.254 |
| Q1 | | 0.070±0.005 | 1.778±0.127 |

Note : D/E1/S dimension do not include mold flash.

32-pin 400mil TSOP-II Package Outline Dimension


NOTE : DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSIONS.
 D AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.



ORDERING INFORMATION

LY62L5128 U V - WW XX Y Z

Z : Packing Type

Blank : Tube or Tray
Tube : 32-pin 450 mil SOP
 32-pin 600 mil P-DIP
Tray : 32-pin 8 mm x 20 mm TSOP-I
 32-pin 8 mm x 13.4 mm STSOP
 36-ball 6 mm x 8 mm TFBGA
 32-pin 400 mil TSOP-II
T : Tape Reel

Y : Temperature Range

Blank : (Commercial) 0°C ~ 70°C
E : (Extended) -20°C ~ 80°C
I : (Industrial) -40°C ~ 85°C

XX : Power Type

LL : Ultra Low Power
SL : Special Ultra Low Power

WW : Access Time(Speed)

V : Lead Information

L : Green Package

U : Package Type

S : 32-pin 450 mil SOP
L : 32-pin 8 mm x 20 mm TSOP-I
R : 32-pin 8 mm x 13.4 mm STSOP
G : 36-ball 6 mm x 8 mm TFBGA
P : 32-pin 600 mil P-DIP
W : 32-pin 400 mil TSOP-II



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