LP5907 用于 RF 和模拟电路的超低噪声、250mA 线性稳压器 - 无需旁路电容

1 特性

- 输入电压范围：2.2V 至 5.5V
- 输出电压范围：1.2V 至 4.5V
- 输出电流：250mA
- 与 1µF 陶瓷输入和输出电容搭配使用，性能稳定
- 无需噪声旁路电容
- 支持远距离安置输出电容
- 热过载保护和短路保护
- 运行结温范围：–40°C 到 125 C
- 低输出电压噪声：< 10μV_{RMS}
- 电源抑制比 (PSRR)：1kHz 频率时为 82dB
- 输出电压容差：±2%
- 几乎零 IQ（禁用时）：< 1µA
- 极低 I_Q（使能时）：12µA
- 启动时间：80µs
- 低压降：120mV（典型值）

2 应用

- 手机
- PDA 手持终端
- 无线局域网 (LAN) 设备

3 说明

LP5907 是一款能够提供 250mA 输出电流的线性稳压器。 此器件专门针对 RF 和模拟电路而设计，可满足其低噪声、高 PSRR、低静态电流以及低线路或负载瞬态响应系数等诸多要求。 LP5907 采用创新的设计技术，无需噪声旁路电容便可提供出色的噪声性能，并且支持远距离安置输出电容。

此器件设计为与 1µF 输入和 1µF 输出陶瓷电容搭配使用（无需独立的噪声旁路电容）。

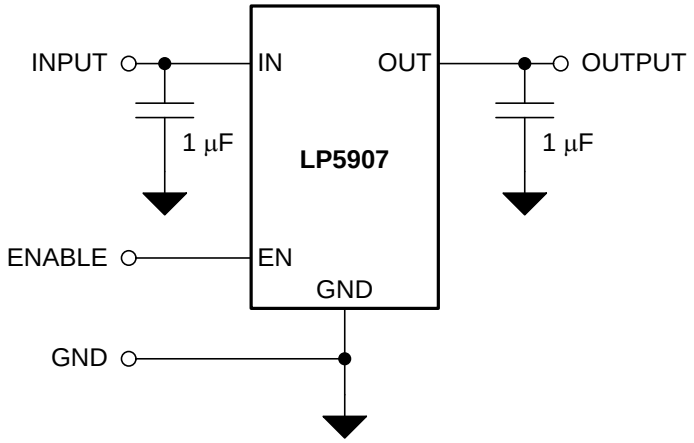
其固定输出电压介于 1.20V 和 4.50V 之间（以 25mV 为单位增量）。 如需特定的电压选项，请联系德州仪器 (TI) 销售代表。

器件信息(1)

器件型号	封装	封装尺寸
LP5907	DSBGA (4)	0.675mm x 0.675mm（最大值）
	SOT-23 (5)	2.90mm x 1.60mm（标称值）
	X2SON (4)	1.00mm x 1.00mm（标称值）

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

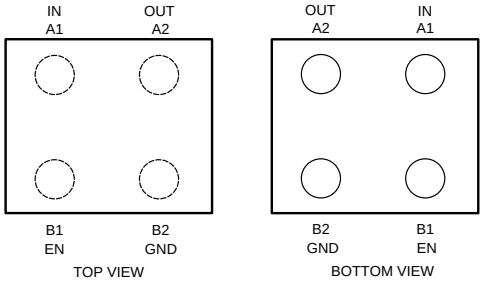
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (October 2013) to Revision H **Page**

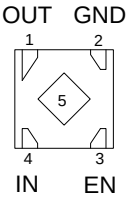
- 已添加 *器件信息*和*处理额定值表*，*特性描述*，*器件功能模式*，*应用和实施*，*电源相关建议*，*布局*，*器件和文档支持*，以及*机械、封装和可订购信息*部分；已将一些曲线移至*应用曲线*部分。 1

5 Pin Configuration and Functions

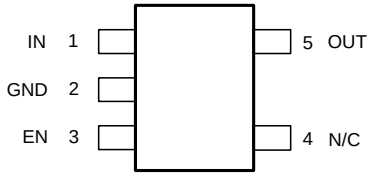
Ultra-Thin DSBGA (YKE)
4 Pins



X2SON (DQN)
4 Pins
Bottom View



SOT-23 (DBV)
5 Pins
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DSBGA NUMBER	X2SON NUMBER	SOT-23 NUMBER		
IN	A1	4	1	I	Input voltage supply. A 1-µF capacitor should be connected at this input.
OUT	A2	1	5	O	Regulated output voltage. A minimum 1-µF low-ESR capacitor should be connected to this pin. Connect this output to the load circuit. An internal 230-Ω (typical) pull-down resistor prevents a charge remaining on V_{OUT} when the regulator is in the shutdown mode (V_{EN} low).
EN	B1	3	3	I	Enable input. A low voltage (< V_{IL}) on this pin turns the regulator off and discharges the output pin to GND through an internal 230-Ω pull-down resistor. A high voltage (> V_{IH}) on this pin enables the regulator output. This pin has an internal 1M-Ω pull-down resistor to hold the regulator off by default.
GND	B2	2	2	—	Common ground
N/C	N/A	N/A	4	—	No internal electrical connection.
Thermal Pad	N/A	5	N/A	—	Thermal pad for X2SON package, connect to GND or leave floating. Do not connect to any potential other than GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3 to (V_{IN} + 0.3 V)	6	
V_{EN}	Enable input voltage	–0.3to (V_{IN} + 0.3 V)	6	
	Continuous power dissipation(4)	Internally Limited		W
T_{JMAX}	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military or Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) All voltages are with respect to the GND pin.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN}	Input supply voltage	2.2	5.5	V
V_{EN}	Enable input voltage	0 to (V_{IN} + 0.3)	5.5	
I_{OUT}	Output current	0	250	mA
T_J	Junction temperature	–40	125	°C
T_A	Ambient temperature(3)	–40	85	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (TA-MAX) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times PD\text{-}MAX)$. See *Application Information*.

6.4 Thermal Information

THERMAL METRIC[1]		LP5907			UNIT
		SOT-23 (DBV)	X2SON (DQN)	DSBGA (YKE)	
		5 PINS	4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.4	216.1	206.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	102.1	161.7	1.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	162.1	37.0	
ψ_{JT}	Junction-to-top characterization parameter	8.4	5.1	15.0	
ψ_{JB}	Junction-to-board characterization parameter	45.3	161.7	36.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	123.0	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, unless otherwise stated.[1][2][3]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	T_A = 25°C	2.2		5.5	V
ΔV_{OUT}	Output voltage tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA to 250 mA, V_{OUT} ≥ 1.8 V	–2		2	%V_{OUT}
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA to 250 mA, V_{OUT} < 1.8 V	–3		3	
	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA		0.02		%/V
	Load regulation	I_{OUT} = 1 mA to 250 mA		0.001		%/mA
I_{LOAD}	Load current	See[4]	0		250	mA
	Maximum output current		250			
I_Q	Quiescent current[5]	V_{EN} = 1.2 V, I_{OUT} = 0 mA		12	25	µA
		V_{EN} = 1.2 V, I_{OUT} = 250 mA		250	425	
		V_{EN} = 0.3 V (Disabled)		0.2	1	
I_G	Ground current[6]	V_{EN} = 1.2 V, I_{OUT} = 0 mA		14		µA
V_{DO}	Dropout voltage[7]	I_{OUT} = 100 mA		50		mV
		I_{OUT} = 250 mA (DSBGA)		120	200	
		I_{OUT} = 250 mA (SOT-23, X2SON packages)			250	
I_{SC}	Short circuit current limit	T_A = 25°C[8]	250	500		mA
PSRR	Power supply rejection ratio[9]	f = 100 Hz, I_{OUT} = 20 mA		90		dB
		f = 1 kHz, I_{OUT} = 20 mA		82		
		f = 10 kHz, I_{OUT} = 20 mA		65		
		f = 100 kHz, I_{OUT} = 20 mA		60		

(1) All voltages are with respect to the device GND terminal, unless otherwise stated.
(2) Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature (T_J) range of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application $R_{\theta JA}$), as given by the following equation: T_{A-MAX} = $T_{J-MAX-OP}$ – ($R_{\theta JA}$ × P_{D-MAX}). See *Applications and Implementation*.
(4) The device maintains a stable, regulated output voltage without a load current.
(5) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.
(6) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
(7) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
(8) Short-circuit current (I_{SC}) for the LP5907 is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100 mV below its nominal voltage.
(9) This specification is verified by design.

Electrical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, unless otherwise stated.(1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
e_N	Output noise voltage(9)	BW = 10 Hz to 100 kHz	I_{OUT} = 1 mA		10		μV_{RMS}
			I_{OUT} = 250 mA		6.5		
R_{AD}	Output Automatic Discharge pull-down resistance	V_{EN} < V_{IL} (output disabled)			230		Ω
T_{SD}	Thermal shutdown	T_J rising			160		°C
	Thermal hysteresis	T_J falling from shutdown			15		
LOGIC INPUT THRESHOLDS							
V_{IL}	Low input threshold	V_{IN} = 2.2 V to 5.5 V V_{EN} falling until the output is disabled				0.4	V
V_{IH}	High input threshold	V_{IN} = 2.2 V to 5.5 V V_{EN} rising until the output is enabled		1.2			V
I_{EN}	Input current at EN pin(10)	V_{EN} = 5.5 V and V_{IN} = 5.5 V			5.5		µA
		V_{EN} = 0 V and V_{IN} = 5.5 V			0.001		
TRANSIENT CHARACTERISTICS							
ΔV_{OUT}	Line transient(9)	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$) + 1.6 V) in 30 µs		–1			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1.6 V) to ($V_{OUT(NOM)}$) + 1.6 V) in 30 µs				1	
	Load transient(9)	I_{OUT} = 1 mA to 250 mA in 10 µs		–40			mV
		I_{OUT} = 250 mA to 1mA in 10 µs				40	
	Overshoot on start-up(9)	Stated as a percentage of $V_{OUT(NOM)}$				5%	
t_{ON}	Turnon time	From V_{EN} > V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$ T_A = 25°C			80	150	µs

(10) There is a 1-MΩ resistor between EN and ground on the device.

6.6 Output and Input Capacitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX	UNIT
C_{IN}	Input capacitance(2)	Capacitance for stability	0.7	1		µF
C_{OUT}	Output capacitance(2)		0.7	1	10	
ESR	Output/Input capacitance(2)		5		500	mΩ

(1) The minimum capacitance should be greater than 0.5 µF over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.
(2) This specification is verified by design.

6.7 Typical Characteristics

Unless otherwise stated: V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C

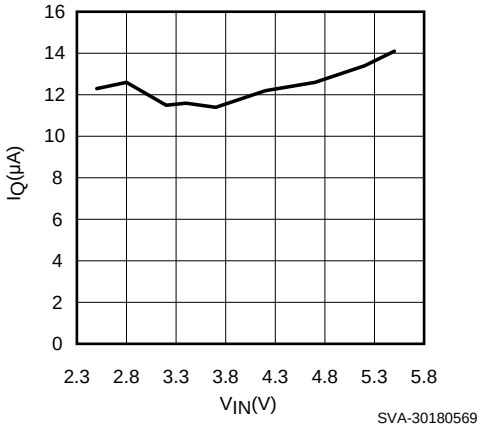


Figure 1. Quiescent Current vs Input Voltage

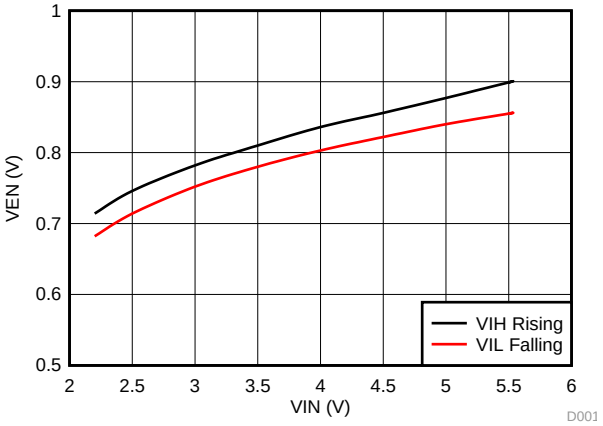


Figure 2. V_{EN} Thresholds vs V_{IN}

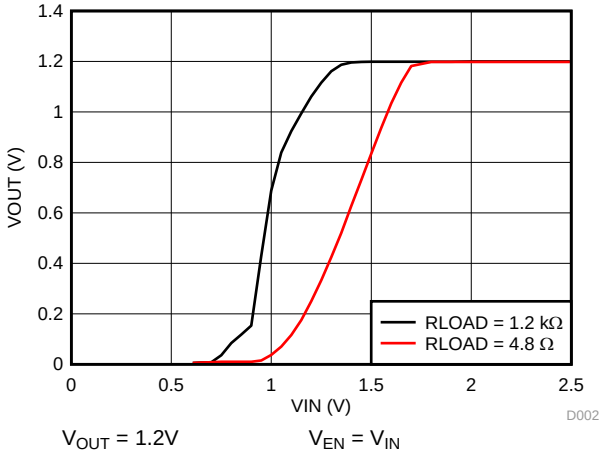


Figure 3. V_{OUT} vs V_{IN}

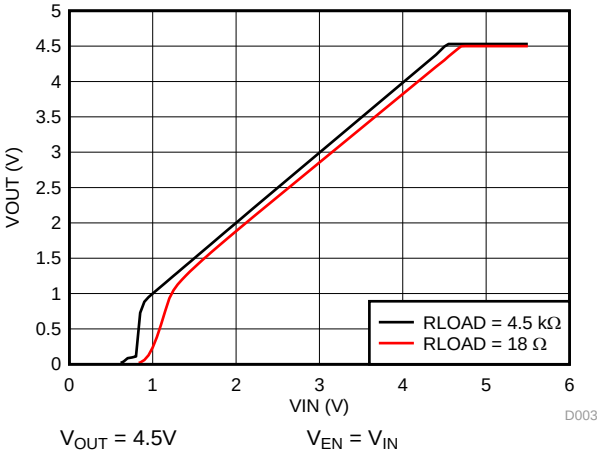


Figure 4. V_{OUT} vs V_{IN}

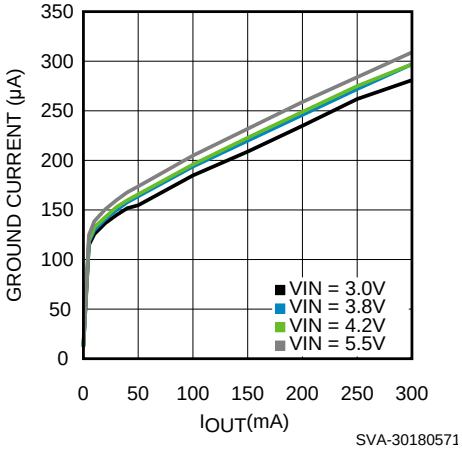


Figure 5. Ground Current vs Output Current

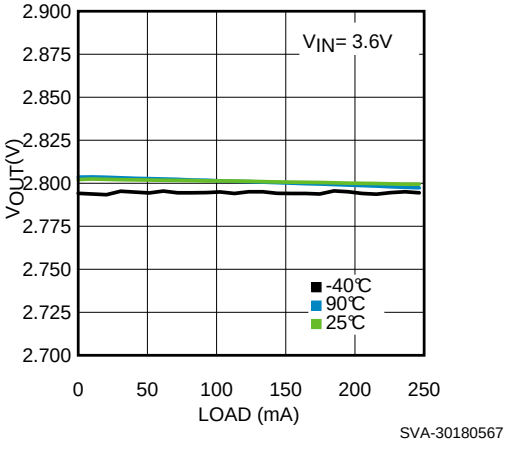


Figure 6. Load Regulation

Typical Characteristics (continued)

Unless otherwise stated: V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C

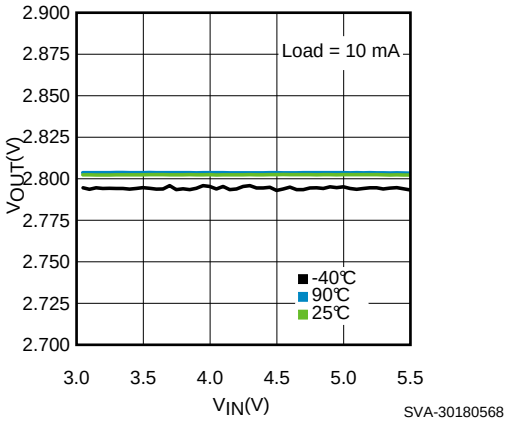


Figure 7. Line Regulation

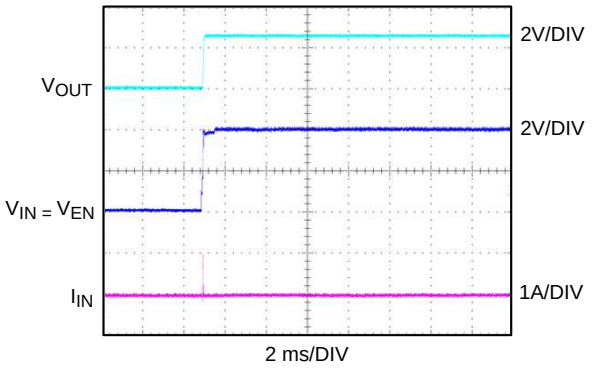
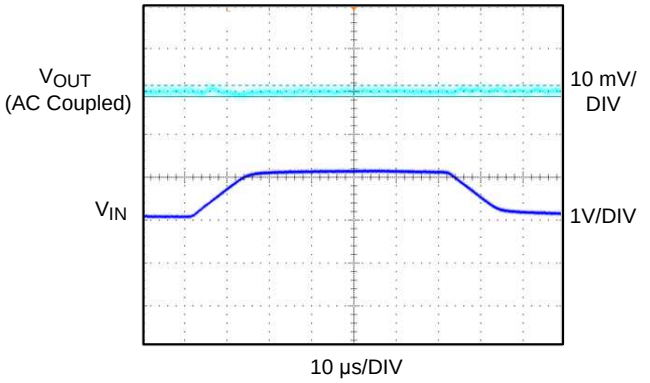
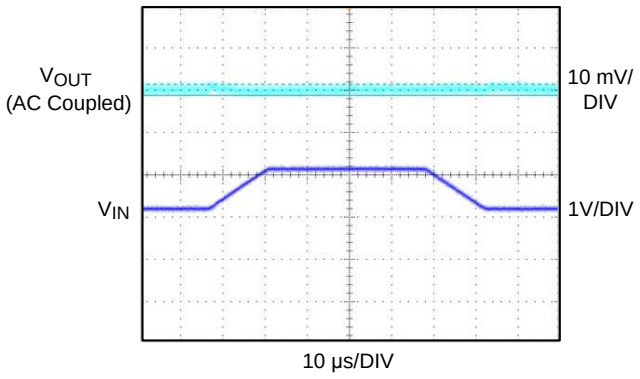


Figure 8. Inrush Current



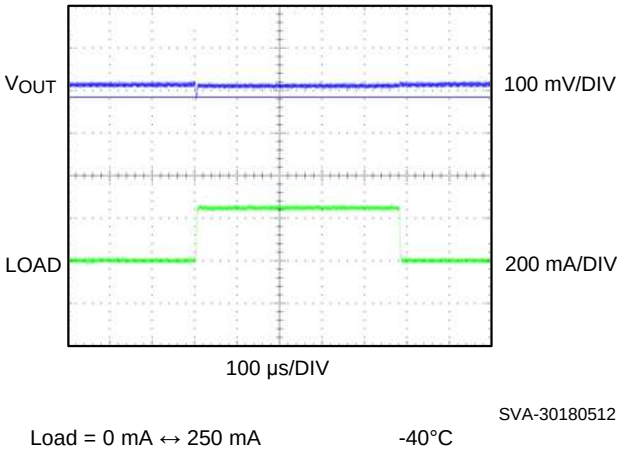
V_{IN} = 3.2 V ↔ 4.2 V Load = 1 mA

Figure 9. Line Transient



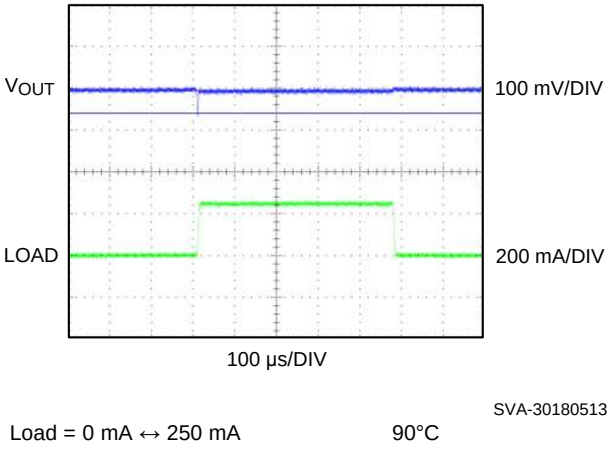
V_{IN} = 3.2 V ↔ 4.2 V Load = 250 mA

Figure 10. Line Transient



Load = 0 mA ↔ 250 mA -40°C

Figure 11. Load Transient



Load = 0 mA ↔ 250 mA 90°C

Figure 12. Load Transient

Typical Characteristics (continued)

Unless otherwise stated: V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C

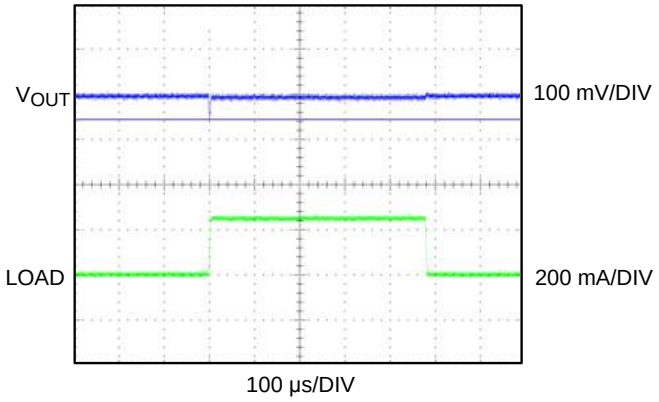


Figure 13. Load Transient

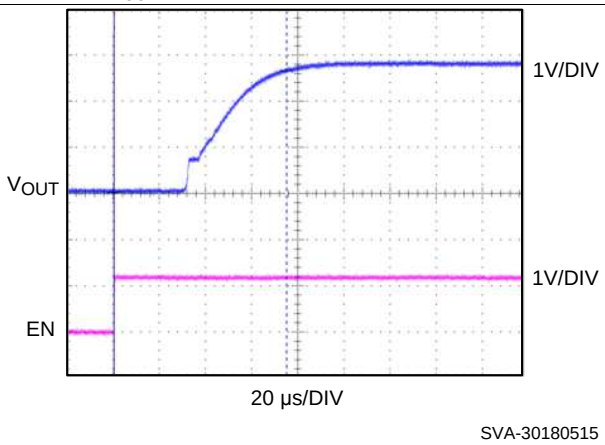


Figure 14. Start-Up

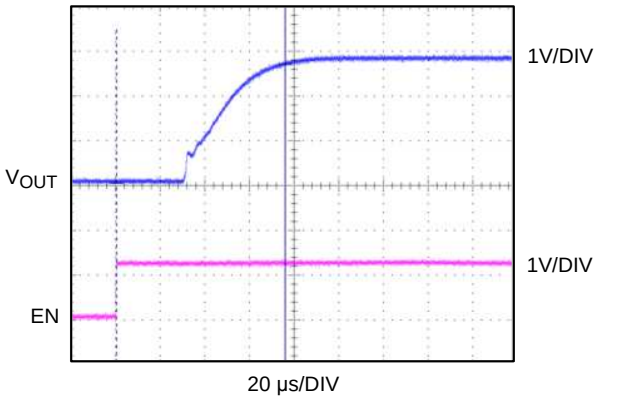


Figure 15. Start-Up

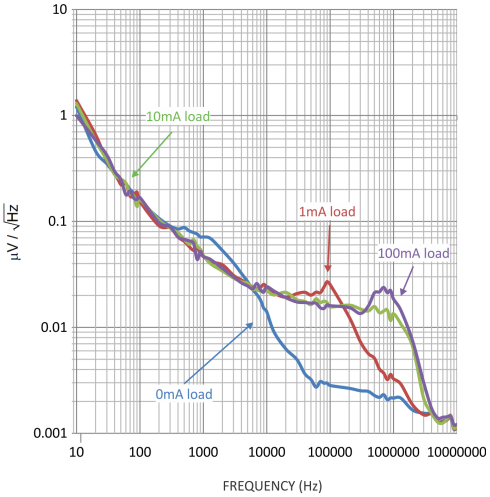


Figure 16. Noise Density Test

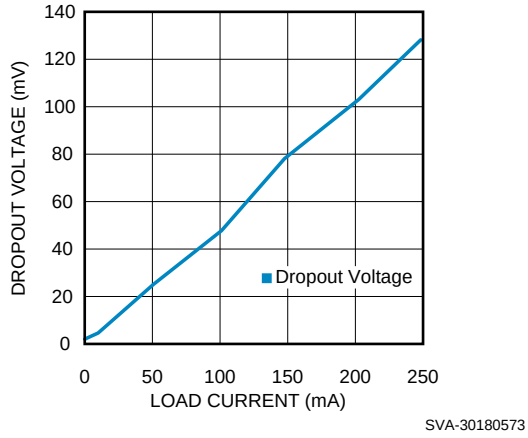


Figure 17. Dropout Voltage vs Load Current

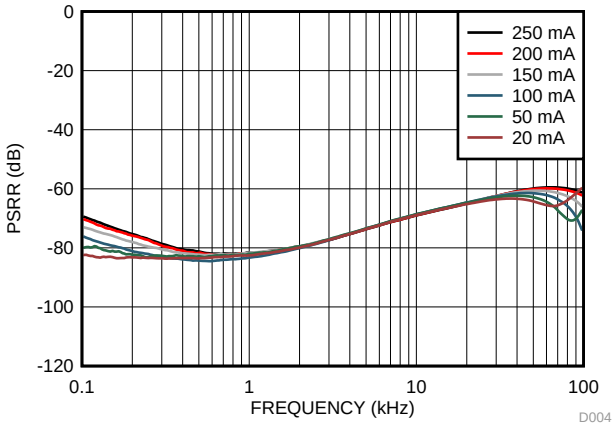


Figure 18. PSRR Loads Averaged 100 Hz To 100 KHz

Typical Characteristics (continued)

Unless otherwise stated: V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C

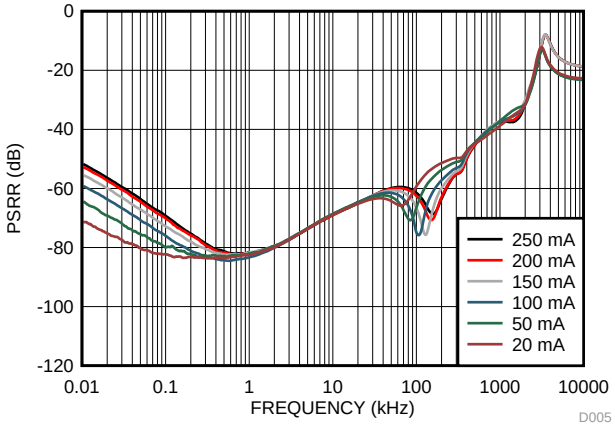


Figure 19. PSRR Loads Averaged 10 Hz To 10 MHz

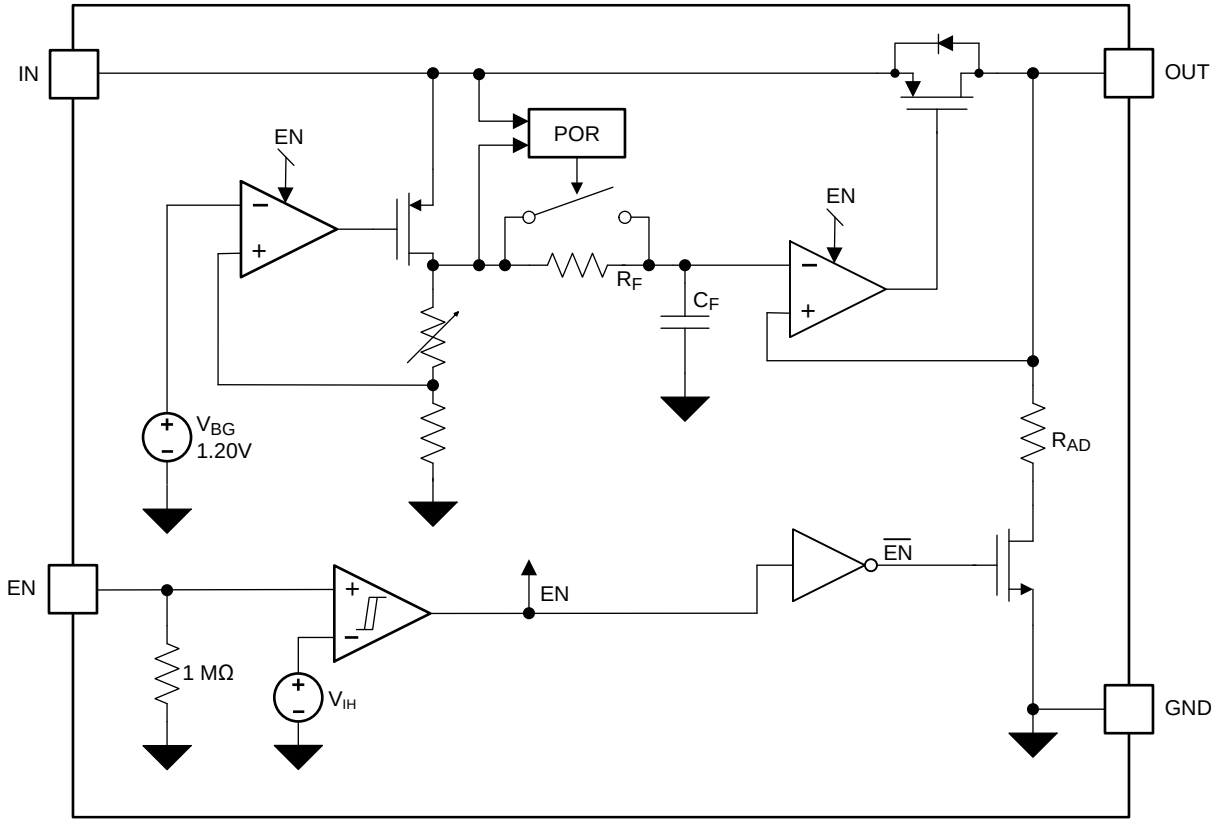
7 Detailed Description

7.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the LP5907 provides low noise, high PSRR, low quiescent current, as well as low line and load transient response figures. Using new innovative design techniques, the LP5907 offers class leading noise performance without the need for a separate noise filter capacitor.

The LP5907 is designed to perform with a single 1-µF input capacitor and a single 1-µF ceramic output capacitor. With a reasonable PCB layout, the single 1-µF ceramic output capacitor can be placed up to 10 cm away from the LP5907 package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The LP5907 EN pin is internally held low by a 1-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

7.3.2 Low Output Noise

Any internal noise at the LP5907 reference voltage is reduced by a first order low-pass RC filter before it is passed to the output buffer stage. The low-pass RC filter has a –3 dB cut-off frequency of approximately 0.1 Hz.

Feature Description (continued)

7.3.3 Output Automatic Discharge

The LP5907 output employs an internal 230-Ω (typical) pull-down resistance to discharge the output when the EN pin is low, and the device is disabled.

7.3.4 Remote Output Capacitor Placement

The LP5907 requires at least a 1-µF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10 cm away from the LDO.

7.3.5 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the LP5907 has been designed to protect against temporary thermal overload conditions. The Thermal Shutdown circuitry was not intended to replace proper heat-sinking. Continuously running the LP5907 device into thermal shutdown may degrade device reliability.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP5907 Enable (EN) pin is internally held low by a 1-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions.

When the EN pin is pulled low, and the output is disabled, the output automatic discharge circuitry is activated. Any charge on the OUT pin is discharged to GND through the internal 230-Ω (typical) pull-down resistance.

7.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5907 does not include any dedicated UVLO circuitry. The LP5907 internal circuitry is not fully functional until V_{IN} is at least 2.2 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2 V or (V_{OUT} + V_{DO}).

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5907 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1 µF. The LP5907 delivers this performance in industry standard packages such as DSBGA, X2SON, and SOT-23 which, for this device, are specified with an operating junction temperature (T_J) of –40°C to 125°C.

8.2 Typical Application

Figure 20 shows the typical application circuit for the LP5907. Input and output capacitances may need to be increased above the 1 µF minimum for some applications.

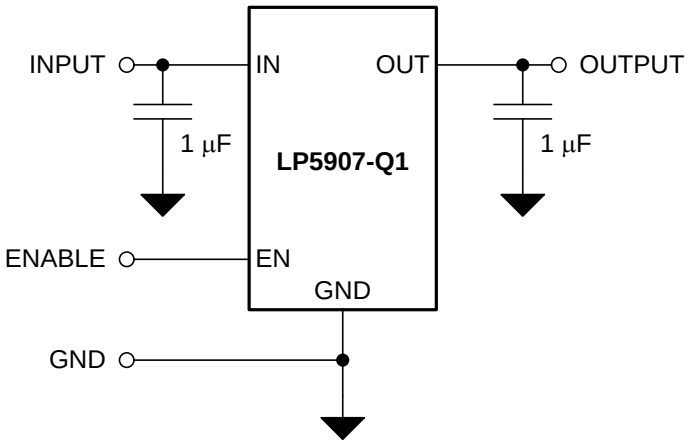


Figure 20. LP5907 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.2 V to 5.5 V
Output voltage	1.8 V
Output current	200 mA
Output capacitor range	0.7 µF to 10 µF
Input/Output capacitor ESR range	5 to 500 mΩ

8.2.2 Detailed Design Procedure

8.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using Equation 1:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

These two equations establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be derated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by Equation 3:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (3)$$

Alternately, if $T_{A\text{-}MAX}$ can not be derated, the P_D value must be reduced. This can be accomplished by reducing V_{IN} in the 'V_{IN}–V_{OUT}' term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

8.2.2.2 External Capacitors

Like most low-dropout regulators, the LP5907 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.3 Input Capacitor

An input capacitor is required for stability. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance. At least a 1 µF capacitor has to be connected between the LP5907 input pin and ground for stable operation over full load current range. Basically, it is ok to have more output capacitance than input, as long as the input is at least 1 µF.

The input capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5907, then it is recommended to increase the input capacitor to at least 10 µF. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be verified by the manufacturer to have a surge current rating sufficient for the application. The initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 µF over the entire operating range.

8.2.2.4 Output Capacitor

The LP5907 is designed specifically to work with a very small ceramic output capacitor, typically 1 µF. A ceramic capacitor (dielectric types X5R or X7R) in the 1 µF to 10 µF range, and with ESR between 5 mΩ to 500 mΩ, is suitable in the LP5907 application circuit. For this device the output capacitor should be connected between the OUT pin and a good connection back to the GND pin.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 mΩ to 500 mΩ for stability. Like the input capacitor, the initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 µF over the entire operating range.

8.2.2.5 Capacitor Characteristics

The LP5907 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 µF to 10 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5907.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 10 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

8.2.2.6 Remote Capacitor Operation

The LP5907 requires at least a 1 µF capacitor at the OUT pin, but there is no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor may be located up to 10 cm away from the LDO. This means that there is no need to have a special capacitor close to the output pin if there is already respective capacitors in the system (like a capacitor at the input of supplied part). The remote capacitor feature helps user to minimize the number of capacitors in the system.

As a good design practice, it is good to keep the wiring parasitic inductance at a minimum, which means to use as wide as possible traces from the LDO output to the capacitors, keeping the LDO output trace layer as close as possible to ground layer and avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. The recommendation is to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, it is recommended to use an input capacitor equal to or larger to the sum of the capacitance at the output node for the best load transient performance.

8.2.2.7 No-Load Stability

The LP5907 remains stable, and in regulation, with no external load.

8.2.2.8 Enable Control

The LP5907 may be switched ON or OFF by a logic input at the EN pin. A voltage on this pin greater than V_{IH} turns the device on, while a voltage less than V_{IL} turns the device off.

When the EN pin is low, the regulator output is off and the device typically consumes less than 1 µA. Additionally, an output pull-down circuit is activated which ensures that any charge stored on C_{OUT} is discharged to ground.

If the application does not require the use of the shutdown feature, the EN pin can be tied directly to the IN pin to keep the regulator output permanently on.

An internal 1-MΩ pull-down resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the *Electrical Characteristics* under V_{IL} and V_{IH}.

8.2.3 Application Curves

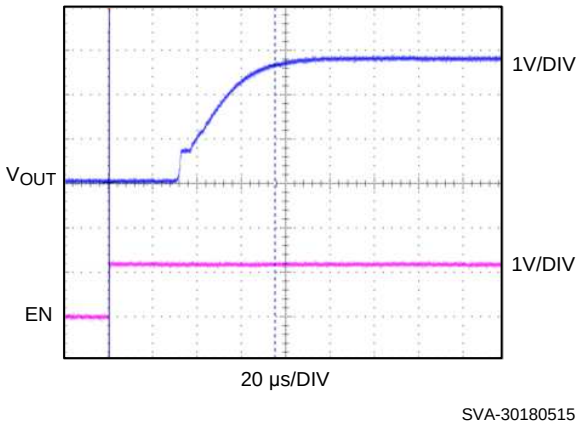


Figure 21. Start-Up

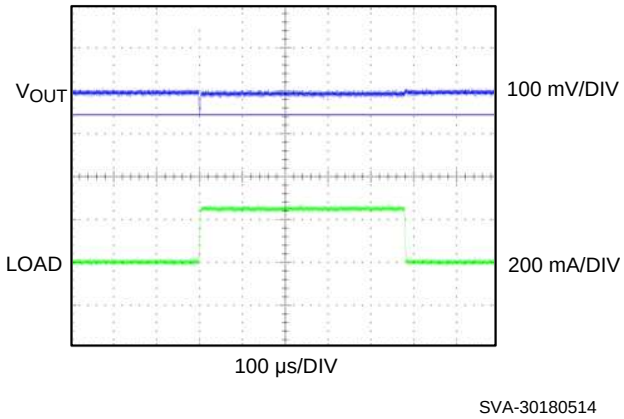


Figure 22. Load Transient Response

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.2 V to 5.5 V. The input supply should be well regulated and free of spurious noise. To ensure that the LP5907 output voltage is well regulated and dynamic performance is optimum, the input supply should be at least V_{OUT} + 1 V. A minimum capacitor value of 1 µF is required to be within 1 cm of the IN pin.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP5907 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5907.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5907, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LP5907 ground pin using as wide, and as short, of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These will add parasitic inductances and resistance that results in inferior performance especially during transient conditions

10.2 Layout Examples

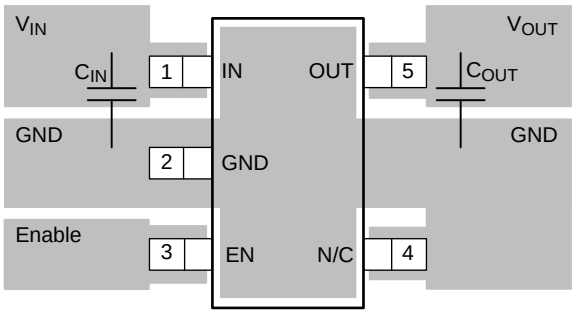


Figure 23. LP5907MF-x.x (SOT-23) Typical Layout

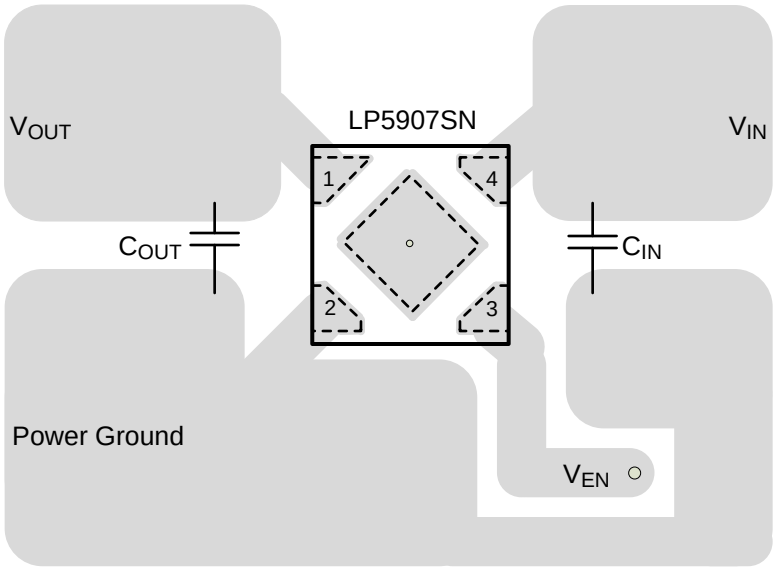


Figure 24. LP5907SN-xx (X2SON) Typical Layout

Layout Examples (continued)

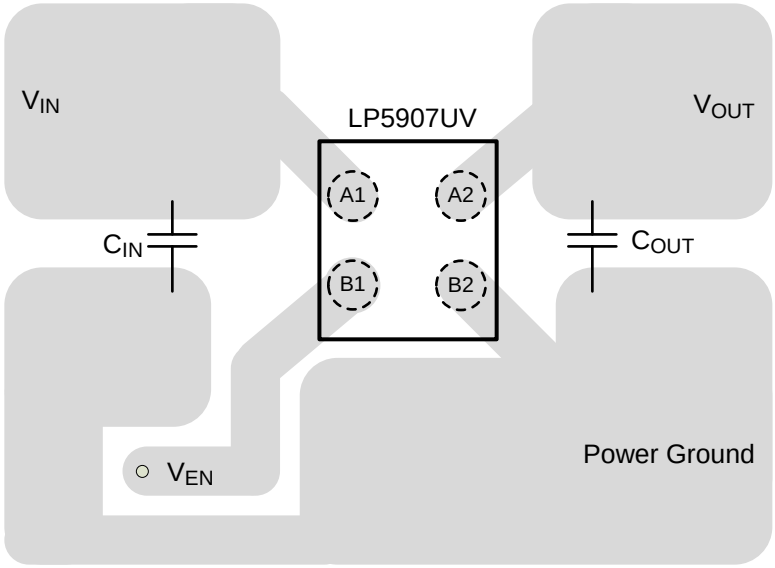


Figure 25. LP5907UV-x.x (DSBGA) Typical Layout

10.3 X2SON Mounting

The X2SON package thermal pad must be soldered to the printed circuit board for proper thermal and mechanical performance. For more information, see the Application Report *QFN/SON PCB Attachment* (SLUA271).

10.4 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in Texas Instruments Application Note AN-1112, *DSBGA Wafer Level Chip Scale Package* (SNVA009). For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

10.5 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device. Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

德州仪器应用手册 AN-1112《*DSBGA 晶圆级芯片规模封装*》（文献编号：SNVA009）。

德州仪器应用手册《*QFN/SON PCB 连接*》（文献编号：SLUA271）

11.2 商标

All trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907A28YKMR	ACTIVE	DSBGA	YKM	4	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 125	Q	Samples
LP5907A33YKMR	ACTIVE	DSBGA	YKM	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	N	Samples
LP5907MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLTB	Samples
LP5907MFX-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN8B	Samples
LP5907MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLUB	Samples
LP5907MFX-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN7B	Samples
LP5907MFX-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLYB	Samples
LP5907MFX-2.85/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN4B	Samples
LP5907MFX-2.9/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	1E5X	Samples
LP5907MFX-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLZB	Samples
LP5907MFX-3.1/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN5B	Samples
LP5907MFX-3.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN6B	Samples
LP5907MFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLVB	Samples
LP5907MFX-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLXB	Samples
LP5907SNX-1.2/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF	Samples
LP5907SNX-1.8/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CG	Samples
LP5907SNX-1.9	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3Z	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907SNX-2.2/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	EP	Samples
LP5907SNX-2.5/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	F9	Samples
LP5907SNX-2.7/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH	Samples
LP5907SNX-2.75	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HI	Samples
LP5907SNX-2.8/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CI	Samples
LP5907SNX-2.85/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ	Samples
LP5907SNX-2.9/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GV	Samples
LP5907SNX-3.0/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK	Samples
LP5907SNX-3.1/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL	Samples
LP5907SNX-3.2/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM	Samples
LP5907SNX-3.3/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CN	Samples
LP5907SNX-4.0/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GU	Samples
LP5907SNX-4.5/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CO	Samples
LP5907UVE-1.2/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R	Samples
LP5907UVE-1.8/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples
LP5907UVE-2.8/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5907UVE-2.85/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V	Samples
LP5907UVE-3.0/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907UVE-3.1/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X	Samples
LP5907UVE-3.2/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
LP5907UVE-3.3/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP5907UVE-4.5/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
LP5907UVX-1.2/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R	Samples
LP5907UVX-1.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples
LP5907UVX-2.5/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E	Samples
LP5907UVX-2.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5907UVX-2.85/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V	Samples
LP5907UVX-3.0/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
LP5907UVX-3.1/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X	Samples
LP5907UVX-3.2/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
LP5907UVX-3.3/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP5907UVX-4.5/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
LP5907UVX19/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
LP5907UVX37/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LP5907 :

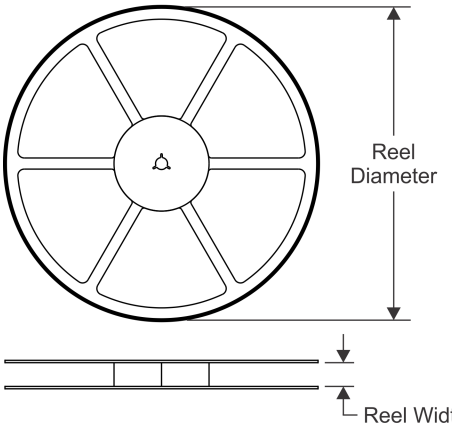
- Automotive: LP5907-Q1

NOTE: Qualified Version Definitions:

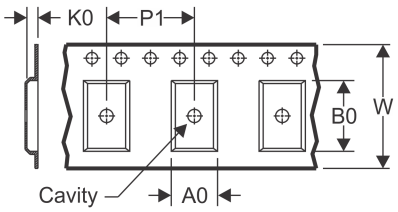
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

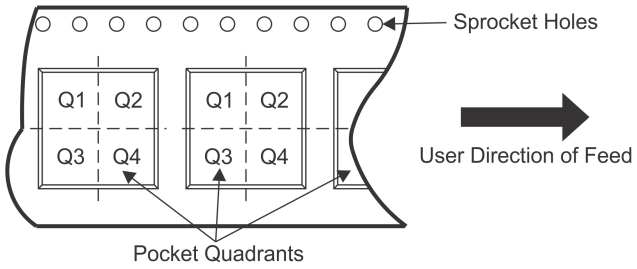


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

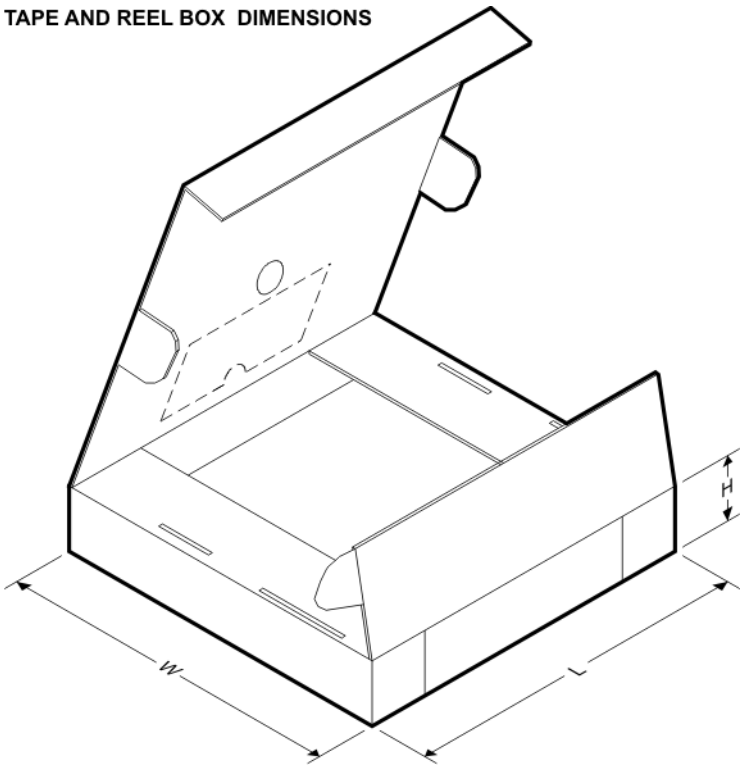


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907A28YKMR	DSBGA	YKM	4	3000	178.0	8.4	0.74	0.74	0.54	4.0	8.0	Q1
LP5907A33YKMR	DSBGA	YKM	4	3000	178.0	8.4	0.74	0.74	0.54	4.0	8.0	Q1
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-1.9	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.75	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.9/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-4.0/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.7	0.7	0.48	4.0	8.0	Q1
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	4.0	8.0	Q1
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	4.0	8.0	Q1
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	4.0	8.0	Q1
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907A28YKMR	DSBGA	YKM	4	3000	220.0	220.0	35.0
LP5907A33YKMR	DSBGA	YKM	4	3000	220.0	220.0	35.0
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-1.9	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0

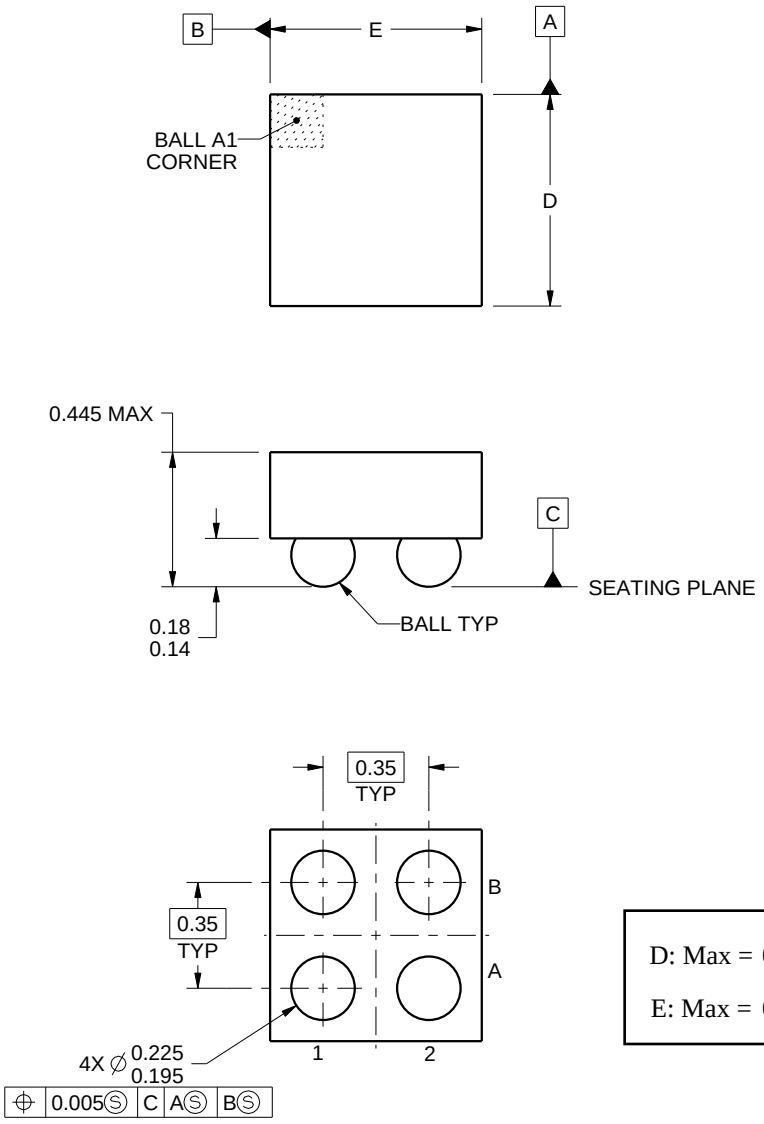
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907SNX-2.75	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.9/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-4.0/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0

PACKAGE OUTLINE

YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.675 mm, Min =0.615 mm

E: Max = 0.675 mm, Min =0.615 mm

4220102/A 11/2014

NOTES:

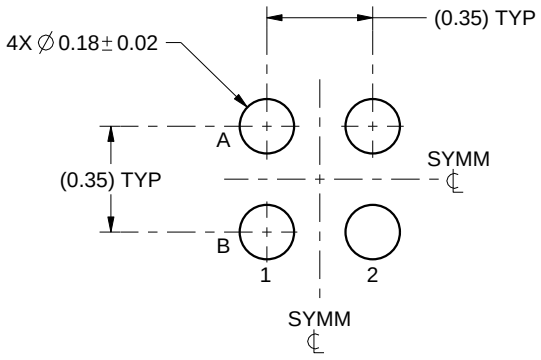
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

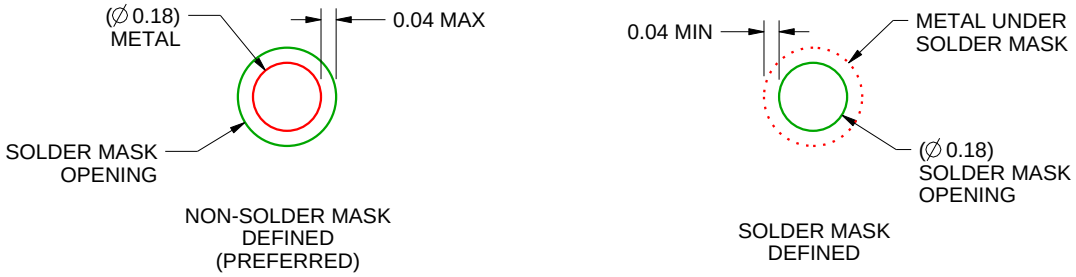
YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4220102/A 11/2014

NOTES: (continued)

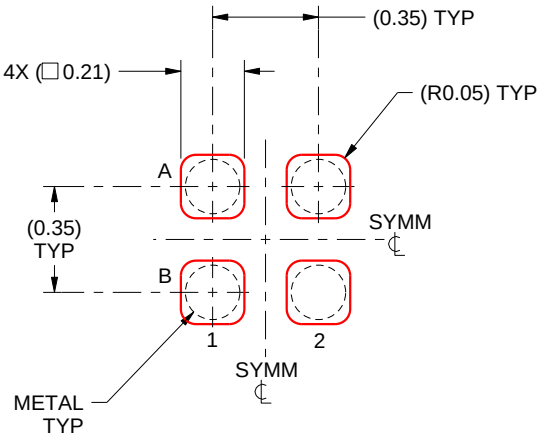
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



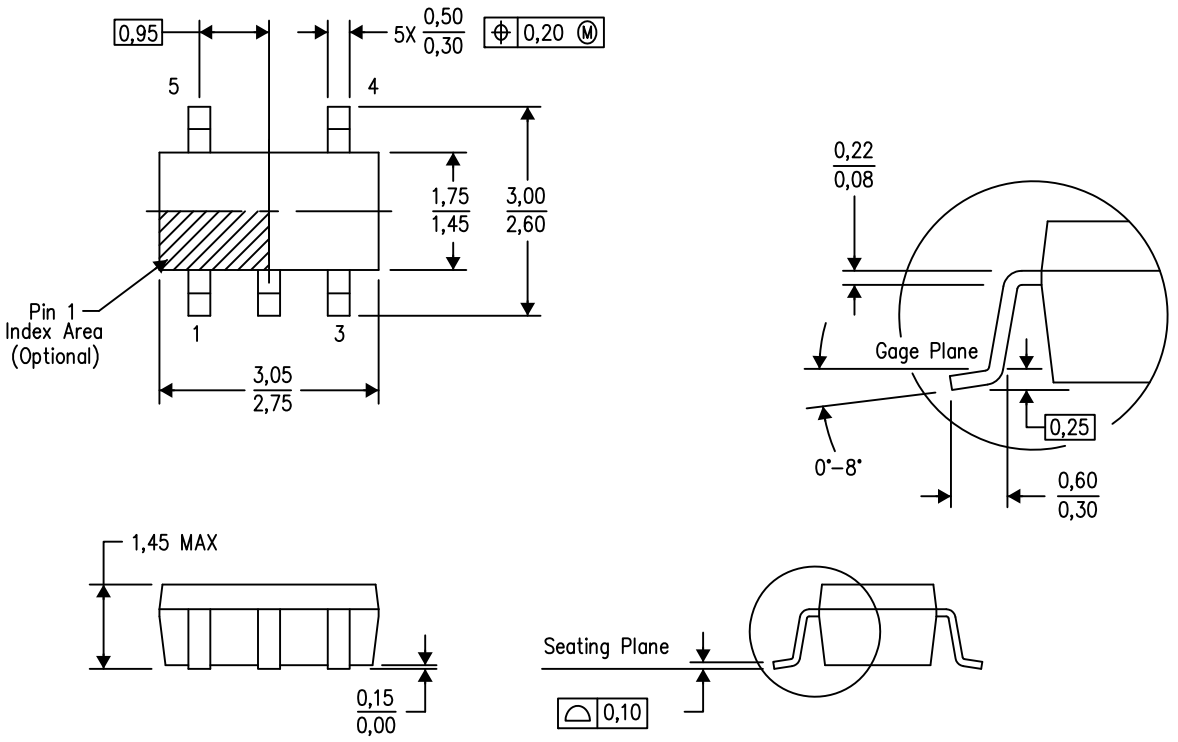
SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL
SCALE:40X

4220102/A 11/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

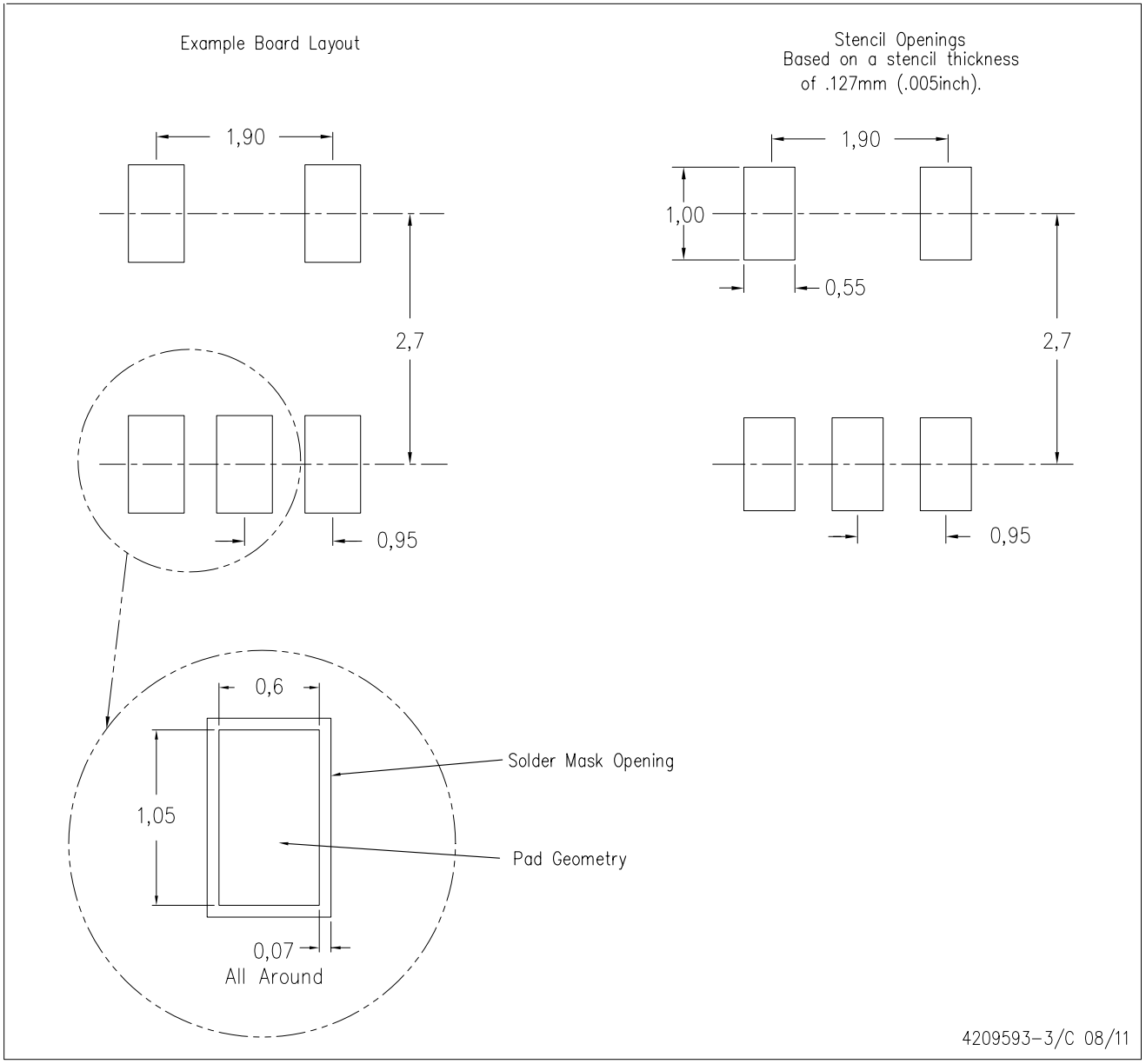
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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