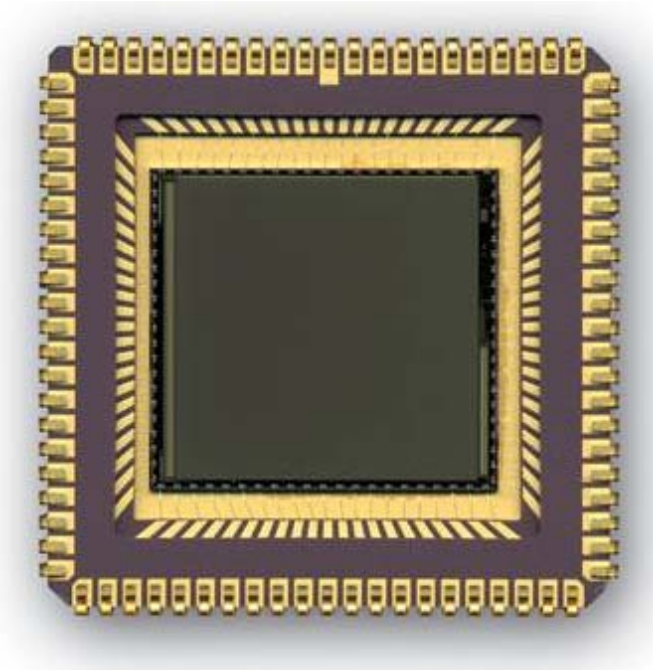
STAR1000 1M Pixel Radiation Hard CMOS Image Sensor

Key Features

The STAR1000 sensor has the following characteristics:

- Integrating 3-transistor Active Pixel Sensor.
- 1024 by 1024 pixels on 15 μm pitch.
- Radiation tolerant design.
- On-chip double sampling circuit to cancel Fixed Pattern Noise.
- Electronic shutter.
- Read out rate: up to 11 full frames per second.
- Region Of Interest (ROI) windowing.
- On-chip 10-bit ADC.
- Programmable gain amplifier.
- Ceramic JLCC-84 package.
- Available with BK7G18 glass and with N_2 filled cavity.



Sensor Description

The STAR1000 is a CMOS image sensor with 1024 by 1024 pixels on a 15 mm pitch. It features on-chip Fixed Pattern Noise (FPN) correction, a programmable gain amplifier, and a 10-bit Analog-to-Digital Converter (ADC).

All circuits are designed using the radiation tolerant design rules for CMOS image sensors, to allow a high tolerance against total dose effects.

Registers that are directly accessed by the external controller contain the X- and Y- addresses of the pixels to be read. This architecture provides flexible operation and allows different operation modes such as (multiple) windowing, subsampling, etc.

Two versions od sensors are available: STAR1000 and STAR1000BK7. The STAR1000 has a quartz glass lid and the cavity between the die and the lid is filled with air. The STAR1000BK7 has a BK7G18 glass lid and the cavity is filled with N_2 which increases the temperature operating range.

Image Sensor Specifications

General Specifications

Table 1. General Specification of the STAR1000 Sensor

Parameter	Specification	Comment
Detector technology	CMOS active pixel sensor	
Pixel structure	3-transistor active pixel	Radiation-tolerant pixel design.
Photodiode	High fill factor photodiode	Using N-well technique.
Sensitive area format	1024 x 1024 pixels	
Pixel size	15 x15 μm^2	
Pixel output rate	12 MHz	Speed can be exchanged for power consumption.
Windowing	X- and Y- addressing random programmable	
Electronic shutter	Electronic rolling shutter. Range: 1:1024	Integration time is variable in time steps equal to the row readout time.
Total dose radiation tolerance	> 250 Krad (Si)	Pixel test structures with a similar design have shown total dose tolerance up to several Mrad. Note: Dark current and DSNU are dependent of radiation dose.
Proton radiation tolerance	$2,4.10^{11}$ proton/cm^2 At 60 MeV	
SEU tolerance	> 127,8 MeV cm^3 mg^{-1}	

Electro-optical Specifications

Table 2. Electro-optical Specifications of the STAR1000 Sensor

Parameter	Value		Comment
	Typical Value	Unit	
Spectral range	400 - 1000	nm	
Quantum efficiency x fill factor	20%		Average over the visual range. See spectral response curve.
Full well capacity	135.000	e-	
Saturation capacity to meet non-linearity within + 5%	99.000	e-	
Output signal swing	1.1	V	
Conversion gain	11.4	μV/e-	
kTC noise	47	e-	
Dynamic range	69	dB	
Fixed pattern noise	Local: 1 σ < 0.30% Global: 1σ <0.56% of full well		
Photo response non-uniformity at Sat/2 (RMS)	Local: 1 σ < 0.67% Global: σ <3.93% of full well		

Table 2. Electro-optical Specifications of the STAR1000 Sensor (continued)

Parameter	Value		Comment
	Typical Value	Unit	
Average dark current at 293K	223	$\rho A/cm^2$	
Dark current signal	3135	e-/s	Dark current rises 425 e-/s per Krad.
DSNU signal	1.055% of Vsat		DSNU rises 14 e-/s per Krad.
Optical cross-talk at 600 nm	Vertical: 16% Horizontal: 17.5%		
Anti-blooming capacity	x 1000		
Output amplifier gain	x1, x2.47, x4.59 and x8.64		Controlled by 2 bits.
Analogue input bandwidth	9.5	MHz	
Analogue input signal range	0.1 to 4.9	V	
Analog-to-Digital converter	10	bit	Radiation-tolerant version of the ADC on Ibis4 and other image sensors.
ADC Differential Non-Linearity (DNL)	<= ±3.5	LSB	
ADC Integral Non-Linearity (INL)	<= ±5.8	LSB	Integral non-linearity of ADC is better than linearity of image sensor.
Supply voltage	5	V	Digital input signals are 3.3V compatible.
Power dissipation	< 350 < 100	mW	With internal ADC powered. Without internal ADC powered. Both values measured at nominal speed (12 MHz).

Spectral Response

Figure 1. Spectral Response Curve

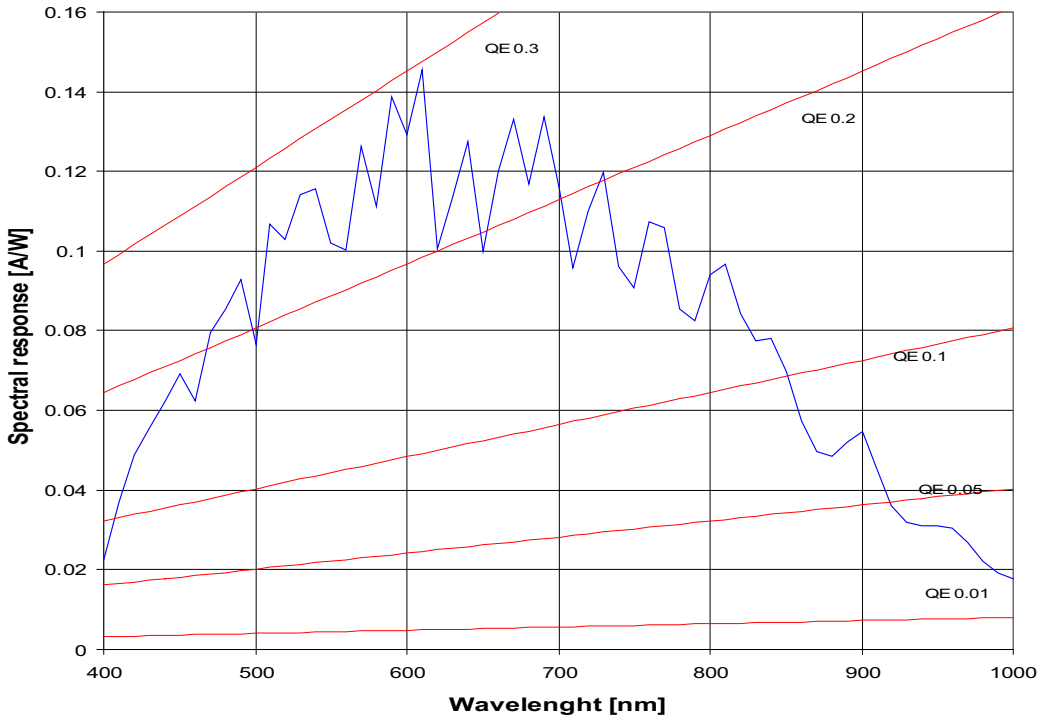
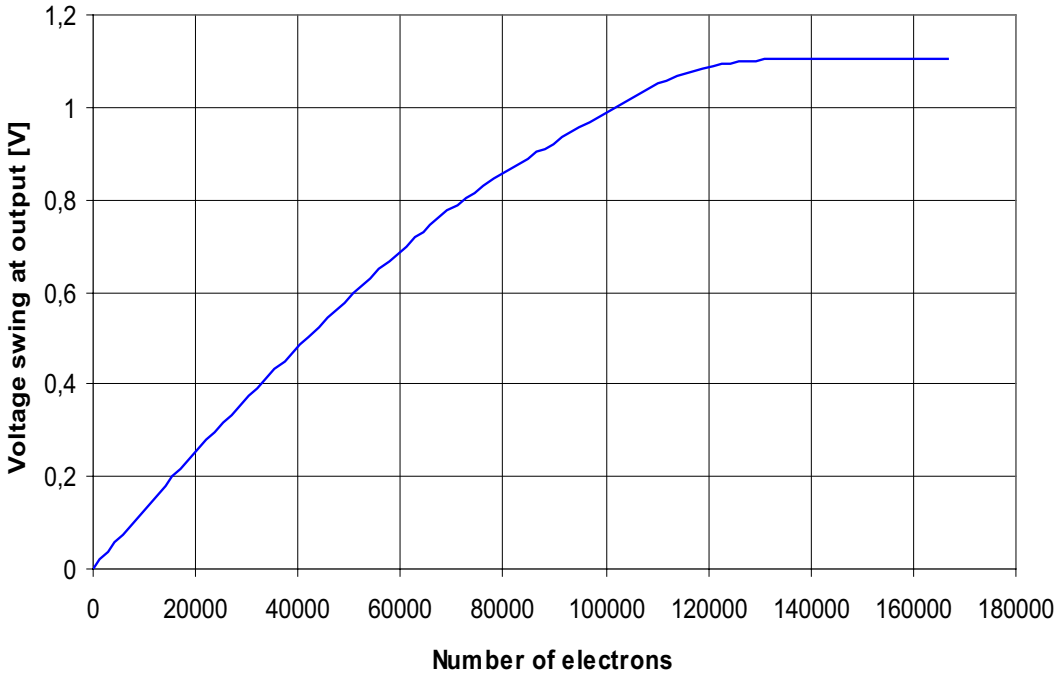


Photo-Voltaic Response

Figure 2. Photo Voltaic Response Curve



Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings STAR1000

Characteristics	Limits		Units	Remarks
	Min	Max		
Any supply voltage	-0.5	+7	V	R
Voltage on any input terminal	-0.5	Vdd + 0.5	V	
Operating temperature	0	+60	°C	Temperature range confirmed by evaluation testing.
Storage temperature	-10	+60	°C	Not longer than 1 hour. Temperature range confirmed by evaluation testing.
Sensor soldering temperature	NA	125	°C	Hand soldering only. The sensor's temperature may not rise above this limit. Please read the soldering and handling section for more information.

Table 4. Absolute Maximum Ratings STAR1000BK7

Characteristics	Limits		Units	Remarks
	Min	Max		
Any supply voltage	-0.5	+7	V	
Voltage on any input terminal	-0.5	Vdd + 0.5	V	
Operating temperature	-40	+85	°C	Temperature range confirmed by evaluation testing.
Storage temperature	-40	+85	°C	Temperature range confirmed by evaluation testing.
	-40	+120		Maximum 1 hour.
Sensor soldering temperature	NA	125	°C	Hand soldering only. The sensor's temperature may not rise above this limit. Please read the soldering and handling section for more information.

DC Operating Conditions

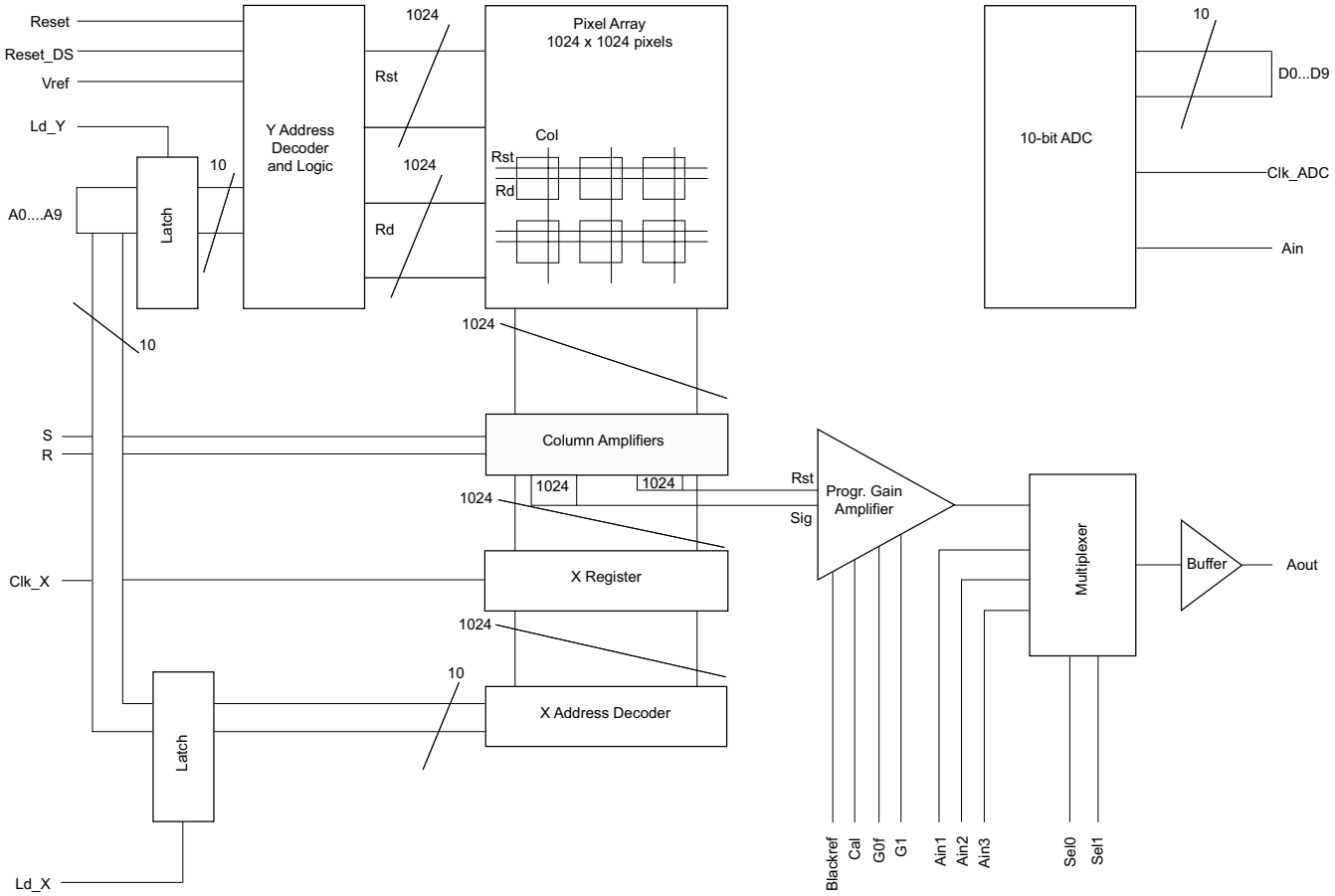
Table 5. DC Operating Conditions

Symbol	Parameter	Limits			Units
		Min	Typ	Max	
VDDA	Analog supply of the image core.		5		V
VDDD	Digital supply of the image core.		5		V
VDD_ADC_ANA	Analog supply of the ADC circuitry.		5		V
VDD_ADC_DIG	Digital supply of the ADC circuitry.		5		V
VDD_DIG_OUT	Power supply of ADC digital output stage.		5		V
VRES	Reset level for RESET signal.		5		V
VREF	Reset level for RESET_DS signal.	4		5	V
GNDA	Analog ground of the image core.		0		V
GNDD	Digital ground of the image core.		0		V
GND_ADC_ANA	Analog ground of the ADC circuitry.		0		V
GND_ADC_DIG	Digital ground of the ADC circuitry.		0		V
V_{IH}	Logical '1' input voltage.	1.8		VDDD	V
V_{IL}	Logical '0' input voltage.	0		1	V
V_{OH}	Logical '1' output voltage.	4.25		VDDD	V
V_{OL}	Logical '0' output voltage.			1	V

Architecture

Floor Plan

Figure 3. Star1000 Floor Plan



The image sensor contains five sections: the pixel array, the X- and Y- addressing logic, the column amplifiers, the output amplifier and the ADC. Figure 3. shows an outline diagram of the sensor, including an indication of the main control signals. The following paragraphs explain in more detail the function and operation of the different imager parts.

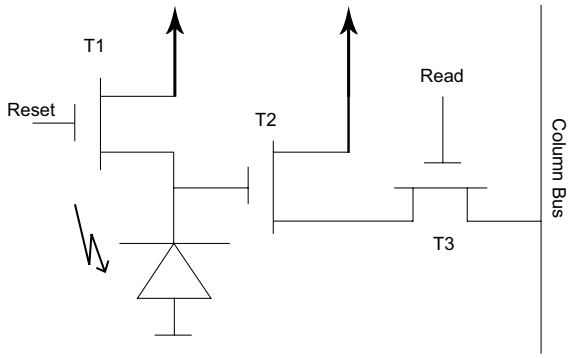
Pixel Array

The pixel array contains 1024 by 1024 active pixels at 15 μm pitch. Each pixel contains one photo diode and three transistors (Figure 4.).

The photo diode is always in reverse bias. At the beginning of the integration cycle, a pulse is applied to the reset line (gate of T1) bringing the cathode of D1 to the reset voltage level. During the integration period, photon-generated electrons accumulate on the diode capacitance reducing the voltage on the gate of T2. The real illumination dependent signal is the difference between the reset level and the output level after integration. This difference is created in the column amplifiers. T2 acts as a source follower and T3 allows connection of the pixel signal (reset level and output level) to the vertical output bus.

The reset lines and the read lines of the pixels in a row are connected together to the Y- decoder logic; the outputs of the pixels in a column are connected together to a column amplifier.

Figure 4. Architecture of the 3T Pixel



Addressing Logic

The addressing logic allows direct addressing of rows and columns. Instead of the one-hot shift registers that are often used, address decoders are implemented. One can select a line by presenting the required address to the address input of the device and latching it to the Y- decoder logic. Presenting the X- address to the device address input and latching it to the X- address decoder can select a column.

A typical line read out sequence will first select a line by applying the Y-address to the Y-decoder. Activation of the LD_Y input on the Y-logic connects the pixel outputs of the selected line to the column amplifiers. The individual column amplifier outputs are connected to the output amplifier by applying the respective X- addresses to the X- address decoder. Applying the appropriate Y- address to the Y-decoder and activating the “Reset” input reset a line. The integration time of a row is the time between the last reset of this row and the time when it is selected for read out.

The Y- decoder logic has two different reset inputs: RESET and RESET_DS. Activation of RESET resets the pixel to the Vdd level; activation of RESET_DS resets the pixel to the voltage level on the VREF input. This feature allows the application of the so called dual slope integration. If dual slope integration is not needed, VREF is tied to Vdd and RESET_DS must never be activated.

Column Amplifiers

All outputs from the pixels in a column are connected in parallel to a column amplifier. This amplifier samples the output voltage and the reset level of the pixel whose row is selected at that moment and presents these voltage levels to the output amplifier. As a result, the pixels are always reset immediately after read out as part of the sample procedure. Note that the maximum integration time of a pixel is the time between two read cycles.

Output Amplifier and Analog Multiplexer

The output amplifier combines subtraction of pixel signal level from reset level with a programmable gain amplifier. Since the amplifier is AC coupled, it also contains a provision to maintain and restore the proper DC level.

An analog signal multiplexing feeds the pixel signal to the final unity gain buffer, providing the required drive capability. Apart from the pixel signal, three other external analog signals can be fed to the output buffer. All these signals can be digitalised by the on-chip ADC if the output of this buffer is externally connected to the input of the ADC.

The purpose of the additional analog inputs (A_IN1, A_IN2, and A_IN3) is to allow the possibility of processing other analog signals through the image sensors signal path. These signals can then be converted by the ADC and processed by the image controller FPGA. The additional analog inputs are intended for low frequency or DC signals and have a reduced bandwidth compared with the image signal path.

ADC

The image sensor has a 10-bit ADC that is electrically separated from the rest of the image sensor circuits and can be powered down if an external ADC is used. The conversion takes place at the falling edge of the clock and the output pins can be disabled to allow operation of the device in a bus structure.

Timing and Control Signals

The pixels addressing is done by direct addressing of rows and columns. This approach has the advantage of full flexibility when accessing the pixel array: multiple windowing and subsampled read out are possible by proper programming.

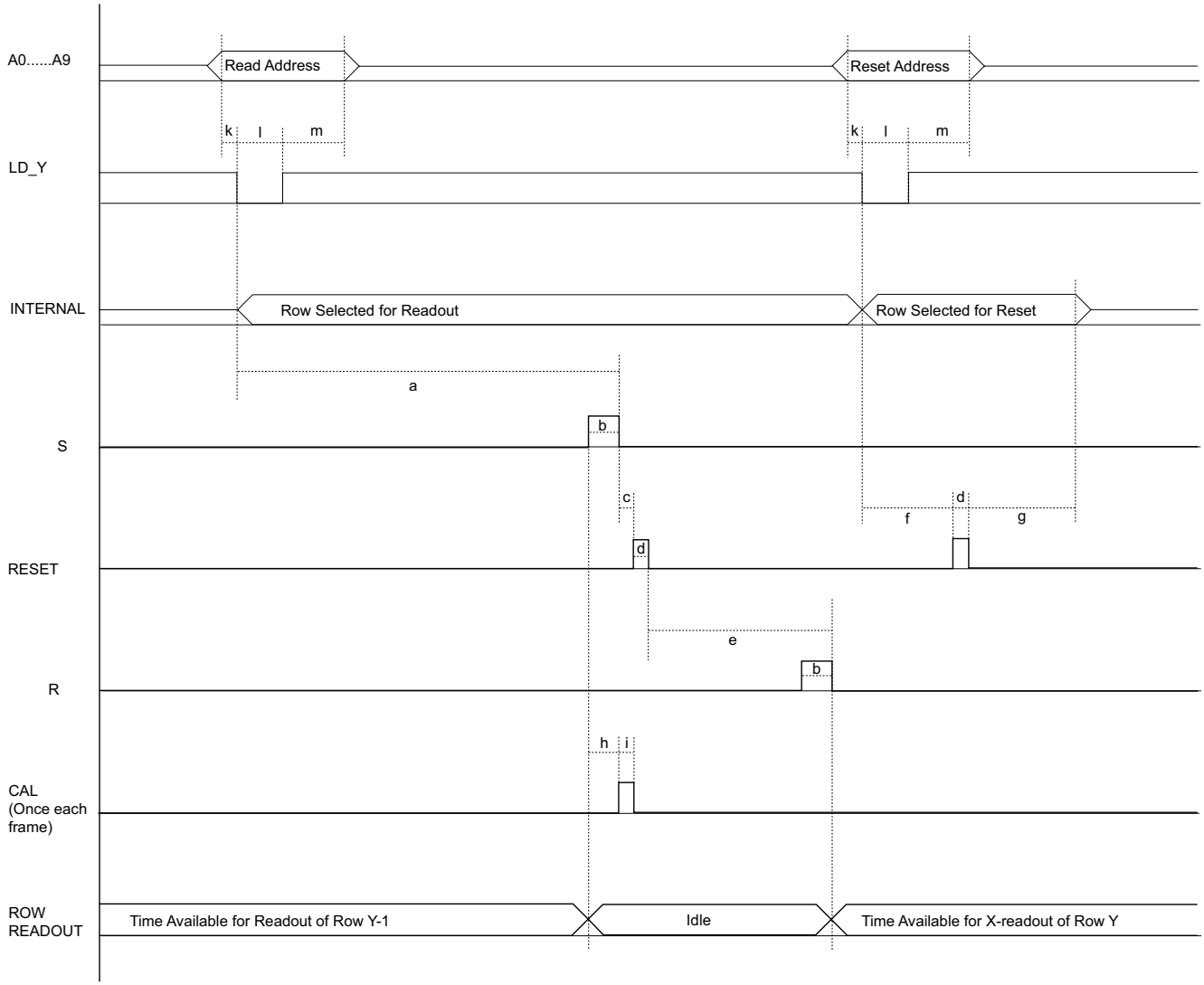
The following paragraphs clarify the timing for row and column readout.

Row Selection and Reset Timing

Figure 5. shows the timing of the line sequence control signals. The timing constraints are presented in Table 6.

The address, presented at the address IO pins (A0…A9) is latched in with the LD-Y pulse (active low). After latching; the external controller already produces a new address.

Figure 5. Line Selection and Reset Sequence



Latching in a Y- address selects the addressed row and connects the pixel outputs of that row to the column amplifiers. Through the sequence of the S and R pulse and the reset pulse in between the pixel output signal and reset level are sampled and produced at the output of the column amplifier (to do the FPN double sampling correction).

At this time horizontal read out of the selected row is started and another row is reset to effectuate reduced integration time (electronic rolling shutter).

Table 6. Timing Constraints of Line Sequence

Symbol	Min	Typ	Description
a	3.6 µs		Delay between selection of a new row and falling edge on S. Minimal value: For maximum, speed a new row can already be selected during X- read out of the previous row.
b	0.4 µs		Duration of S and R pulse.
c	0	100 ns	Delay between falling edge of S and rising edge of reset.
d	200 ns		Minimum duration of reset pulse.
e	1.6 µs		Delay between falling edge of reset and falling edge of R.
f	0	100 ns	Minimum delay between falling edge on LD_Y and rising edge of reset.
g		g	Minimum required extension of Y- address after falling edge of reset pulse.
h	100 ns	200 ns	Position of cal pulse after rising edge of S. The cal pulse must only be given once per frame.
i	100 ns	1 µs	Duration of cal pulse.
k	10 ns		Address set up time.
l	20 ns		Load register value.
m	10 ns		Address stable after load.

Pixel Read Out Timing

Figure 6. shows the timing of the pixel readout sequence. The external digital controller presents a column address that is latched by the rising edge of the LD_X pulse. After decoding the X- address the column selection is clocked in the X-register by CLK-X. The output amplifier uses the same pulse to subtract the pixel output level from the pixel reset level and the signal level. This causes a pipeline effect such that the analog output of the first pixel is effectively present at the device output terminal at the third rising edge of the X-CLK signal.

The ADC conversion starts at the falling edge of the CLK-ADC signal and produces a valid digital output 20 ns after this edge. The timing constraints are given in Table 7.

Important note: The values of the X shift-register tend to leak away after a while. Therefore it is very important to keep the CLK_X signal asserted for as long as the sensor is powered up. If the sensor sits idle and CLK_X is not asserted, the leakage of the X shift-register will cause multiple columns to be selected at once. This forces high current through the sensor and may cause damage.

Figure 6. Column Selection and Read Out Sequence

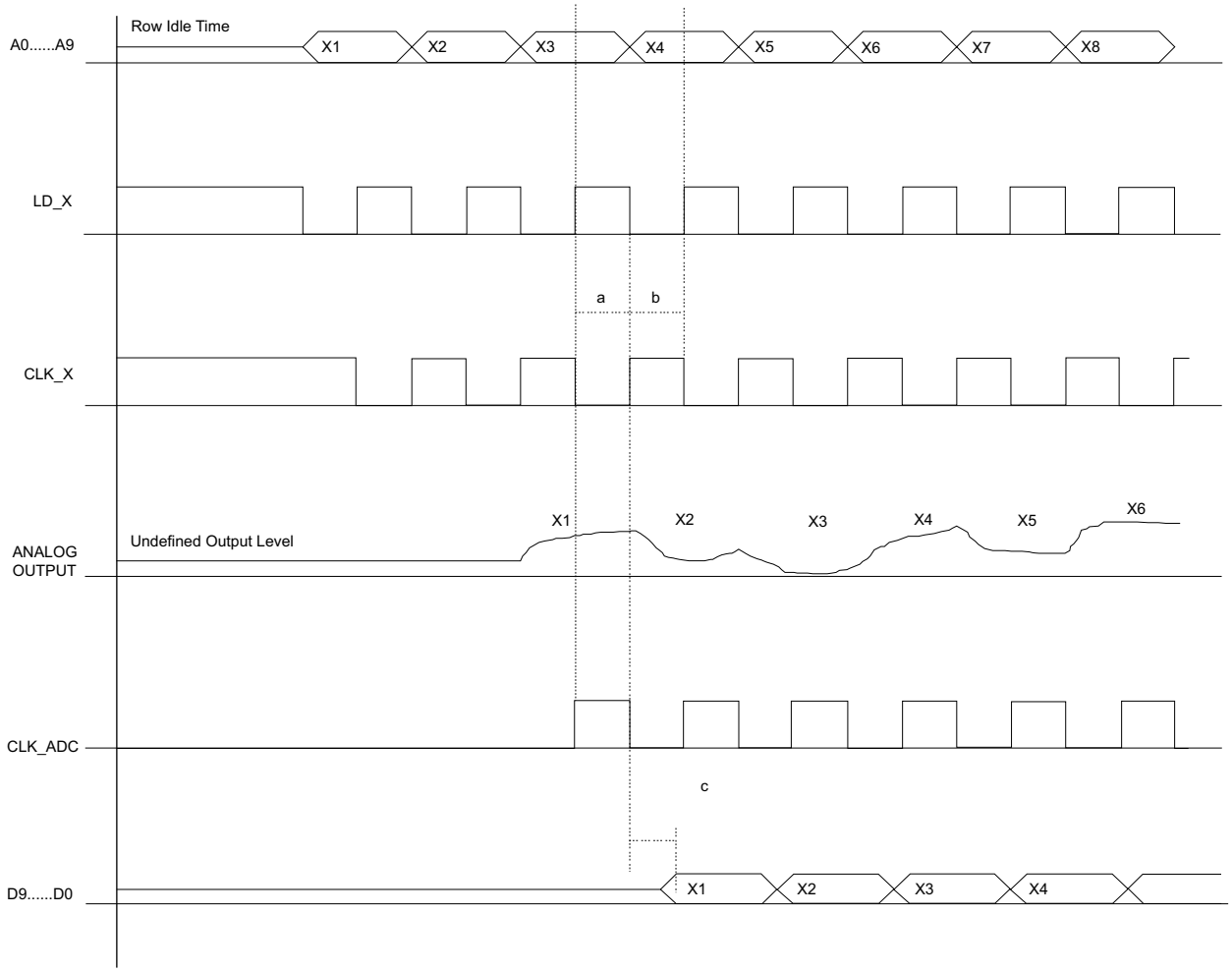


Table 7. Timing Constraints of Column Read Out

Symbol	Min	Typ	Description
a	20 ns		Address setup time.
b	40 ns		Address valid time.
c	0	20 ns	ADC output valid after falling edge of CLK_ADC.

Pin List

Figure 7. displays the pin connections of the STAR1000. The tables that follow group the connections by their functionality.

Figure 7. STAR1000 Pin Connections

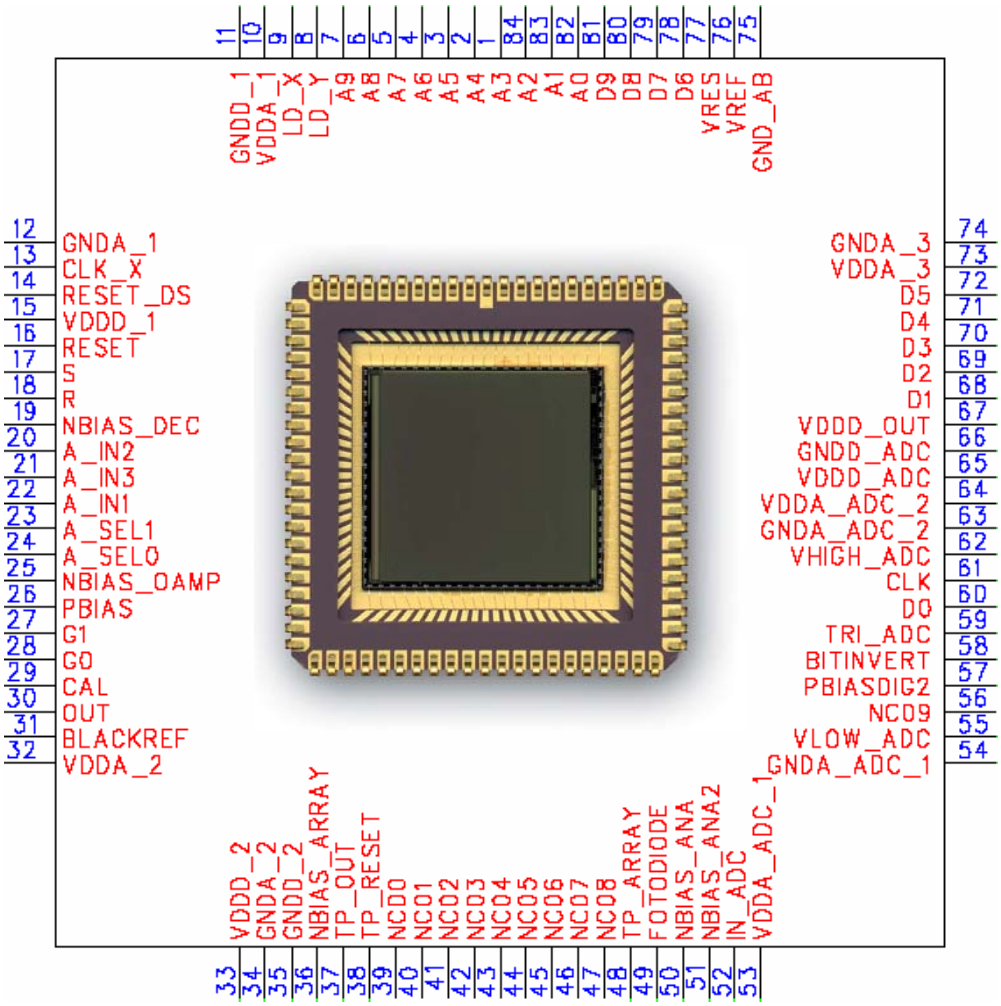


Table 8. Pin List of the STAR1000 Sensor

Pin	Pin Name	Pin Type	Pin Description
1	A3	Input	Digital input.Address inputs for row and column addressing. A9=LSB, A0=MSB.
2	A4	Input	
3	A5	Input	
4	A6	Input	
5	A7	Input	
6	A8	Input	
7	A9	Input	
8	LD_Y	Input	Digital Input. Latch address (A0…A9) to Y-register (0 = track, 1 = hold).

Table 8. Pin List of the STAR1000 Sensor (continued)

Pin	Pin Name	Pin Type	Pin Description
9	LD_X	Input	Digital input. Latch address (A0…A9) to X-register (0 = track, 1 = hold).
10	VDDA	Supply	Analog power supply of the imager (typical 5V).
11	GNDD	Ground	Digital ground of the imager.
12	GNDA	Ground	Analog ground of the imager.
13	CLK_X	Input	Digital input. Clock X-register (output valid & stable when CLK_X is high).
14	RESET_DS	Input	Digital input (high active). Resets row indicated by Y-address (see sensor timing diagram). RESET_DS is used for dual-slope integration (see FAQ). GND is used for normal operation.
15	VDDD	Supply	Digital supply of the image sensor.
16	RESET	Input	Digital input (high active). Resets row indicated by Y-address (see sensor timing diagram).
17	S	Input	Digital input (high active). Control signal for column amplifier (see sensor timing diagram).
18	R	Input	Digital input (high active). Control signal for column amplifier (see sensor timing diagram).
19	NBIAS_DEC	Input	Analog input. Biasing of address decoder. Connect with 100 kΩ to VDDA and decouple with 100 to GND.
20	A_IN2	Input	Additional analog inputs. For proper conversion with on-chip ADC, the input signal must lie within the output signal range of the image sensor (approximately +2V to +4V).
21	A_IN3	Input	
22	A_IN1	Input	
23	A_SEL1	Input	Selection of analog channel: '00' selects image sensor ('01' selects A_IN1, '10' A_IN2, and '11' A_IN3).
24	A_SEL0	Input	
25	NBIAS_OAMP	Input	Analog input. Bias of output amplifier (speed/power control). Connect with 100 kΩ to VDDA and decouple with 100 nF to GND for 12.5 MHz output rate (lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation).
26	PBIAS	Input	Analog input. Biasing of the multiplexer circuitry. Connect with 20 kω to GND and decouple with 100 nF to VDD.
27	G1	Input	Digital input. Select output amplifier gain value: G0 = LSB, G1 = MSB ('00' = unity gain, '01' = x2, '10'= x4, '11'=x8).
28	G0	Input	
29	CAL	Input	Digital input (active high). Initialization of output amplifier. Output amplifier outputs BLACKREF in unity gain mode when CAL is high (1). Apply pulse pattern (see sensor timing diagram).
30	OUT	Output	Analog Output Video Signal. Connected to the analog input of the internal (pin 52) 10-bit ADC or an external ADC.
31	BLACKREF	Input	Analog input. Control voltage for output signal offset level. Buffered on-chip, the reference level can be generated by a 100 kω resistive divider. Connect to 2V DC for use with on-chip ADC.
32	VDDA	Supply	Analog power supply of image core (typical 5V).
33	VDDD	Supply	Digital power supply of image core (typical 5V).

Table 8. Pin List of the STAR1000 Sensor (continued)

Pin	Pin Name	Pin Type	Pin Description
34	GNDA	Ground	Analog ground of image core.
35	GNDD	Ground	Digital ground of image core.
36	NBIAS_ARRAY	Input	Analog input. Biasing of the pixel array. Connect with 1MΩ to VDDA and decouple with 100 nF capacitor to GND.
37	TESTPIX_OUT	Output	Output of single test pixel. Is used for electro-optical evaluation.
38	TESTPIX_RESET	Input	Digital input (active high). Reset signal of single test pixel. Used to reset the single test pixel during electro-optical evaluation.
39	n.c.		
40	n.c.		
41	n.c.		
42	n.c.		
43	n.c.		
44	n.c.		
45	n.c.		
46	n.c.		
47	n.c.		
48	TESTPIXARRAY	Output	Analog output of an array of 20 x 35 test pixels where all photodiodes are connected in parallel. Is used for electro-optical evaluation.
49	PHOTODIODE	Output	Plain Photo Diode (without circuitry). Area of the photodiode = 20 x 35 pixels. Is used for electro-optical evaluation.
50	NBIAS_ANA	Input	Analog input. Analog biasing of the ADC circuitry. Connect with 100 kΩ to VDDA and decouple with 100 nF to GND.
51	NBIAS_ANA2	Input	
52	IN_ADC	Input	Analog input of the internal ADC. Connect to analog output of image sensor (pin 30). Input range (typically 2V and 4V) of the internal ADC is set between by VLOW_ADC (pin 55) and VHIGH_ADC (pin 62).
53	VDD_ADC_ANA	Supply	Analog power supply of the ADC (typical 5V).
54	GND_ADC_ANA	Ground	Analog ground of the ADC.
55	VLOW_ADC	Input	Low reference voltage of internal ADC. Nominal input range of the ADC is between 2V and 4V. The resistance between VLOW_ADC and VHIGH_ADC is approximately 1.5 kΩ. Connect with 1k 5Ω to GND and decouple with 100 nF to GND.
56	n.c.		
57	PBIASDIG2	Input	Connect with 20K to GND and decouple with 100 nF to VDDA.
58	BITINVERT	Input	Digital input. Inversion of the ADC output bits. 0 = invert output bits (0 => black, 1023; white, 0), 1 = no inversion of output bits (black, 0; white, 1023).
59	TRI_ADC	Input	Digital input. Tri-state control of digital ADC outputs (1 = tri-state, 0 = normal mode).
60	D0	Input	ADC output bits.#D0 = LSB, D9=MSB.
61	CLK	Input	Digital input. ADC clock. ADC converts on falling edge.

Table 8. Pin List of the STAR1000 Sensor (continued)

Pin	Pin Name	Pin Type	Pin Description
62	VHIGH_ADC	Input	High reference voltage of internal ADC. Nominal input range of the ADC is between 2V and 4V. The resistance between VLOW_ADC and VHIGH_ADC is about 1.5 kΩ. Connect with 1k 1 Ω to VDDA and decouple with 100 nF to GND.
63	GND_ADC_ANA	Ground	Analog ground of the ADC circuitry.
64	VDD_ADC_ANA	Supply	Analog supply of the ADC circuitry (typical 5V).
65	VDD_ADC_DIG	Supply	Digital supply of the ADC circuitry (typical 5V).
66	GND_ADC_DIG	Output	Digital ground of the ADC circuitry.
67	VDD_DIG_OUT	Supply	Power supply of ADC digital output. Connect to 5V for normal operation. Can be brought to lower voltage when image sensor must be interfaced to low voltage periphery.
68	D1	Output	ADC output bits. #D0 = LSB, D9=MSB.
69	D2	Output	
70	D3	Output	
71	D4	Output	
72	D5	Output	
73	VDDA	Supply	Analog supply of the image core (typical 5V).
74	GNDA	Ground	Analog ground of the image core (typical 5V).
75	GND_AB	Supply	Anti-blooming drain control voltage. Default: connect to ground where the anti-blooming is operational but not maximal. Apply 1V DC for improved anti-blooming.
76	VREF	Supply	Analog supply. Reset level for RESET_DS. Is used for extended optical dynamic range. See FAQ for more details.
77	VRES	Supply	Analog supply. Reset level for RESET (typical 5V).
78	D6	Output	ADC output bits.#D0 = LSB, D9=MSB.
79	D7	Output	
80	D8	Output	
81	D9	Output	
82	A0	Input	Digital input. Address inputs for row and column addressing. A9=LSB, A0=MSB.
83	A1	Input	
84	A2	Input	

Notes
1. All pins with the same name can be connected together.
2. Unused inputs must always be tied to an appropriate level, e.g., VDD or GND.
3. Note on power up behavior: At power on, the image sensor is in an undefined state. It is advised that after start up an address is latched as soon as possible into the Y- decoder and the X- decoder to prevent high current consumption.
4. There is no on-chip power supply rejection. This means that every noise signal on the analog supply voltages is copied directly to the analog video signal (decoupling of the supply voltages as close as possible to the image sensor is recommended).

Packaging and Geometrical Constraints

Package Drawing

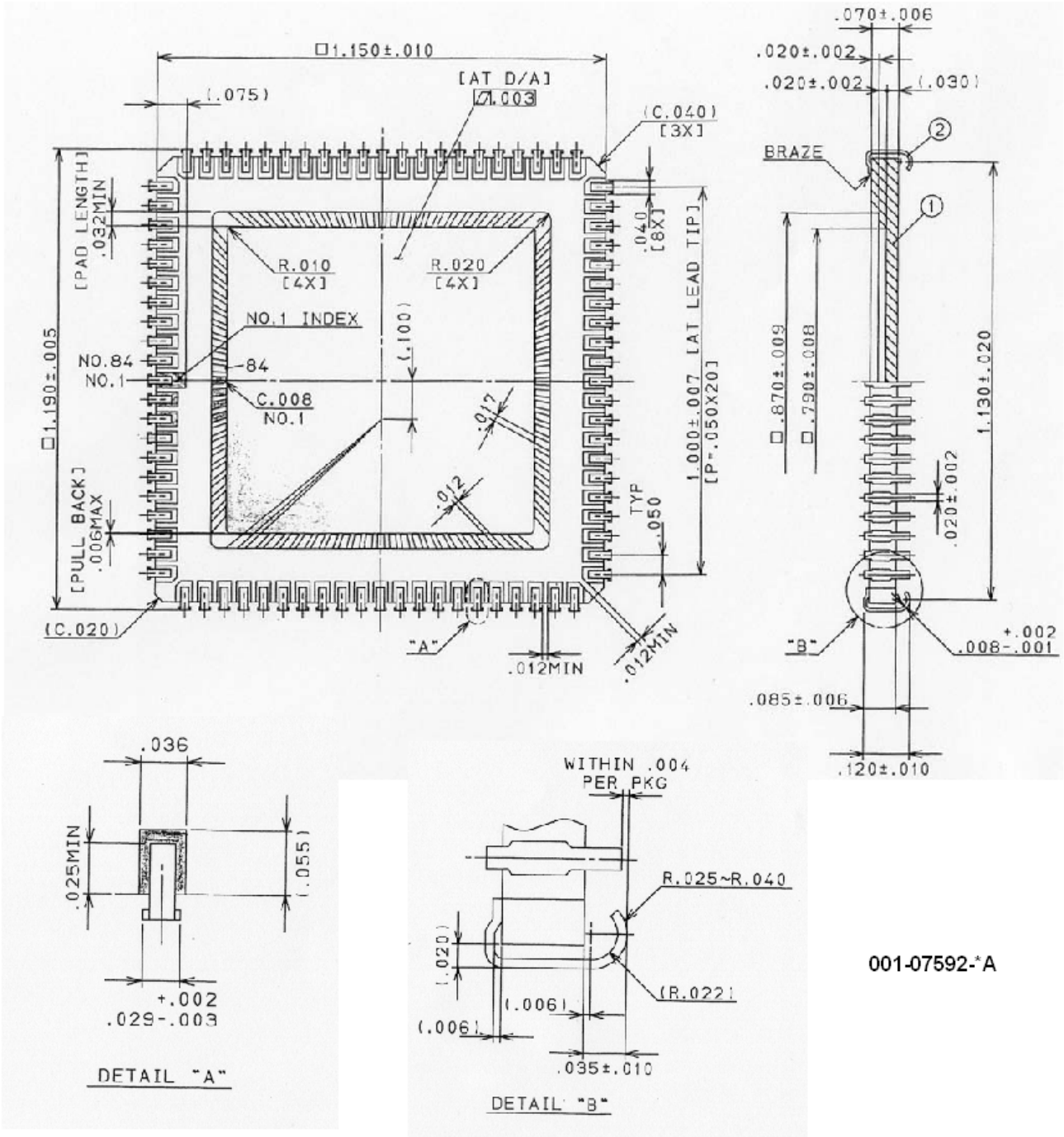
The detector is packaged in an 84-pin J-leaded package.

The detector is mounted into position with thermally and electrically conductive adhesive. The bottom plate of the cavity is electrically connected to a ground pin.

The detector is positioned into the cavity such that the optical center of the detector coincides with the geometrical center of the cavity within a tolerance of ± 50 μm in X- and Y direction. The tolerance on the parallelism of the detector is ± 50 μm in X- and Y- direction.

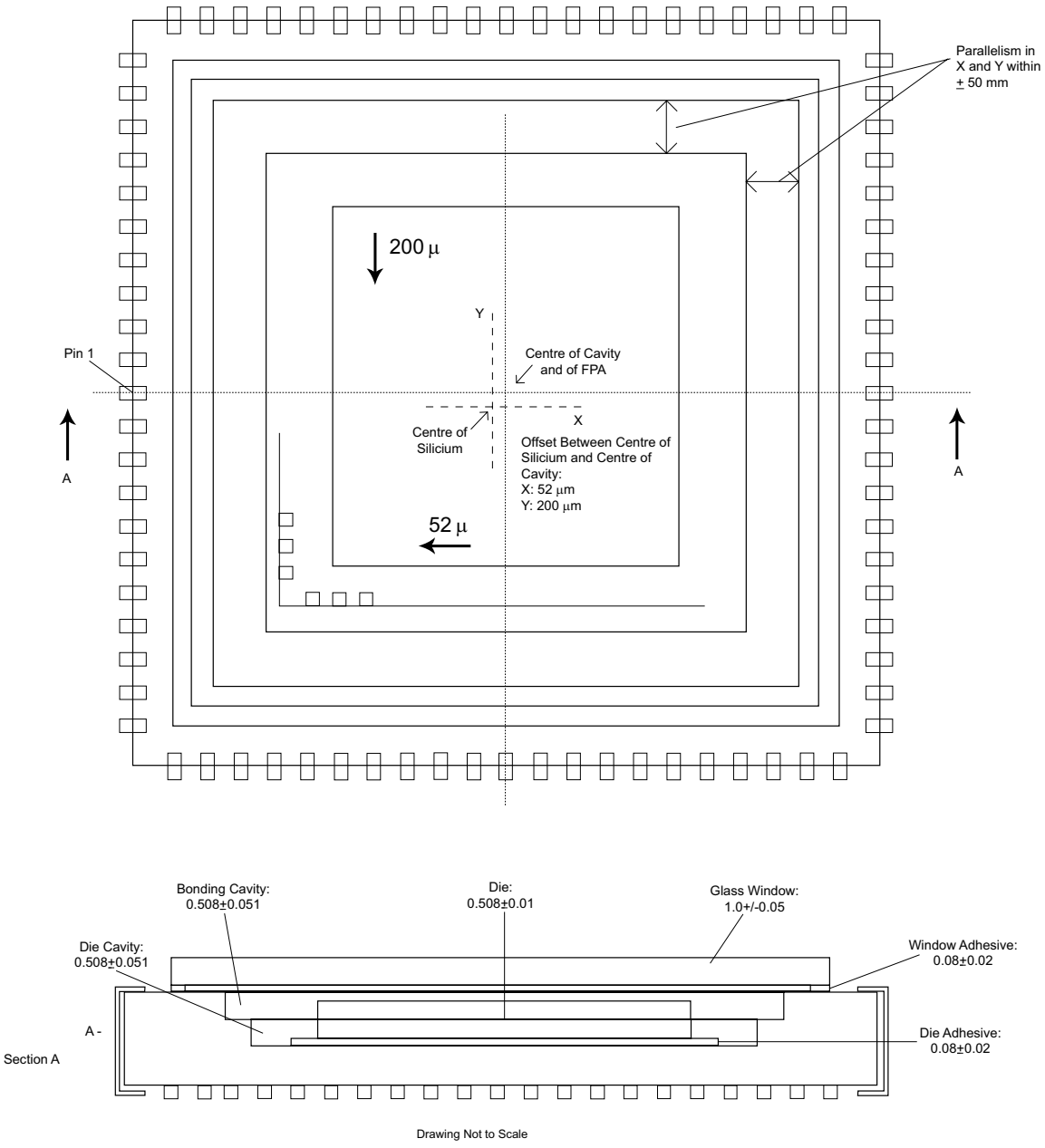
Note: The dimensions in Figure 8.are in inches.

Figure 8. Package Drawing



Die Alignment

Figure 9. Die Alignment



Glass Lids

There are 2 glass lid versions available:

- STAR1000 - Quartz glass with air inside the cavity
- STAR1000BK7 - BK7G18 glass with N_2 inside the cavity

Soldering and Handling

Soldering and Handling Conditions

Take special care when soldering image sensors onto a circuit board. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. The following recommendations are made to ensure that sensor performance is not compromised during end users' assembly processes.

Board Assembly

The STAR250 is very sensitive to ESD. Device placement onto boards should be done in accordance with strict ESD controls for Class 0, JESD22 Human Body Model, and Class A, JESD22 Machine Model devices. Assembly operators need to always wear all designated and approved grounding equipment; grounded wrist straps at ESD protected workstations are recommended including the use of ionized blowers. All tools should be ESD protected.

Manual Soldering

When a soldering iron is used the following conditions should be observed:

Use a soldering iron with temperature control at the tip. The soldering iron tip temperature should not exceed 350°C.

The soldering period for each pin should be less than five seconds.

Reflow Soldering

Reflow soldering is not allowed.

Precautions and Cleaning

Avoid spilling solder flux on the cover glass; bare glass and particularly glass with antireflection filters may be harmed by the flux. Avoid mechanical or particulate damage to the cover glass.

Use isopropyl alcohol (IPA) as a solvent for cleaning the image sensor glass lid. When using other solvents, it should be confirm whether the solvent will dissolve the package and/or the glass lid.

RoHS (lead free) Compliance

This paragraph reports the use of Hazardous chemical substances as required by the RoHS Directive (excluding packing material).

Table 9. Chemical Substances in STAR250 Sensor

Chemical Substance	Any intentional content	If there is any intentional content, in which portion is it contained?
Lead	NO	-
Cadmium	NO	-
Mercury	NO	-
Hexavalent chromium	NO	-
PBB (Polybrominated biphenyls)	NO	-
PBDE (Polybrominated diphenyl ethers)	NO	-

Information on Lead Free Soldering

The product cannot withstand a lead free soldering process. Reflow or wave soldering Is not recommended. Hand soldering is needed for this part type. Solder 1 pin on each side and let the sensor cool down for minimum 1 minute before continuing.

Note: "Intentional content" is defined as any material demanding special attention is contained into the inquired product by these cases:

1. A case that the above material is added as a chemical composition into the inquired product intentionally in order to produce and maintain the required performance and function of the intended product
2. A case that the above material, which is used intentionally in the manufacturing process, is contained in or adhered to the inquired product.

The following case is not treated as "intentional content":

A case that the above material is contained as an impurity into raw materials or parts of the intended product. The impurity is defined as a substance that cannot be removed industrially, or it is produced at a process like chemical composing or reaction and it cannot be removed technically.

Ordering Information

Table 10. Ordering Information

FillFactory Part Number	Cypress Part Number	Package	Glass Lid	Mono/Color
STAR1000	CYIS1SM1000AA-HQC	84-pin JLCC	Quartz	Mono
STAR1000-BK7	CYIS1SM1000AA-HHC	84-pin JLCC	BK7G18	Mono

Disclaimer

FillFactory image sensors are only warranteed to meet the specifications as described in the production data sheet. FillFactory reserves the right to change any information contained herein without notice.

Please contact info@FillFactory.com for more information.

APPENDIX A: STAR1000 Evaluation System

For evaluating purposes, a STAR1000 evaluation kit is available.

The STAR1000 evaluation kit consists of a multifunctional digital board (memory, sequencer, and IEEE 1394 Fire Wire interface) and an analog image sensor board.

Visual Basic software (under Windows 2000 or XP) allows the grabbing and display of images from the sensor. All acquired images can be stored in different file formats (8 or 16-bit). All settings can be adjusted dynamically to evaluate the sensors specs. Default register values can be loaded to start the software in a desired state.

Document History Page

Document Title: STAR1000 1M Pixel Radiation Hard CMOS Image Sensor Document Number: 38-05714				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	310213	SEE ECN	SIL	Initial Cypress release
*A	603177	SEE ECN	QGS	Converted to Framemaker Format
*B	649371	SEE ECN	FPW	Package spec label update + ordering information update