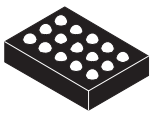
LV52133A

Programmable DC-DC Converter, ±5V dual-output, Single-Inductor

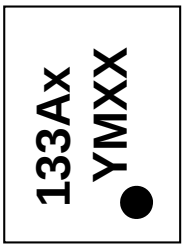
ON Semiconductor®
www.onsemi.com



WLCSP15, 0.4mm pitch
(2.15mm x 1.55mm, Amax=0.650 mm)

MARKING DIAGRAM

TOP view



● = Device Mark
XX = Assembly lot Code

ORDERING INFORMATION

Ordering Code:
LV52133A0XA-VH
LV52133A5XA-VH

Package
WLCSP15 (2.15x1.55)
(Pb-Free / Halogen Free)

Shipping (Qty / packing)
4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Overview

LV52133A0XA and LV52133A5XA are dc-dc converters specifically designed for LCD panels. These dc-dc converters generate two different output voltages from a single inductor. Each of the output voltages are adjustable from ±4.1 V to ±5.7V. LCD panel power modules using these dc-dc converters can be implemented within smaller board footprints, compared to converters that require dual inductors. The short circuit protection function, integrated for both positive and negative output pins, provides protection from continuous overcurrent when the output is shorted. This feature enhances the safety of the design. The extremely low standby current (0.3µA typical) enables longer application operating time.

The differences of the LV52133A0XA-VH and LV52133A5XA-VH are shown in below table.

Table. Correspondence table of between Vout1/2's default voltages and the marking vs product names

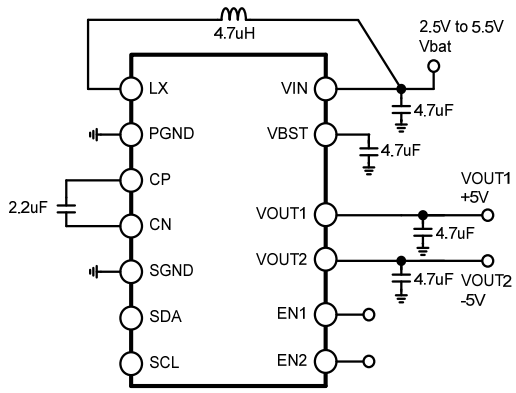
	LV52133A0XA-VH	LV52133A5XA-VH
Default voltages	±5.0V	±5.5V
Marking	133A0 YMXX	133A5 YMXX

Features

- Dual-Outputs by Single-Inductor architecture
- VOUT1 default output voltage (+5.0V/+5.5V)
- VOUT2 default output voltage (–5.0V/ –5.5V)
- Adjustable both output voltages by I^2C (I^2C disable at standby)
- Operating voltage range 2.5V to 5.5V
- High speed inverted charge pump technology
- Short Circuit Protection
- Standby current dissipation 0.3µA

Typical Applications

- Mobile LCD panel power supply
- General around ±5.0V applications



Typical Application Diagram

* I^2C Bus is a trademark of Philips Corporation.

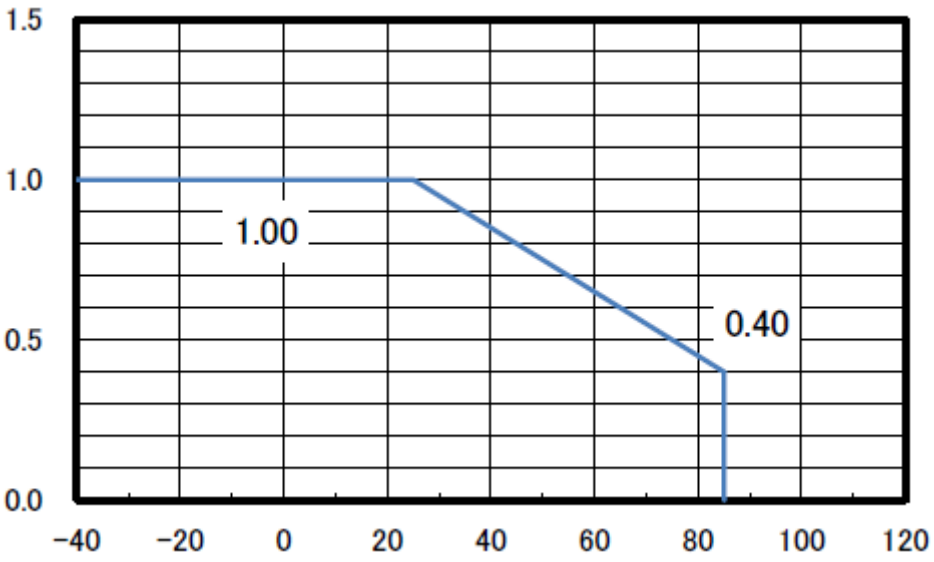
Specifications

Absolute Maximum Ratings at Ta = 25°C (Note 1)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VINmax	VIN to GNDs	+6	V
Maximum Pin voltage1	Vpin1max	CN,VOUT2 to GNDs	–6	V
Maximum Pin voltage2	Vpin2max	LX	+7	V
Maximum Pin voltage3	Vpin3max	Other pin to GNDs	+6	V
Allowable power dissipation	Pdmax	Ta=25°C The specified board (Note2)	1	W
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

1. Stresses exceeding those listed in the Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Mounted on a specified board: 50mm×50mm×1mm (2 layer glass epoxy)
3. Absolute maximum ratings represent the values which cannot be exceeded for any length of time.
4. Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be decrease. Please contact ON Semiconductor for the further details.

Pd-max



Ambient temperature [°C]

(Note 2) Mounted on a specified board: 50mm×50mm×1mm (2 layer glass epoxy)

Recommended Operating Conditions at Ta = 25°C (Note 5)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	VIN_{op}		2.5 to 5.5	V

5. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics (Note 6)

VIN=3.7V VOUT1=5.0V VOUT2=-5.0V at Ta = 25°C, (Unless otherwise noted)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
VIN current						
Standby current	ICC1	EN1=EN2=OFF		0.3		μA
VBST Boost Converter						
VBST current limit	ICLBST	LX		1.2		A
VOUT1 LDO						
VOUT1 voltage	VOUT1	Default		5.0/5.5		V
VOUT1 voltage range	VOUT1	100mVsteps by I2C	4.1		5.7	V
VOUT1 voltage accuracy	VOUT1		–1		1	%
VOUT1 current	IOUT1	IOUT2=0		200		mA
VOUT1 line regulation	VLINR1	dVo=1V Io=30mA		0.3		%/V
VOUT1 load regulation	VLDR1	Io=2mA/150mA		4		mV
Discharge Resistance 1	RVO1			70		Ω
Soft-start	tssvo1			0.6		ms
VOUT2 Inverted Charge pump						
VOUT2 voltage	VOUT2	Default		–5.0/–5.5		V
VOUT2 voltage range	VOUT2R	100mV steps by I2C	–5.7		–4.1	V
VOUT2 voltage accuracy	VOUT2A		–1		1	%
VOUT2 current	IOUT2	IOUT1=0		100		mA
VOUT2 line regulation	VLINR2	dVo=1V Io=30mA		0.3		%/V
VOUT2 load regulation	VLDR2	Io=2mA/60mA		20		mV
Discharge Resistance 2	RVO2			20		Ω
Soft-start	tssvo2			0.8		ms
Oscillator						
OSC frequency1	Fosc1	Boost converter	1.48	1.85	2.22	MHz
OSC frequency2	Fosc2	Inverted charge pump	0.74	0.925	1.11	MHz
Under Voltage Locked Out						
UVLO up	Vuvlo_h	VIN up		2.3		V
UVLO down	Vuvlo_l	VIN down		2.1		V
Control Input						
High level input voltage	VINH	SDA/SCL/EN1/EN2	1.26		VIN	V
Low level input voltage	VINL	SDA/SCL/EN1/EN2	0		0.54	V
Pulldown Resistance1	Rpd1	EN1		400		kΩ
Pulldown Resistance2	Rpd2	EN2		200		kΩ

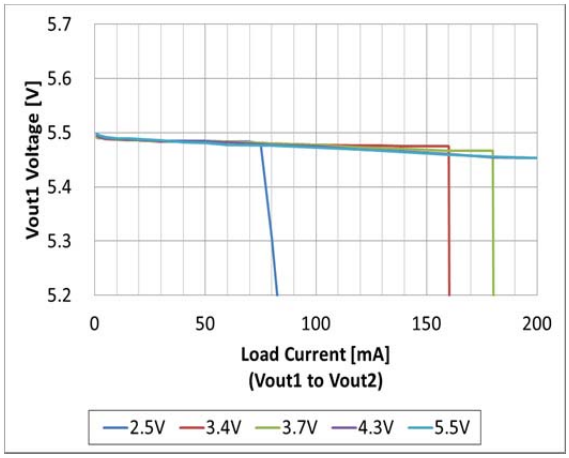
6. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL OPERATING CHARACTERISTICS

VIN=3.7V at Ta = 25°C, (Unless otherwise noted)

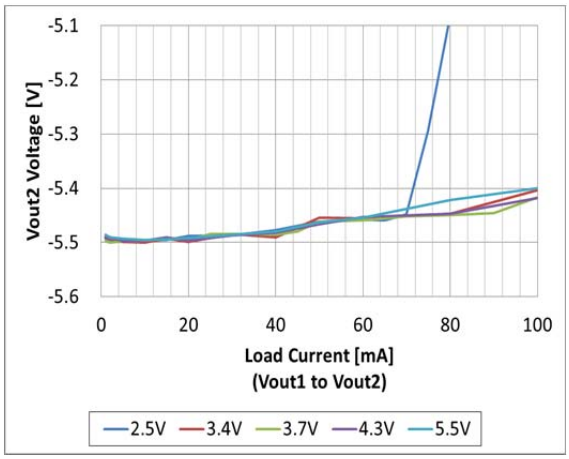
Load regulation of Vout1

The load current is from Vout1 to Vout2.



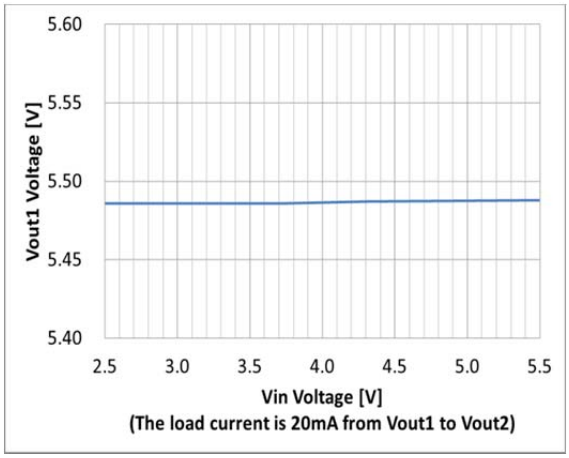
Load regulation of Vout2

The load current is from Vout1 to Vout2.



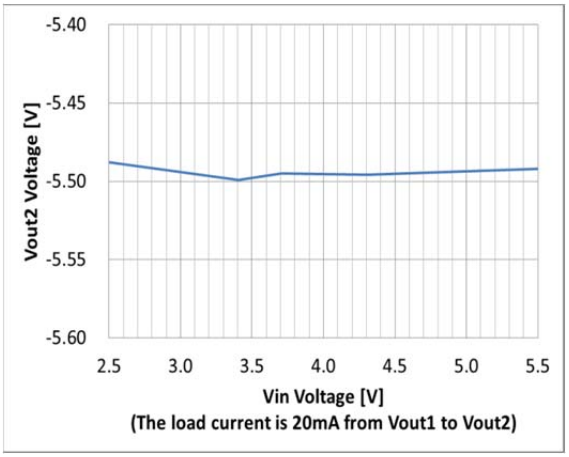
Line regulation of Vout1

The load current is 20mA from Vout1 to Vout2.



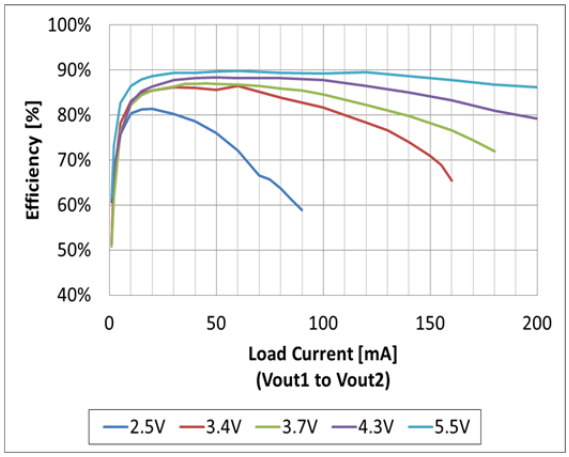
Line regulation of Vout2

The load current is 20mA from Vout1 to Vout2.



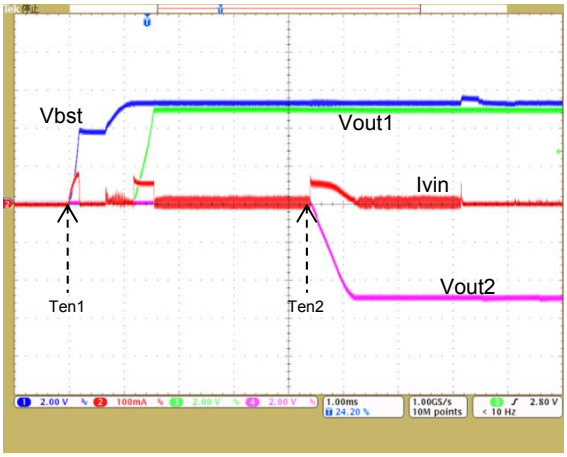
Efficiency

The load current is from Vout1 to Vout2.



Startup waveform example

The output voltages are set |5.0V|.



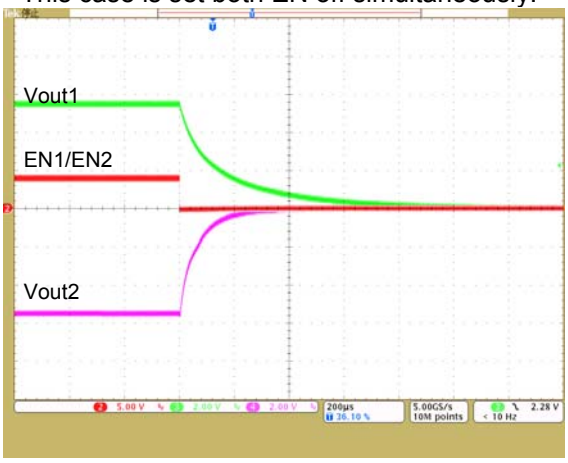
Ten1: EN1 pin = ON, Ten2: EN2 pin = ON

TYPICAL OPERATING CHARACTERISTICS

VIN=3.7V at Ta = 25°C, (Unless otherwise noted)

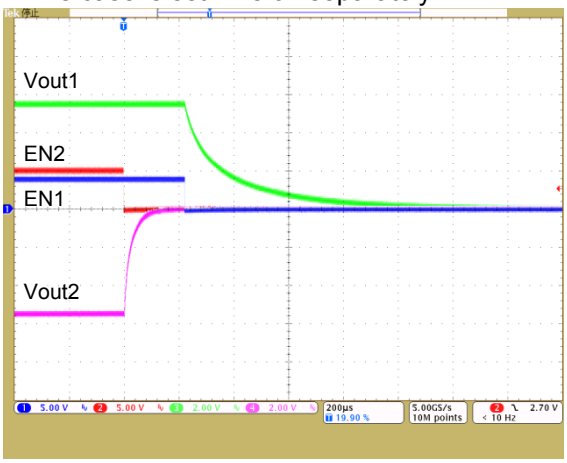
Shutdown waveform1

This case is set both EN off simultaneously.



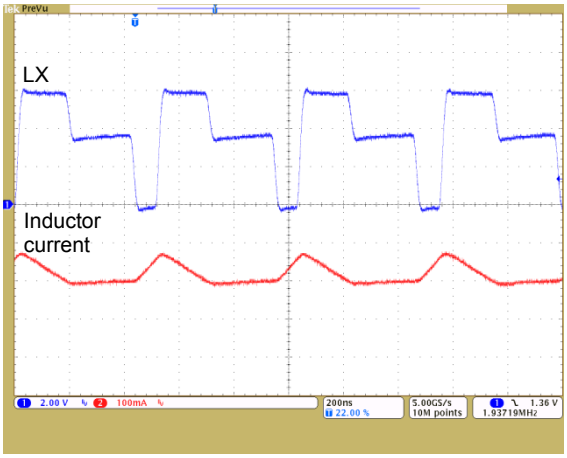
Shutdown waveform2

This case is set ENs off separately.



Boost converter - switching waveform1

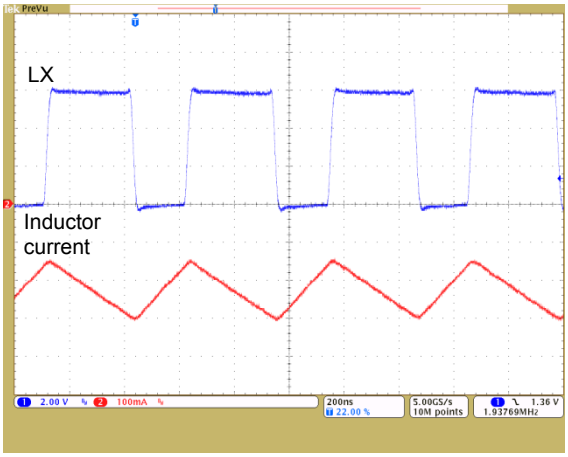
The load current is 5mA from Vout1 to Vout2.



ch2: offset=200mA

Boost converter - switching waveform2

The load current is 50mA from Vout1 to Vout2.

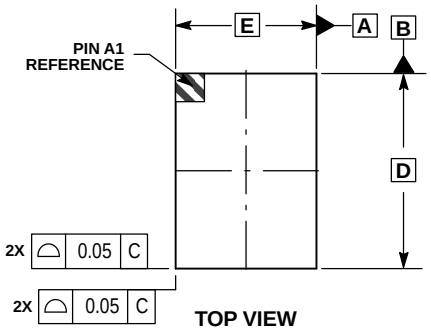


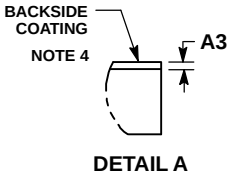
ch2: offset=400mA

Package Dimensions

unit : mm

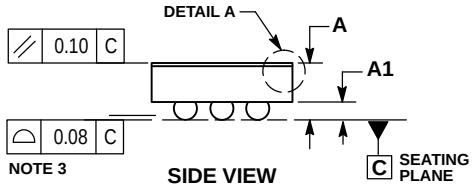
WLCSP15, 2.15x1.55
CASE 567HY
ISSUE B

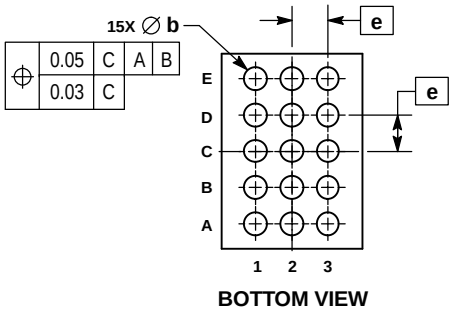




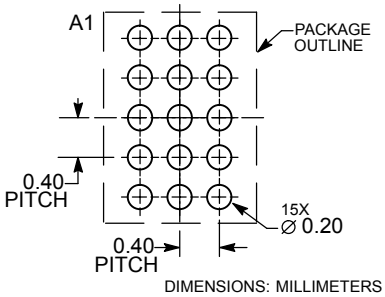
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.
4. BACKSIDE COATING IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.65
A1	0.16	0.26
A3	0.025 REF	
b	0.21	0.31
D	2.15 BSC	
E	1.55 BSC	
e	0.40 BSC	





RECOMMENDED SOLDERING FOOTPRINT*

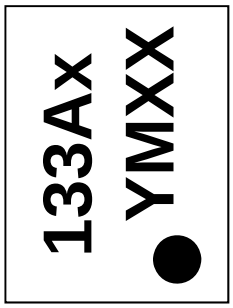


DIMENSIONS: MILLIMETERS

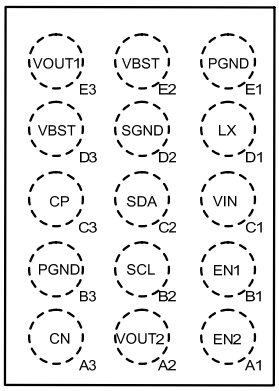
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

LV52133A0XA-VH/LV52133A5XA-VH is as follows.

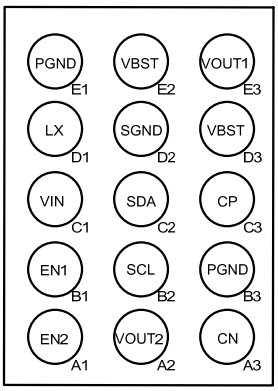
MARKING DIAGRAM
Top view



Top view (1)



Top view (2)



Bottom view

● = Device Mark
XX = Assembly lot Code

Pin Function

PIN #	Pin Name	Description
A1	EN2	Enable1 input pin
A2	VOUT2	VOUT2 output pin
A3	CN	Flying capacitor connection pin for charge pump
B1	EN1	Enable1 input pin
B2	SCL	I2C clock signal input pin
B3/E1	PGND	Power Ground
C1	VIN	Power supply voltage
C2	SDA	I2C data signal input / output pin
C3	CP	Flying capacitor connection pin for charge pump
D1	LX	Boost converter switching pin
D2	SGND	Signal Ground
D3/E2	VBST	Boost converter direct output pin
E3	VOUT1	VOUT1 output pin

I²C serial bus communication

BITMAP (I2C control) / I2C disable at standby

WRITE: IC Address : 0111110x x=0:Write mode / x=1:inhibition

	Sub Address	MSB (7)	(6)	(5)	(4)	(3)	(2)	(1)	LSB (0)
VOUT1	0000 0000	-	-	-	VOUT1	VOUT1	VOUT1	VOUT1	VOUT1
VOUT2	0000 0001	-	-	-	VOUT2	VOUT2	VOUT2	VOUT2	VOUT2

bits	VOUT1 [V]	VOUT2 [V]
0	not use	not use
1	4.1	–4.1
2	4.2	–4.2
3	4.3	–4.3
4	4.4	–4.4
5	4.5	–4.5
6	4.6	–4.6
7	4.7	–4.7
8	4.8	–4.8
9	4.9	–4.9
10	5.0*	–5.0*
11	5.1	–5.1
12	5.2	–5.2
13	5.3	–5.3
14	5.4	–5.4
15	5.5**	–5.5**
16	5.6	–5.6
17	5.7	–5.7

* :default = ±5.0V (LV52133A0XA-VH)

** :default = ±5.5V (LV52133A5XA-VH)

Serial Bus Communication Specifications

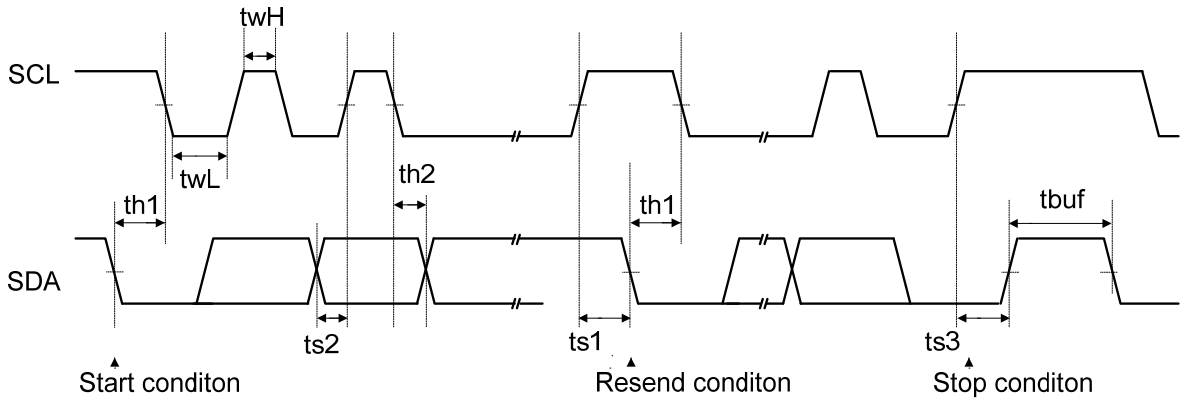
Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0	-	100	kHz
Data set up time	ts1	SCL setup time relative to the fall of SDA	4.7	-	-	μs
	ts2	SDA setup time relative to the rise of SCL	250	-	-	ns
	ts3	SCL setup time relative to the rise of SDA	4.0	-	-	μs
Data hold time	th1	SCL data hold time relative to the rise of SDA	4.0	-	-	μs
	th2	SDA hold time relative to the fall of SCL	0	-	-	μs
Pulse width	twL	SCL pulse width for the L period	4.7	-	-	μs
	twH	SCL pulse width for the H period	4.0	-	-	μs
Input waveform conditions	ton	SCL and SDA (input) rise time	-	-	1000	ns
	tof	SCL and SDA (input) fall time	-	-	300	ns
Bus free time	tbuf	Time between STOP and START conditions	4.7	-	-	μs

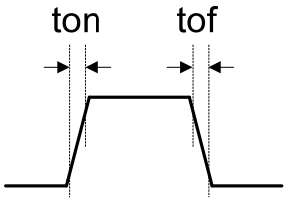
High-speed mode

Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0	-	400	kHz
Data setup time	ts1	SCL setup time relative to the fall of SDA	0.6	-	-	μs
	ts2	SDA setup time relative to the rise of SCL	100	-	-	ns
	ts3	SCL setup time relative to the rise of SDA	0.6	-	-	μs
Data hold time	th1	SCL data hold time relative to the rise of SDA	0.6	-	-	μs
	th2	SDA hold time relative to the fall of SCL	0	-	-	μs
Pulse width	twL	SCL pulse width for the L period	1.3	-	-	μs
	twH	SCL pulse width for the H period	0.6	-	-	μs
Input waveform conditions	ton	SCL and SDA (input) rise time	-	-	300	ns
	tof	SCL and SDA (input) fall time	-	-	300	ns
Bus free time	tbuf	Time between STOP and START conditions	1.3	-	-	μs

I^2C serial transfer timing conditions

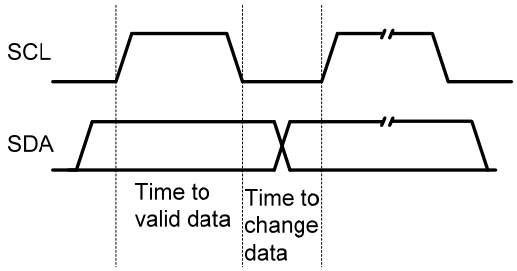


Input waveform condition



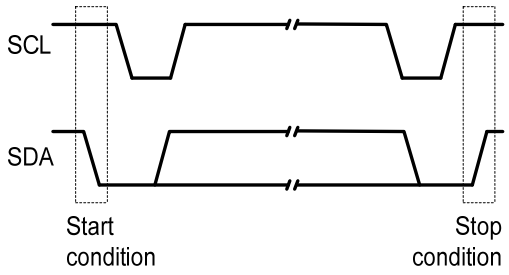
I2C control transmission method

In start and stop conditions of the I^2C bus, SDA should be kept in the constant state while SCL is "H" as shown below during data transfer.



When data transfer is not made, both SCL and SDA are in the "H" state.
When SCL = SDA="H", change of SDA from "H" to "L" enables the start conditions to start access.

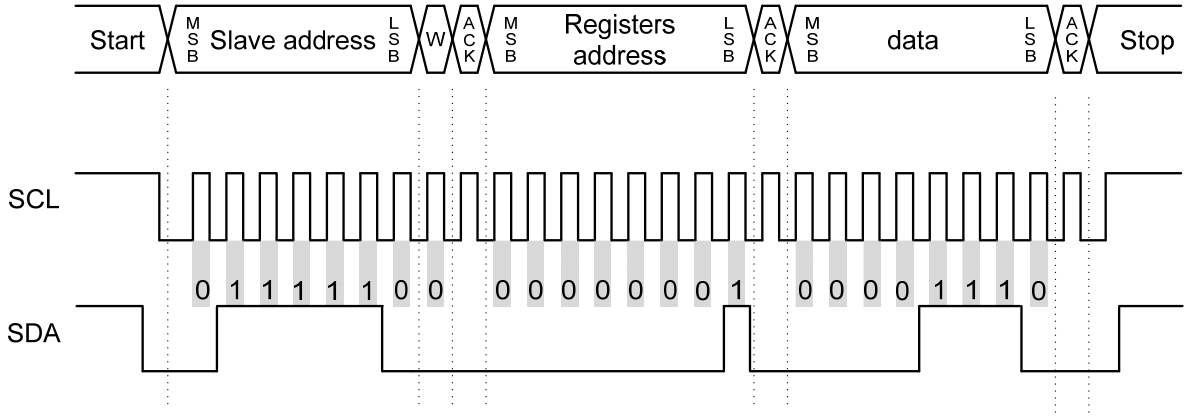
When SCL is "H", change of SDA from "L" to "H" enables the stop conditions to stop access.



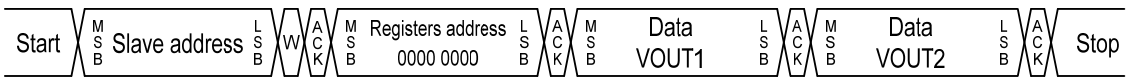
Data transfer and acknowledgement response

After establishment of start conditions, Data transfer is made by one byte (8-bits). Data transfer enables continuous transfer of any number of bytes. Each time of the 8-bit data is transferred, the ACK signal is sent from the receive side to the send side. The ACK signal is issued when SDA(on the send side) is released and SDA(on the receive side) is set "L" immediately after fall of the clock pulse at the SCL eighth bit of data transfer to "L". When the next 1-byte transfer is left in the receive state after transmission of the ACK signal from the receive side, the receive side releases SDA at fall of the SCL ninth clock. In the I2C bus, there is no CE signal. Instead, 7-bit slave address is assigned to each device and the first byte of transfer is assigned to the command (R/W) representing the 7-bit slave address and subsequent transfer direction. Note that only WRITE is valid in this IC. The 7-bit address is transferred sequentially from MSB and the eighth bit is "L" representing WRITE.

Input 1data



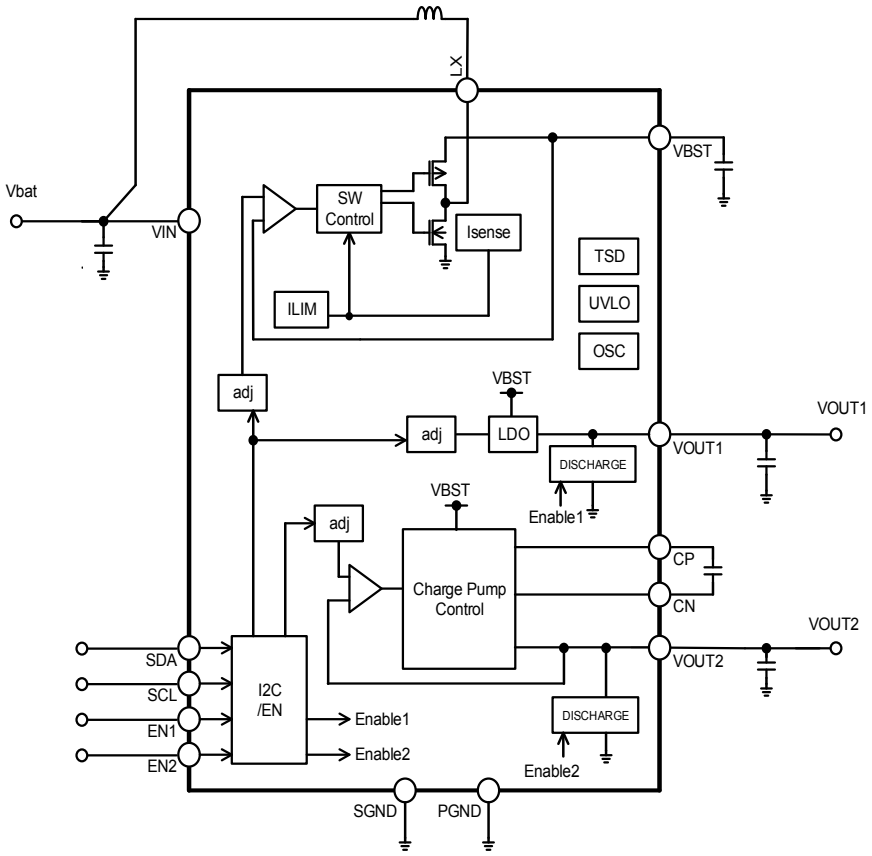
Input 2data (register address auto Increment)



Detailed Descriptions

The LV52133A has dual-output VOUT1 (LDO) and VOUT2 (built-in inverted charge pump) with single inductor. Both output voltages are separately controlled by I2C control and pin EN1/EN2. Boost converter is a fixed-frequency pulse width modulated (PWM) regulator. At rated load, each converter operates at continuous conduction mode (CCM). At light loads, both converters can enter in discontinuous conduction mode (DCM). A cycle-by-cycle peak current limit and thermal provide value added features to protect the device.

Block Diagram



Recommendation Applications

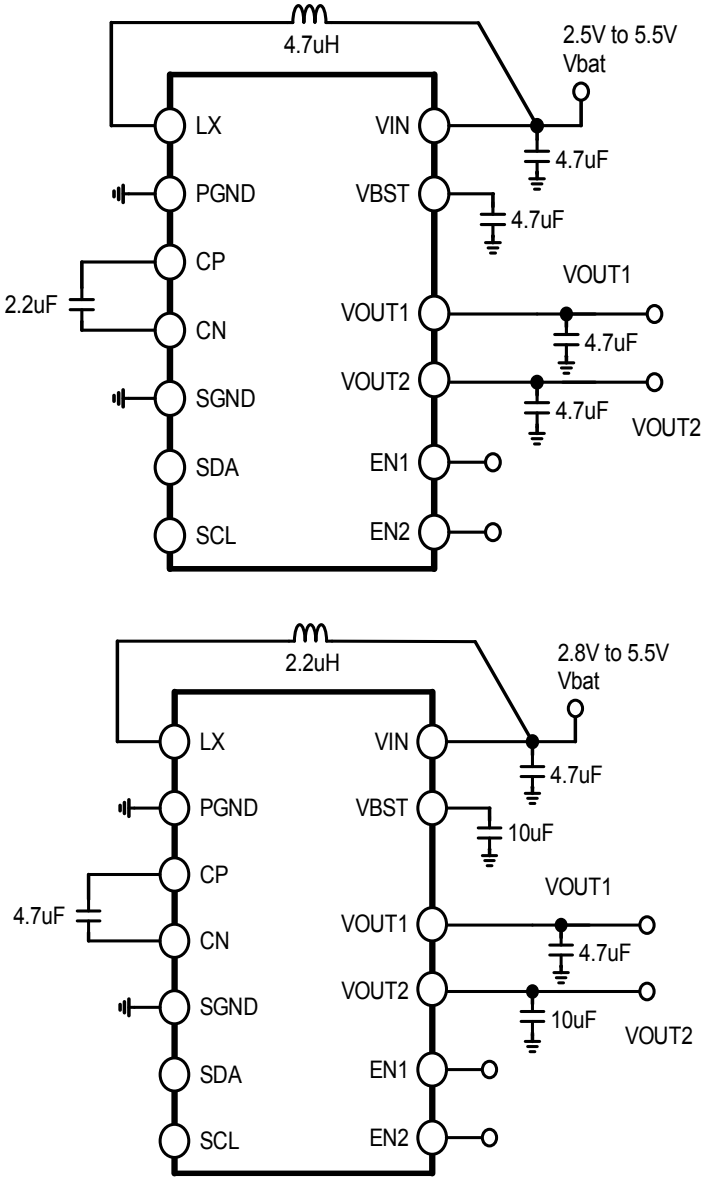


Fig. Recommendation Applications

Table . Component List for Typical Characteristics Circuit

Reference	Description	Manufacturer and Part Number
C	2.2μF, ±10%, 10V, X5R, ceramic	TDK – C1608X5R1A225K
	4.7μF, ±10%, 10V, X5R, ceramic	TDK – C1608X5R1A475K
	10μF, ±10%, 10V, X5R, ceramic	TDK – C1608X5R1A106K
L	2.2μH, 1.1A, 120mΩ, 2.5mm×2.0mm×1.1mm	TDK – MLP2520V2R2ST0S1
	4.7μH, 0.8A, 220mΩ, 2.5mm×2.0mm×1.1mm	TDK – MLP2520V4R7ST0S1

Inductor Selection

Three different electrical parameters need to be considered when selecting an inductor, the value of the inductor, the saturation current and the DCR. During normal and heavy load operation, the LV52133A is intended to operate in Continuous Conduction Mode (CCM). The equation below can be used to calculate the peak current.

$$Ipeak\_p = Iout1 / (n1 \times (1 - D1)) + (VIN \times D1) / 2 \times L1 \times Fosc1$$

VIN: battery voltage, IOUT1:load current, L:inductor value, Fosc1: OSC frequency1, D1:duty cycle, n1:converter efficiency varies with load current.

A good approximation is to use $\eta = 0.85$. It is important to ensure that the inductor current rating is high enough such that it not saturate. As the inductor size is reduced, the peak current for a given set of conditions increases along with higher current ripple so it is not possible to deliver maximum output power at lower inductor values. Finally an acceptable DCR must be selected regarding losses in the inductor and must be lower than 250mΩ (typical) to limit excessive voltage drop. In addition, as DCR is reduced, overall efficiency will improve. The inductor value is recommended to use a 4.7μH or 2.2μH.

POR function

This is “Power On Reset” function to reset internal logic circuits. This function can be worked by reducing IC’s VIN voltage until about 1V.

Start/Shutdown Sequencing

The pins EN1/EN2 are used as enable input logic. An active high logic level on those pins enables the device. A built-in pull-down resistor disables the device if the pin is left open. If a high logic signal is applied, the LV52133A starts with timing sequence as depicted below figure that is as in often cases of panel power supply. In the figure, VOUT1’s ramp up time is shown as 600μs. This is the case that the VOUT1 output capacitance is selected 4.7μF. If the capacitance is 10μF, the ramp up time becomes 1.3ms. according to next formula. The T_{rampup} had better be kept within 2.5ms in order to avoid highly inrush current. If the time is over 2.5ms, IC can also wake up with larger current limiter, which is described in OCP section. And next, time of VOUT2’s ramp-up is also same idea as VOUT1. Please estimate by changing the 600μs to 800μs in the same expression.

$$T_{rampup} = 600us \times \frac{Cx}{4.7uF}$$

Typically the next step is starting of panel load in the case of VOUT2. The timing from EN2=ON is needed over 2.5ms and over calculated time with the above equations. This is only to avoid unnecessary inrush current. Even if over the time, each output involves the unnecessary inrush current, but is able to wake up outputs.

When each EN is off, active discharge resistance work always in each output, and the output voltage goes to GND voltage.

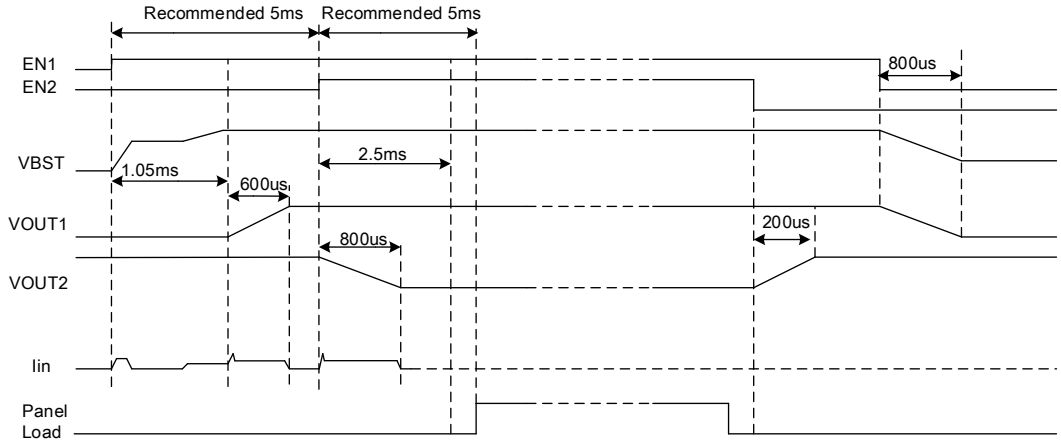


Fig. Typically Sequence Diagram

OCP and SCP function

IC has OCP and SCP function and explained the behavior shown in figures below in some situations.

(1) OCP limit transition in normal operation

The OCP means “Over Current Protection” and is equipped for preventing excessive inrush current about Vout1 in the startup sequence and more. It watches for limit of 40mA during 2.5msec from ramp up of Vout1, and then changes almost free, which mean depending on VBST current capacity.

(2) Heavy load of during ramp up

As shown in the below fig, if it is not reaching target voltage at the end of the 2.5ms for some reasons as large capacitance or large load current, then the OCP is changed to 230mA mode till reaching the target voltage. And after the reaching the target voltage, OCP is changed to depending on VBST mode.

Therefore in the case that the load current is under 230mA, VOUT1 voltage can be raised. But from the viewpoint of suppressing the inrush current (about 500mA), the use of this 230mA is better to avoid as much as possible by capacitance selection and timing design of panel module.

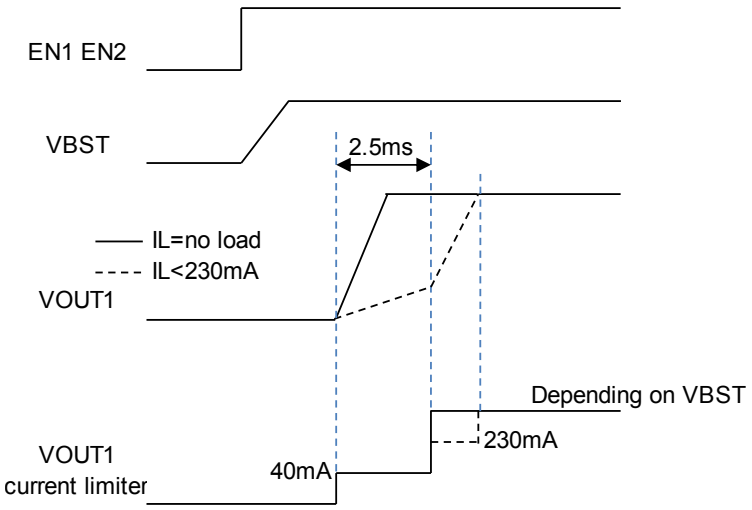


Fig. OCP behavior in some situations

(3) SCP function

The SCP means “Short Circuit Protection”. This is used to protect each Vout when they are connected to the GND. SCP function becomes active when Vout voltage reaches under 60% of its target voltage. Once SCP is activated, the counter begins to count 10msec. If the SCP detection is active for full 10msec, IC then gets shut down and latch. On the other hand, if the Vout voltage is recovered within this 10msec IC will reactivate. This latch is released by setting EN1 and EN2 to off.

Reference sequence design

For start up

(1) EN1=H ;

(2) After 5msec from (1), EN2=H;

(3) 5msec later, start panel load;

For shut down

(1) stop panel load;

(2) EN1 and EN2 = L;

(3) till Next EN1=H, space more than 1msec;