

NB100LVEP221

2.5V/3.3V 1:20 Differential HSTL/ECL/PECL Clock Driver

The NB100LVEP221 is a low skew 1-to-20 differential clock driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The two clock inputs are differential ECL/PECL; CLK1/ $\overline{\text{CLK1}}$ can also receive HSTL signal levels. The LVPECL input signals can be either differential configuration or single-ended (if the V_{BB} output is used).

The LVEP221 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure tightest skew, both sides of differential outputs should be terminated identically into $50\ \Omega$ even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The NB100LVEP221, as with most other ECL devices, can be operated from a positive V_{CC} supply in LVPECL mode. This allows the LVEP221 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on PECL terminations, designers should refer to Application Note AND8020/D.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended LVPECL input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a $0.01\ \mu\text{F}$ capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Single-ended CLK input operation is limited to a $V_{\text{CC}} \geq 3.0\ \text{V}$ in LVPECL mode, or $V_{\text{EE}} \leq -3.0\ \text{V}$ in NECL mode.

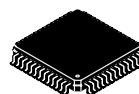
- 15 ps Typical Output-to-Output Skew
- 40 ps Typical Device-to- Device Skew
- Jitter Less than 2 ps RMS
- Maximum Frequency > 1.0 GHz Typical
- Thermally Enhanced 52-Lead LQFP
- V_{BB} Output
- 540 ps Typical Propagation Delay
- LVPECL and HSTL Mode Operating Range:
 $V_{\text{CC}} = 2.375\ \text{V}$ to $3.8\ \text{V}$ with $V_{\text{EE}} = 0\ \text{V}$
- NECL Mode Operating Range:
 $V_{\text{CC}} = 0\ \text{V}$ with $V_{\text{EE}} = -2.375\ \text{V}$ to $-3.8\ \text{V}$
- Q Output will Default Low with Inputs Open or at V_{EE}
- Pin Compatible with Motorola MC100EP221



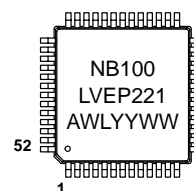
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MARKING DIAGRAM*



52-LEAD LQFP
THERMALLY ENHANCED
CASE 848H
FA SUFFIX



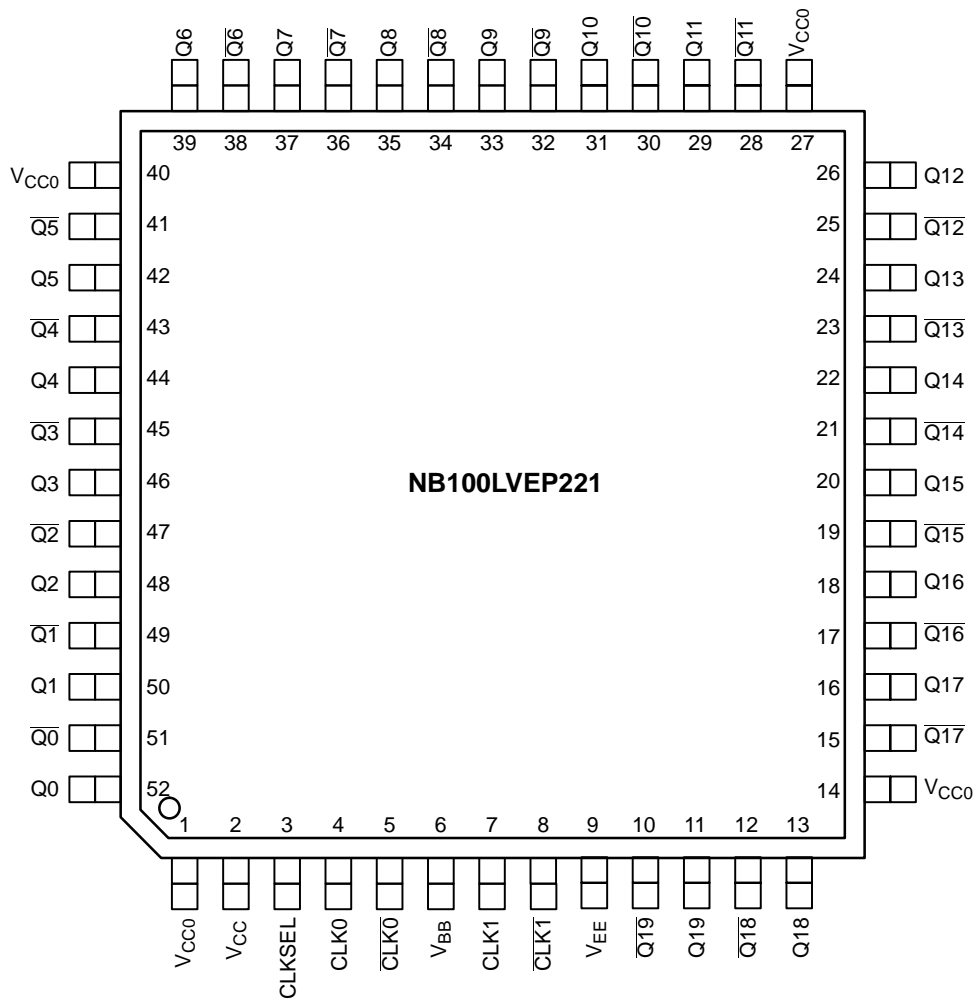
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NB100LVEP221FA	LQFP-52	160 Units/Tray
NB100LVEP221FAR2	LQFP-52	1500/Tape & Reel

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All V_{CC} , V_{CC0} , and V_{EE} pins must be externally connected to appropriate Power Supply to guarantee proper operation. The thermally conductive exposed pad on package bottom (see package case drawing) must be attached to a heat-sinking conduit, capable of transferring 1.2 Watts. This exposed pad is electrically connected to V_{EE} internally.

Figure 1. 52-Lead LQFP Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
CLK0*, $\overline{CLK0}$ **	ECL/PECL Differential Inputs
CLK1*, $\overline{CLK1}$ **	ECL/PECL or HSTL Differential Inputs
Q0:19, $\overline{Q0}$:19	ECL/PECL Differential Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
V_{BB}	Reference Voltage Output
V_{CC}/V_{CC0}	Positive Supply
V_{EE} ***	Negative Supply

* Pins will default LOW when left open.

** Pins will default HIGH when left open.

***The thermally conductive exposed pad on the bottom of the package is electrically connected to V_{EE} internally.

FUNCTION TABLE

CLK_SEL	Active Input
L	CLK0, $\overline{CLK0}$
H	CLK1, $\overline{CLK1}$

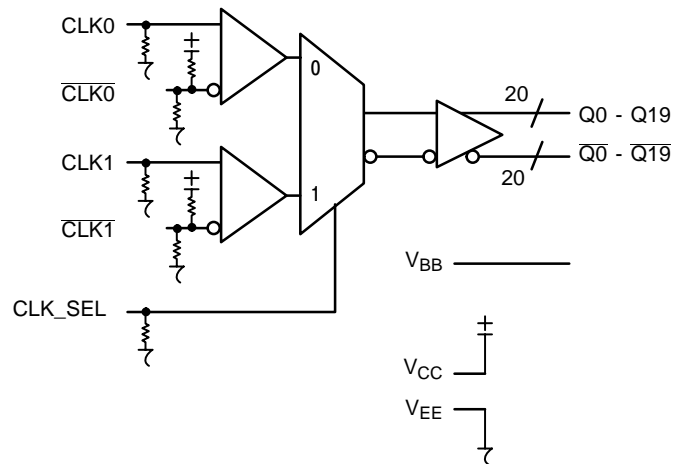


Figure 2. Logic Diagram

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ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 k Ω
Internal Input Pullup Resistor		37.5 k Ω
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 200 V
	Charged Device Model	> 2 kV
Moisture Sensitivity (Note 1)		Level 3
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		533 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, refer to Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		6	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-6	V
V _I	PECL Mode Input Voltage	V _{EE} = 0 V	V _I ≤ V _{CC}	6	V
	NECL Mode Input Voltage	V _{CC} = 0 V	V _I ≥ V _{EE}	-6	V
I _{out}	Output Current	Continuous Surge		50	mA
				100	mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (See Application Information)	0 LFPM	52 LQFP	35.6	°C/W
		500 LFPM	52 LQFP	30	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case) (See Application Information)	0 LFPM	52 LQFP	3.2	°C/W
		500 LFPM	52 LQFP	6.4	°C/W
T _{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC} = 2.5 V; V_{EE} = 0 V (Note 3)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I _{EE}	Power Supply Current	100	125	150	104	130	156	116	145	174	mA	
V _{OH}	Output HIGH Voltage (Note 4)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	
V _{OL}	Output LOW Voltage (Note 4)	555	680	900	555	680	900	555	680	900	mV	
V _{IH}	Input HIGH Voltage (Single-Ended) (Note 5)	1335		1620	1335		1620	1275		1620	mV	
V _{IL}	Input LOW Voltage (Single-Ended) (Note 5)	555		900	555		900	555		900	mV	
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6)											
		CLK0/CLK0	1.2		2.5	1.2		2.5	1.2		2.5	V
		CLK1/CLK1	0.3		1.6	0.3		1.6	0.3		1.6	V
I _{IH}	Input HIGH Current			150			150			150	μA	
I _{IL}	Input LOW Current	CLK	0.5		0.5			0.5			μA	
		CLK	-150		-150			-150				

NOTE: 100LVEP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

- Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary + 0.125 V to -1.3 V.
- All outputs loaded with 50 Ω to V_{CC} - 2.0 V.
- Do not use V_{BB} at V_{CC} < 3.0 V.
- V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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LVPECL DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 7)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	100	125	150	104	130	156	116	145	174	mA
V_{OH}	Output HIGH Voltage (Note 8)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 8)	1355	1480	1700	1355	1480	1700	1355	1480	1700	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1700	1355		1700	1355		1700	mV
V_{BB}	Output Reference Voltage (Note 9)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10) CLK0/CLK0 CLK1/CLK1	1.2 0.3		3.3 1.6	1.2 0.3		3.3 1.6	1.2 0.3		3.3 1.6	V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 100LVEP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

7. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary + 0.925 V to -0.5 V.

8. All outputs loaded with 50 Ω to V_{CC} - 2.0 V.

9. Single-ended input operation is limited $V_{CC} \geq 3.0\text{ V}$ in LVPECL mode.

10. V_{IHCMR} min varies 1:1 with V_{EE} ; V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

LVNECL DC CHARACTERISTICS $V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V}$ to -3.8 V (Note 11)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	100	125	150	104	130	156	116	145	174	mA
V_{OH}	Output HIGH Voltage (Note 12)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 12)	-1945	-1820	-1600	-1945	-1820	-1600	-1945	-1820	-1600	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1600	-1945		-1600	-1945		-1600	mV
V_{BB}	Output Reference Voltage (Note 13)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 14) CLK0/CLK0 CLK1/CLK1	$V_{EE} + 1.2$ $V_{EE} + 0.3$		0.0 -0.9	$V_{EE} + 1.2$ $V_{EE} + 0.3$		0.0 -0.9	$V_{EE} + 1.2$ $V_{EE} + 0.3$		0.0 -0.9	V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 100LVEP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

11. Input and output parameters vary 1:1 with V_{CC} .

12. All outputs loaded with 50 Ω to V_{CC} -2.0 V.

13. Single-ended input operation is limited $V_{EE} \leq -3.0\text{ V}$ in NECL mode.

14. V_{IHCMR} min varies 1:1 with V_{EE} ; V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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HSTL DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}; V_{EE} = 0\text{ V}$

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage CLK1/ $\overline{\text{CLK1}}$	V_x+100		1600	V_x+100		1600	V_x+100		1600	mV
V_{IL}	Input LOW Voltage CLK1/ $\overline{\text{CLK1}}$	-300		V_x-100	-300		V_x-100	-300		V_x-100	mV
V_x	Differential Configuration Cross Point Voltage	680		900	680		900	680		900	mV
I_{IH}	Input HIGH Current	-150		150	-150		150	-150		150	μA
I_{IL}	Input LOW Current CLK1 CLK1	-150 -250			-150 -250			-150 -250			μA

NOTE: 100LVEP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

AC CHARACTERISTICS $V_{CC} = 0\text{ V}; V_{EE} = -2.375\text{ to }-3.8\text{ V}$ or $V_{CC} = 2.375\text{ to }3.8\text{ V}; V_{EE} = 0\text{ V}$ (Note 15)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{Opp}	Differential Output Voltage (Figure 3) $f_{out} < 50\text{ MHz}$ $f_{out} < 0.8\text{ GHz}$ $f_{out} < 1.0\text{ GHz}$	550	700		600	700		600	700		mV
		550	700		550	700		500	700		mV
		500	700		500	700		400	600		mV
t_{PLH}/t_{PHL}	Propagation Delay (Differential Configuration) CLK0-Qx CLK1-Qx		540	600		540	660		540	750	ps
			590	640		590	710		590	800	ps
t_{skew}	Within-Device Skew (Note 16)		15	50		15	50		15	50	ps
	Device-to-Device Skew (Note 17)		40	200		40	200		40	200	ps
t_{JITTER}	Random Clock Jitter (RMS) (Figure 3)		1	2		1	2		1	2	ps
V_{PP}	Input Swing (Differential Configuration) (Note 18) (Figure 4) CLK0 CLK1 HSTL	400	800	1200	400	800	1200	400	800	1200	mV
		300	800	1000	300	800	1000	300	800	1000	mV
DCO	Output Duty Cycle	49.5	50	50.5	49.5	50	50.5	49.5	50	50.5	%
t_r/t_f	Output Rise/Fall Time (20%-80%)	100	200	300	100	200	300	150	250	350	ps

15. Measured with 750 mV source (LVPECL) or 1 V (HSTL) source, 50% duty cycle clock source. All outputs loaded with 50 Ω to $V_{CC}-2\text{ V}$.

16. Skew is measured between outputs under identical transitions and conditions on any one device.

17. Device-to-Device skew for identical transitions, outputs and V_{CC} levels.

18. V_{PP} is the differential configuration input voltage swing required to maintain AC characteristics.

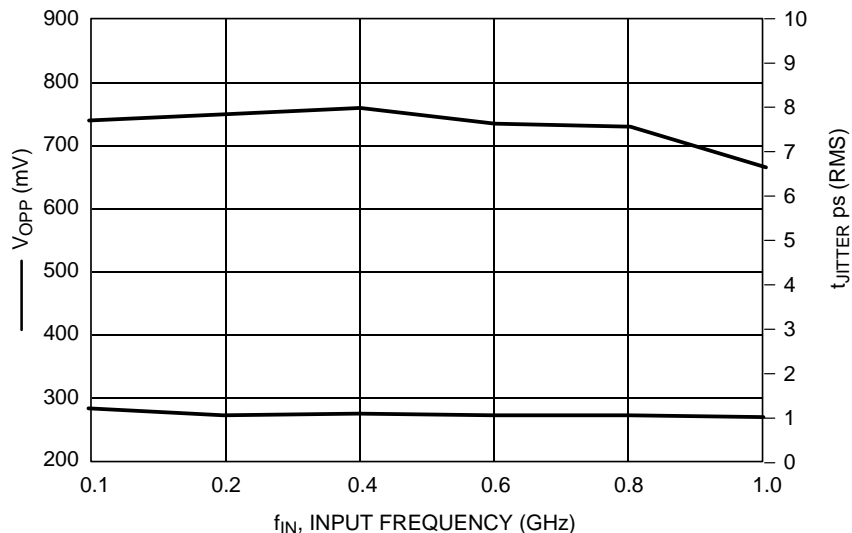


Figure 3. Output Voltage (V_{OPP})/Jitter versus Input Frequency ($V_{CC} - V_{EE} = 3.3\text{ V}$ @ 25°C)

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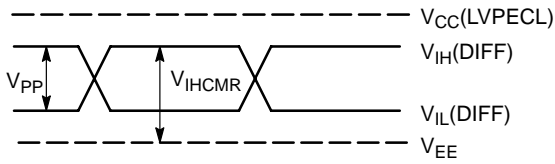


Figure 4. LVPECL Differential Input Levels

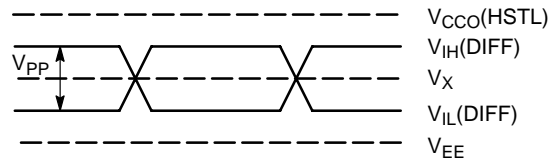


Figure 5. HSTL Differential Input Levels

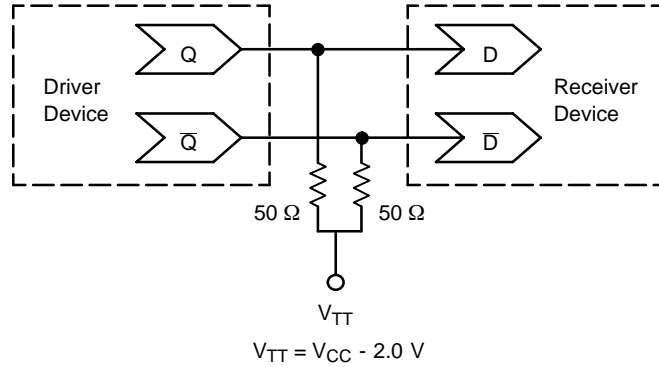


Figure 6. Typical Termination for Output Driver and Device Evaluation
(Refer to Application Note AND8020 - Termination of ECL Logic Devices.)

Resource Reference of Application Notes

- AN1405 - ECL Clock Distribution Techniques
- AND8002 - Marking and Date Codes
- AND8009 - ECLinPS Plus Spice I/O Model Kit
- AND8020 - Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

APPLICATIONS INFORMATION

Using the thermally enhanced package of the NB100LVEP221

The NB100LVEP221 uses a thermally enhanced 52-lead LQFP package. The package is molded so that a portion of the leadframe is exposed at the surface of the package bottom side. This exposed metal pad will provide the low thermal impedance that supports the power consumption of the NB100LVEP221 high-speed bipolar integrated circuit and will ease the power management task for the system design. In multilayer board designs, a thermal land pattern on the printed circuit board and thermal vias are recommended to maximize both the removal of heat from the package and electrical performance of the NB100LVEP221. The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the solderable area should be at least the same size and shape as the exposed pad on the package. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal conduit. The thermal vias will connect the exposed pad of the package to internal copper planes of the board. The number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern.

The recommended thermal land design for NB100LVEP221 applications on multi-layer boards comprises a 4 X 4 thermal via array using a 1.2 mm pitch as shown in Figure 7 providing an efficient heat removal path.

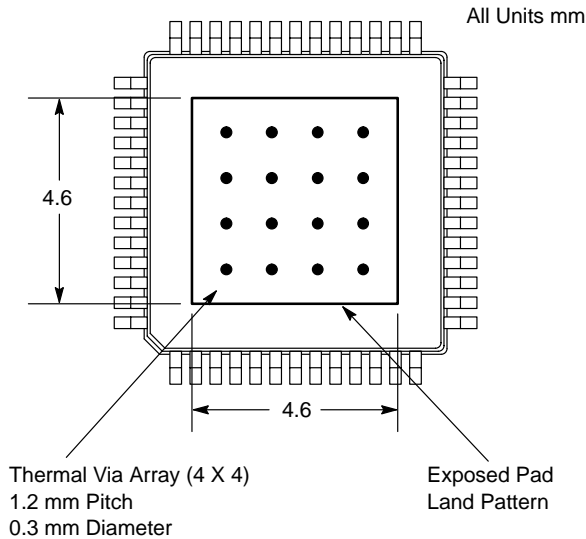


Figure 7. Recommended Thermal Land Pattern

The via diameter should be approximately 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via may result in voiding during the solder process and must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will

supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for the exposed pad package is equivalent to standard surface mount packages. Figure 8, “Recommended solder mask openings”, shows a recommended solder mask opening with respect to a 4 X 4 thermal via array. Because a large solder mask opening may result in a poor rework release, the opening should be subdivided as shown in Figure 8. For the nominal package standoff of 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

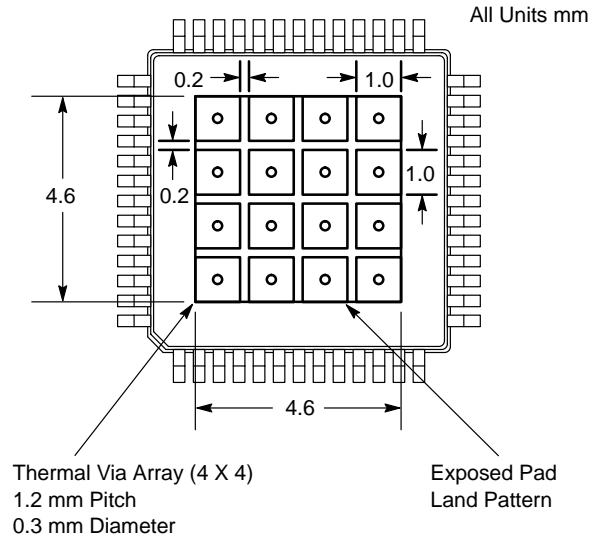


Figure 8. Recommended Solder Mask Openings

Proper thermal management is critical for reliable system operation. This is especially true for high-fanout and high output drive capability products.

For thermal system analysis and junction temperature calculation, the thermal resistance parameters of the package are provided:

Table 1. Thermal Resistance *

LFPM	θ_{JA} °C/W	θ_{JC} °C/W
0	35.6	3.2
100	32.8	4.9
500	30.0	6.4

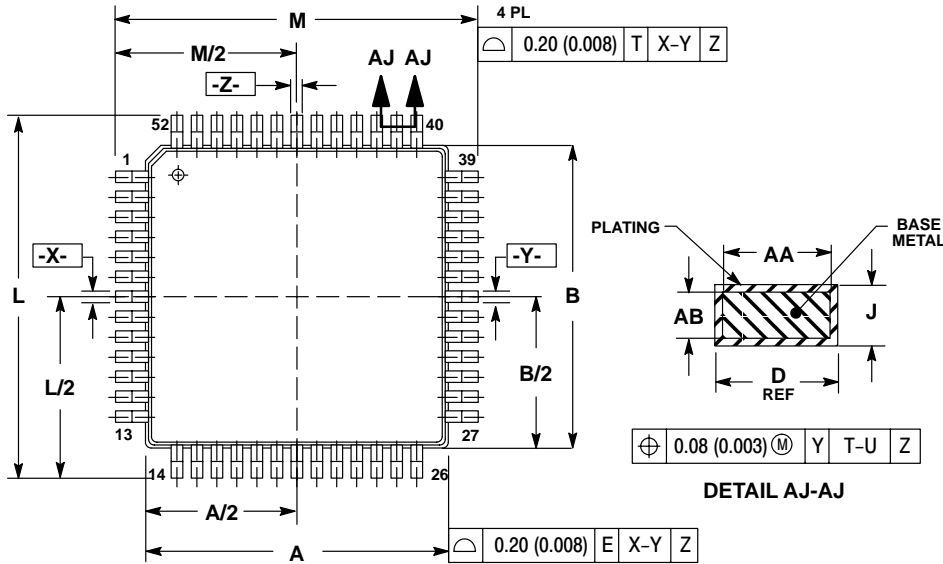
* Junction to ambient and Junction to board, four-conductor layer test board (2S2P) per JESD 51-8

These recommendations are to be used as a guideline, only. It is therefore recommended that users employ sufficient thermal modeling analysis to assist in applying the general recommendations to their particular application to assure adequate thermal performance. The exposed pad of the NB100LVEP221 package is electrically shorted to the substrate of the integrated circuit and V_{EE} . The thermal land should be electrically connected to V_{EE} .

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PACKAGE DIMENSIONS

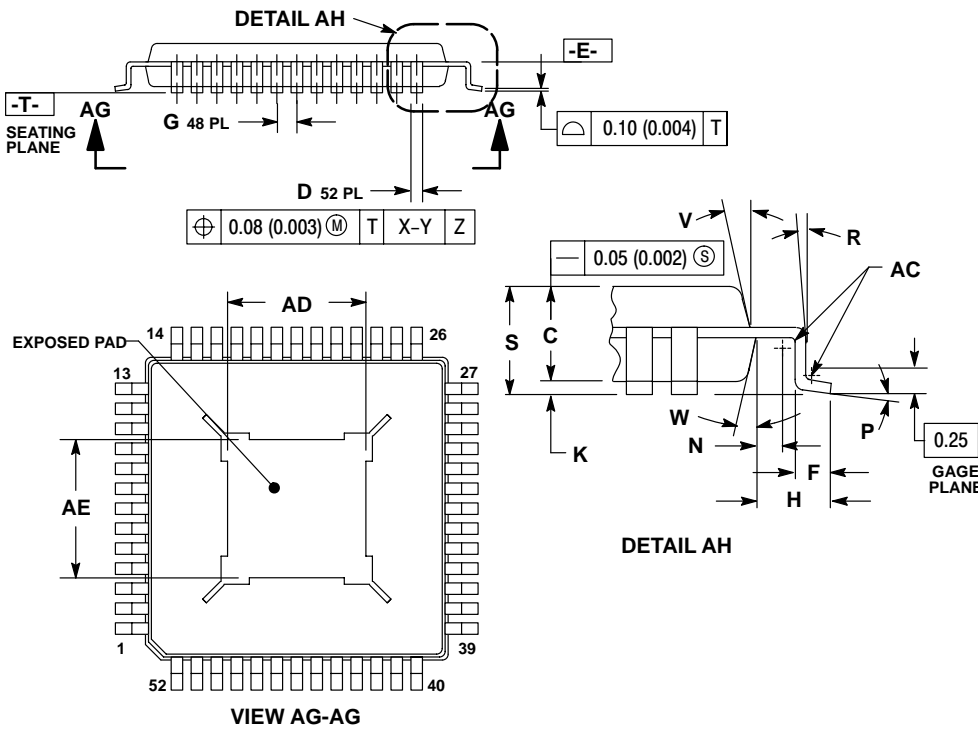
LQFP 52 LEAD EXPOSED PAD PACKAGE CASE 848H-01 ISSUE A




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.
3. DATUM PLANE "E" IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING PLANE.
4. DATUM "X", "Y" AND "Z" TO BE DETERMINED AT DATUM PLANE DATUM "E".
5. DIMENSIONS M AND L TO BE DETERMINED AT SEATING PLANE DATUM "T".
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE "E".
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM D DIMENSION BY MORE THAN 0.08 (0.003). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
B	10.00 BSC		0.394 BSC	
C	1.30	1.50	0.051	0.059
D	0.22	0.40	0.009	0.016
F	0.45	0.75	0.018	0.030
G	0.65 BSC		0.026 BSC	
H	1.00 REF		0.039 BSC	
J	0.09	0.20	0.004	0.008
K	0.05	0.20	0.002	0.008
L	12.00 BSC		0.472 BSC	
M	12.00 BSC		0.472 BSC	
N	0.20 REF		0.008 REF	
P	0°	7°	0°	7°
R	0°	---	0°	---
S	---	1.70	---	0.067
V	12° REF		12° REF	
W	12° REF		12° REF	
AA	0.20	0.35	0.008	0.014
AB	0.07	0.16	0.003	0.006
AC	0.08	0.20	0.003	0.008
AD	4.58	4.78	0.180	0.188
AE	4.58	4.78	0.180	0.188



Notes

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