Data Sheet No. PD60219 rev C

International
IOR Rectifier

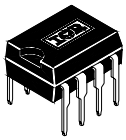
IR2161(S) & (PbF)

HALOGEN CONVERTOR CONTROL IC

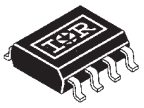
Features

- Intelligent half-bridge driver
- Auto Resetting Short Circuit Protection
- Auto Resetting Overload Protection
- Externally Triggerable Latching Shutdown
- Latching Overtemperature Protection
- Frequency Modulation "dither" (for lower EMI)
- Micropower Startup (<300 μA)
- Phase Cut dimmable for leading / trailing edge
- Output Voltage Shift Compensation.
- Real Softstart
- Adaptive Dead Time
- Small 8 Pin DIP/SOIC Package
- Also available LEAD-FREE (PbF)

Packages



8-Lead PDIP
IR2161

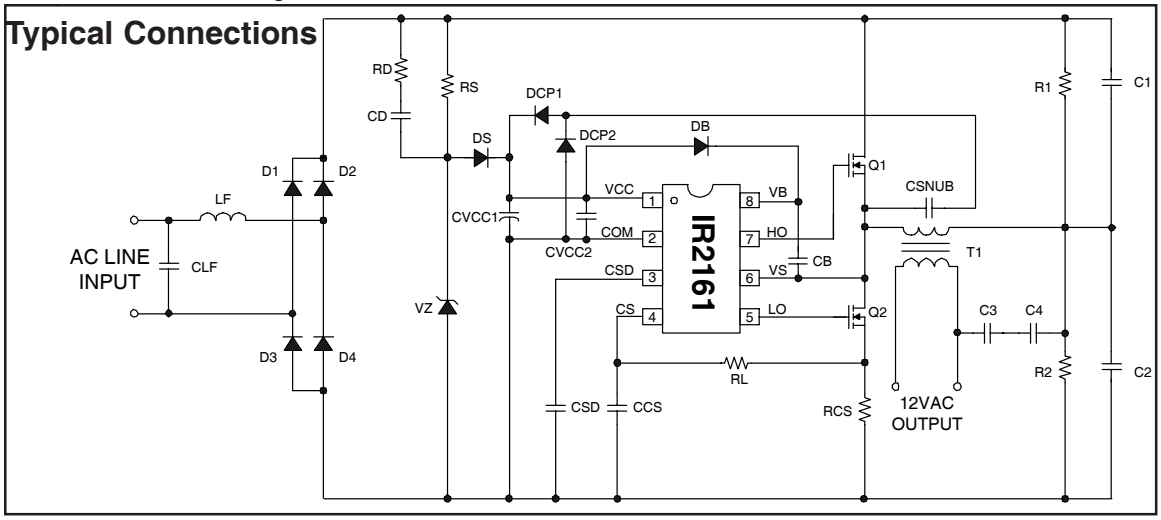


8-Lead SOIC
IR2161S

Description

The IR2161 is a dedicated Intelligent Half bridge Driver IC for a Halogen convertor (electronic transformer). It includes all necessary protection features and also allows the Convertor to be dimmed externally with a standard phase cut dimmer with both leading or trailing edge types. This IC provides the advantage of reduced thermal stress in the lamp due to softstart. There is also compensation of the output voltage for load regulation. It enables the convertor to operate with extremely low harmonic distortion over the full range of loads. The IR2161 includes adaptive deadtime to allow cool running MOSFETs and improves the EMI behaviour due to frequency modulation (dither). All the features are integrated in a small 8 pin DIP/SOIC package to allow for a size reduction in the next generation of convertors.

Typical Connections



Note: Throughout this data sheet "convertor" is spelled in accordance with standard IEC 61047 "DC or AC supplied convertors for filament lamps – Performance requirements".

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
IO_{MAX}	Maximum allowable output current (HO,LO) due to external power transistor miller effect		-500	500	mA
V_{CSDMAX}	CSD pin voltage		-0.3	V_{CC} + 0.3	V
V_{CS}	Current sense pin voltage		-0.3	V_{CC} + 0.3	
I_{CS}	Current sense pin current		-5	5	mA
I_{CC}	Supply current (Note 1)		-20	20	
dV/dt	Allowable offset voltage slew rate		-50	50	V/ns
P_D	Maximum power dissipation @ $T_A \leq +25°C$	(8 Lead DIP)	—	1	W
	$PD = (T_{JMAX}-T_A)/Rth_{JA}$	(8 Lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 Lead DIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
T_J	Junction temperature		-55	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{BS}	High side floating supply voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_{BSMIN}	Minimum required VBS voltage for proper HO functionality	4.3	—	
V_S	Steady state high-side floating supply offset voltage	-1	600	
V_{CC}	Supply voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	Supply current	(Note 2)	10	mA
C_{SD}	CSD pin external capacitor	47	—	nF
I_{CS}	Current sense pin current	-1	1	mA
T_J	Junction temperature	-25	125	°C

Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Note 2: Enough current should be supplied into the V_{CC} pin to keep the internal 15.6V zener clamp diode on this pin regulating its voltage, V_{CLAMP}.

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 14V, +/- 0.25V, VCSD = 5.0V, C_{LO} =C_{HO} = 1000 pF, and T_A = 25°C unless otherwise specified.

Supply Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	11.5	12.1	12.7	V	V_{CC} rising from 0V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	10	10.5	11		V_{CC} falling from 14V
V_{CCUVL-}	V_{CC} supply softstart reset negative going threshold	—	—	5.5		V_{CC} - V_{CCUV-} (-2V)
I_{QCCUV}	UVLO mode quiescent current	—	250	300	µA	V_{CC} = 11V
I_{CCFLT}	Fault-mode quiescent current	—	1.4	2.0	mA	CS=8V, VCSD=0V
I_{CCLF}	VCC current (low frequency)	—	2.0	3.0		VCC=14V,VCSD=5.2V
I_{CCHF}	VCC current (high frequency)	—	4.0	7.0		VCC=14V,VCSD=0V
V_{CLAMP}	V_{CC} zener clamp voltage	14.5	15.4	16.5	V	I_{CC} = 5mA

Floating Supply Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSMIN}	Minimum V_{BS} to start oscillation at HO	3.0	3.6	4.3	V	
I_{BSHF}	V_{BS} high frequency supply current	—	3.0	—	mA	VCC=14V,VBS=14V, VCSD=0V
I_{BSLF}	V_{BS} low frequency supply current	—	0.8	—		VCC=14V,VBS=14V, VCSD=5.2V
I_{LEAK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V

Voltage Compensation Characteristics (Run Mode)

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{CSD\ (min)}$	Min CSD voltage (in Run Mode)	—	0	—	V	VCS = 0V
$V_{CSD\ (max)}$	Max CSD voltage (in Run Mode)	—	5.5	—	V	VCS = 0.4V

Electrical Characteristics (cont'd)

V_{CC} = V_{BS} = V_{BIAS} = 14V, +/- 0.25V, VCSD = 5.0V, C_{LO} = C_{HO} = 1000 pF, and T_A = 25°C unless otherwise specified.

Shutdown Circuit Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CSOL}	Overload threshold (CS PID)	0.47	0.56	0.64	V	
V_{CSSC}	CSD short circuit threshold (CS PID)	1	1.2	1.4		
I_{OL}	CSD overload charging current	6	9	12	uA	VCS=0.8V,VCSD=7V
I_{SC}	CSD short circuit charging current	75	100	120		VCS=1.5V,VCSD=7V
I_{RESET}	CSD shutdown reset current	0.1	0.7	—		VCSD=14V
$V_{CSLATCH}$	Latched shutdown threshold	—	9	—	V	
$T_{CSLATCH}$	Latched shutdown delay		1		µsec	VCS>VCSLATCH
V_{CSDOL}	Begin fault timing	—	5	—	V	VCS>VCSOL
V_{CSDSD}	Positive going threshold for oscillator shutdown	—	12	—		VCS > VCSOL
V_{CSDRS}	Negative going threshold for oscillator restart	—	2.4	—		

Thermal Shutdown Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
T_{SD}	Latched over temperature limit	—	135	—	°C	

Oscillator Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$f_{(min)}$	Minimum oscillator frequency	—	34	—	kHz	VCSD = 5.3V
$f_{(max)}$	Maximum oscillator frequency in RUN mode	—	70	—		VCSD = 0V
D	Oscillator duty cycle	—	50	—	%	
$DTLO_{(max)}$	Maximum LO output deadtime (run mode default)	—	1.0		µsec	no reset from ADT
$DT_{HO(max)}$	Maximum HO output deadtime (run mode default)	—	1.0			

Adaptive Dead-Time System Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$DT_{LO(min)}$	Minimum LO output deadtime	—	700	—	nsec	Minimum propagation delay from ADT to output drivers
$DT_{HO(min)}$	Minimum HO output deadtime	—	700	—		

Electrical Characteristics (cont.)

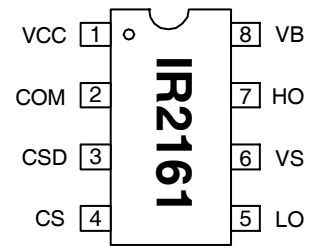
V_{CC} = V_{BS} = V_{BIAS} = 14V, +/- 0.25V, VCSD = 5.0V, C_{LO} =C_{HO} = 1000 pF, and T_A = 25°C unless otherwise specified.

Soft Start Characteristics						
Symbol	**Definition**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
I_{SS}	Soft start CSD charge current	—	0.5	—	mA	
f_{SS}	Soft start frequency	—	115	—	kHz	VCC>VCCUV+
Gate Driver Output Characteristics						
Symbol	**Definition**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
$V_{LO=LOW}$	LO voltage when LO is low	—	COM	—		
$V_{HO=LOW}$	HO voltage when HO is low	—	COM	—		
$V_{LO=HIGH}$	LO voltage when LO is high	—	VCC	—		
$V_{HO=HIGH}$	HO voltage when HO is high	—	VCC	—		
t_{RISE}	Turn-on rise time	—	110	250	ns	C_{HO}=C_{LO}=1nF
t_{FALL}	Turn-off fall time	—	60	140		
IO+	HO, LO source current	—	200	—	mA	
IO-	HO, LO sink current	—	300	—		

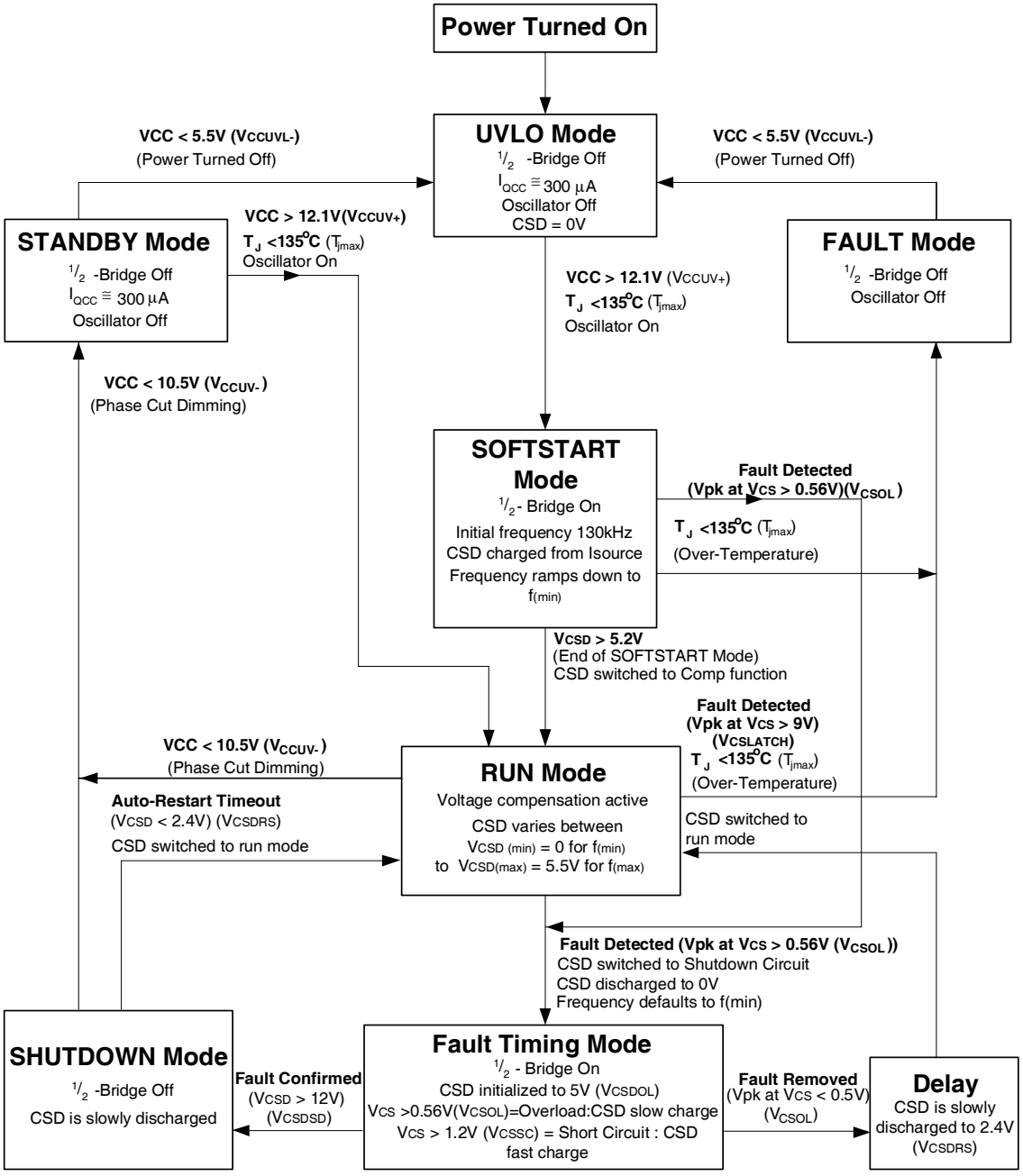
Lead Definitions

Symbol	Description
V_{CC}	Supply voltage
COM	IC power and signal ground
CSD	Shutdown timing and compensation capacitor
CS	Current sensing input
LO	Low-side gate driver output
V_S	High-side floating return
HO	High side gate driver output
V_B	High side gate driver floating supply

Lead Assignments



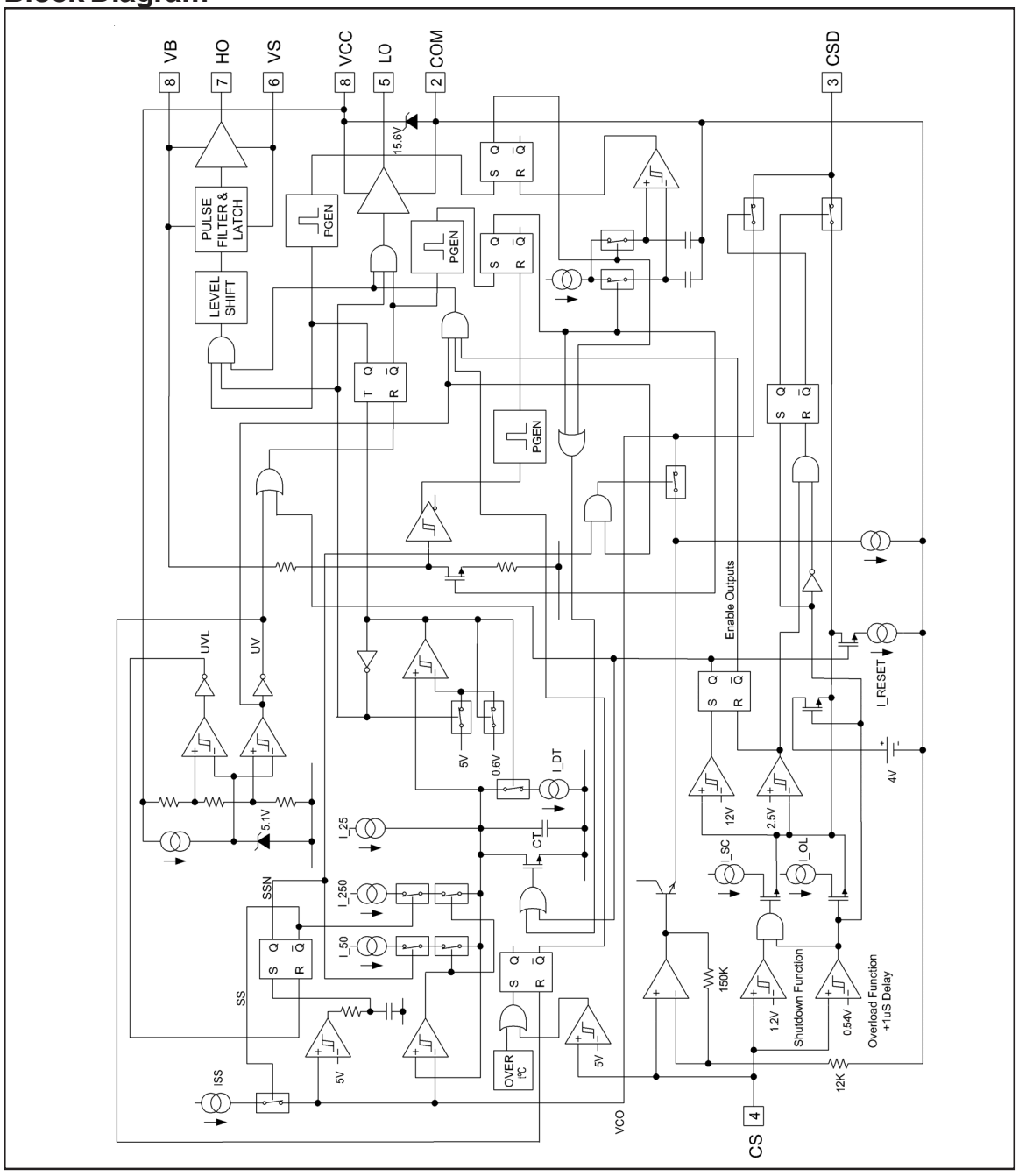
* Recommended value for CSD is 100nF (all performance data relates to this value)
NOTE: The recommended value for RL is 1K Ohm and CCS is 1nF.



All values are typical

NOTE: If the IR2161 die temperature exceeds 135° at any time the system will enter FAULT Mode. At a typical frequency of 40kHz, the die temperature is approximately 12°C above the ambient air temperature

Block Diagram



Halogen Convertor Controller Functional Description

Under-voltage Lock-Out Mode (UVLO)

The under-voltage lockout mode (UVLO) is defined as the state the IC is in when VCC is below the turn-on threshold. To identify the different modes of operation, refer to the State Diagram shown on page 7 of this data sheet. The IR2161 under voltage lock-out is designed to maintain an ultra low supply current of less than 300uA, and to guarantee the IC is fully functional before the high and low side output drivers are activated. Figure 1 shows a simple VCC supply arrangement that will work effectively, also when the convertor is being dimmed from a conventional triac based wall dimmer

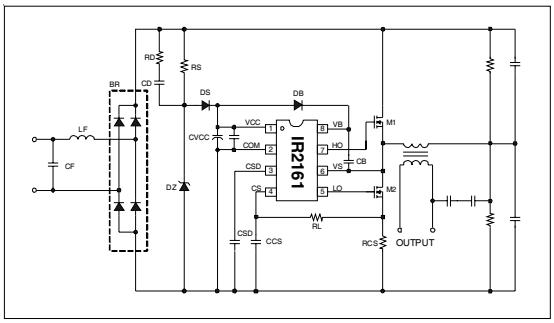


Figure 1, Halogen Convertor.

The start-up capacitor (C_{VCC}) is charged by current through supply resistor (RS) minus the start-up current drawn by the IC. This resistor is chosen to provide sufficient current to supply the IR2161 from the DC bus. In a Halogen convertor it is important to consider that the DC bus is completely unsmoothed and has a full wave rectified shape. C_{VCC} should be large enough to hold the voltage at Vcc above the UVLO threshold for one half cycle of the line voltage as it will only be charged at the peak. A charge pump consisting of two diodes (DCP1 and DCP2) connected to CSNUB is recommended to supply VCC as this allows RS to be a large value since it is only needed at startup. IF RS is required to supply the circuit without a charge pump it needs to be a relatively low value and consequently dissipates 1 to 2W, which is undesirable.

An external 16V zener diode DZ has been added to avoid the need for the internal zener to dissipate power (it should be rated at 1.3W). The resistor RD in series with CD is necessary if the convertor is required to operate from a triac based (leading edge) phase cut dimmer. When the triac fires at a point during the mains half-cycle the high dv/dt allows a large current to flow through this path to instantly charge C_{VCC} to the maximum Vcc voltage.

The external zener (DZ) will prevent possible damage to the IC by shunting excess current to COM.

Once the capacitor voltage on VCC reaches the start-up threshold the IC turns on and HO and LO begin to oscillate.

The supply resistor (RS) and RD/CD must be selected such that enough supply current is available over all ballast operating conditions. A bootstrap diode (DB) and supply capacitor (CB) comprise the supply voltage for the high side driver circuitry. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin. During under voltage lock-out mode, the high and low-side driver outputs HO and LO are both low.

Soft Start Mode

The soft start mode is defined as the state the IC is in at system switch on when the lamp filament is cold. As with any type of filament lamp, the Dichroic Halogen lamp has a positive temperature coefficient of resistance such that the cold resistance (at switch on when the lamp has been off long enough to cool) is much lower than the hot resistance when the lamp is running. This normally results in a high inrush current occurring at switch on. Under worst-case conditions this could potentially trigger the convertor's shut down circuit. To overcome this problem the IR2161 incorporates the soft start function.

When the IC starts oscillating the frequency is initially very high (about 130kHz). This causes the output voltage of the convertor to be lower since the HF transformer in the system has a fixed primary leakage inductance that will present a higher impedance at higher frequency and thus allowing less AC voltage to appear across the primary. The reduced output voltage will naturally result in a reduced current in the lamp which eases the inrush current thus avoiding tripping of the shutdown circuit and will ease the stress on the lamp filament as well as reducing the current in the half bridge MOSFETs (M1 and M2).

The frequency sweeps down gradually from 130kHz to the

minimum frequency over a period of around 1s (assuming CSD=100nF). During this time the external capacitor at the CSD pin charges from 0V to 5V, controlling the oscillator frequency through the internal voltage controlled oscillator (VCO). The value of CSD will determine the duration of the soft start sweep. However, since it also governs the shut down circuit delays, the value should be kept at 100nF to achieve the datasheet operation.

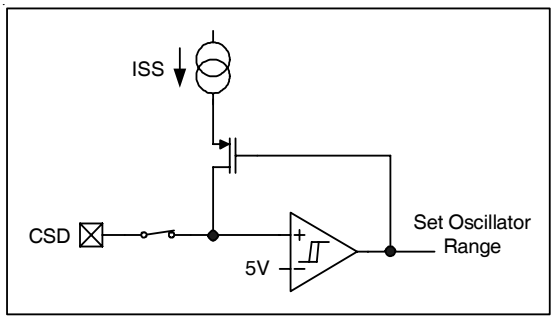


Figure 2, Halogen Convertor.

It can be seen from Figure 2, that at switch on, the CSD capacitor is internally switched to the soft start circuit input. A current source charges CSD linearly to 5V over a period of 0.5s at which time the comparator output goes high. The PMOS switch opens and the ISS current source is disconnected from CSD. The comparator latches high at this point and this causes the oscillator range to change and the CSD capacitor to be disconnected from the soft start circuit and connected to the voltage compensation circuit. The latching comparator has a built in delay of at least 20uS in order to prevent false triggering caused by transients.

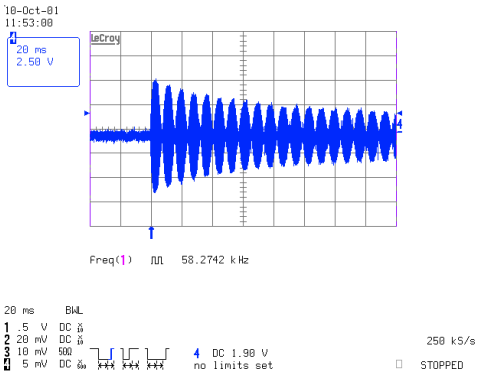


Figure 3, Typical Cold Lamp Inrush Current.

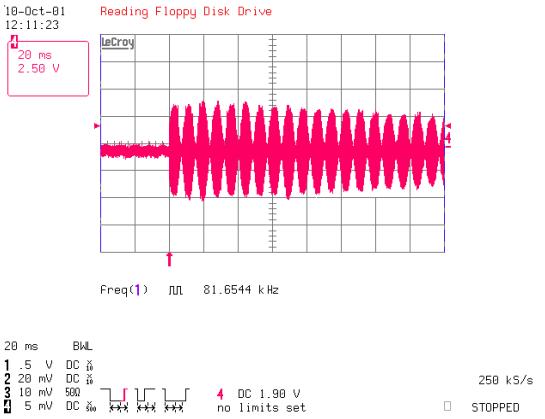


Figure 4, Cold Lamp Inrush Current with Soft Start.

Run Mode (Voltage Compensation)

When soft start is completed the system switches over to compensation mode. This function provides some regulation of the output voltage of the convertor from minimum to maximum load. In this type of system it is desirable that the voltage supplied to the lamp does not exceed a particular limit. If the lamp voltage becomes too high the temperature of the filament runs too high and the life of the lamp is significantly reduced. The problem is that the output transformer is never perfectly coupled so there will always be a degree of load regulation.

The transformer has to be designed such that the lamp voltage at maximum load is sufficiently high to ensure adequate light output.

At minimum load the voltage will consequently be higher and is likely to exceed the maximum desired lamp voltage.

In the widely used self-oscillating system based around bipolar power transistors, there is some frequency change (increasing the frequency reduces the output voltage) depending on the load that helps to compensate for this, although this is non-linear and depends on many parameters in the circuit and so is not easy to predict.

The IR2161 based system includes a function that monitors the load current through the current sense resistor (RCS). The peak current is detected and amplified within the IC then appears at the CSD pin during run mode. The voltage

across the CSD capacitor will vary from 0V if there is no load to approximately 5V at maximum load.

This is provided that the correct value of current sense resistor has been selected for the maximum rated load and line voltage supply of the convertor. This should be 0.33 Ohm (0.5W) for a 100W system running from a 220-240V AC line. (It should be noted that the RCS resistor value is also critical for setting the limits for the shut down circuit)

In RUN mode the oscillator frequency will vary from approximately 34kHz when VCSD is 5V (maximum load) to 70kHz when VCSD is 0V (no load). The result of this is that if a lighter load, such as a single 35W lamp, is connected to a 100W convertor, the frequency will shift upwards so that the output voltage falls below the maximum that is desirable for the lamp. This provides sufficient compensation for the load to ensure that the lamp voltage will always be within acceptable limits but does not require a complicated regulation scheme involving feedback from the output.

An additional internal current source has been included to discharge the external capacitor. This will provide approximately 10% ripple at twice the line frequency if CSD is 100nF.

The advantage of this is that during the line voltage half cycle the oscillator frequency will vary by several kHz thus spreading the EMI conducted and radiated emissions over a range of frequencies and avoiding high amplitude peaks at particular frequencies. In this way the filter components used may be similar to those used in a common bipolar self-oscillating system.

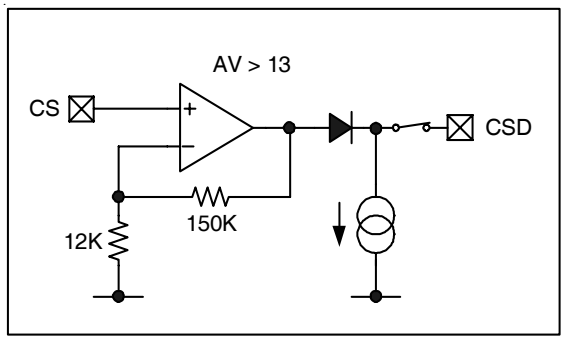


Figure 5, Voltage Compensation Circuit

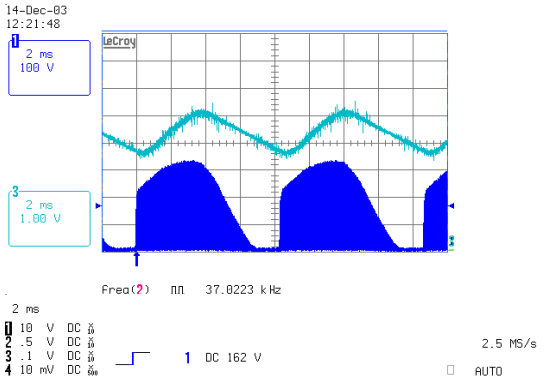


Figure 6, VS voltage and CSD voltage.

In the above trace it can be seen that a leading edge phase cut (triac) dimmer is connected at close to maximum brightness. There is a short delay at the beginning of each half cycle before the AC line voltage is switched to the convertor. Dimming increases the ripple in the CSD voltage and gives more modulation. This is an inherent effect that causes no system problems.

The startup sequence of the CSD pin can be seen from the point where VCC increases above the UVLO+ threshold.

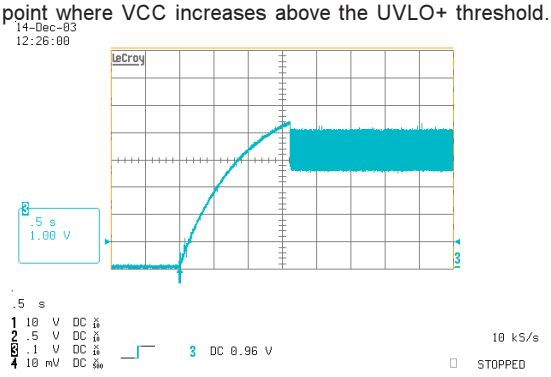


Figure 7, Startup sequence of CSD.

This trace shows that after the CSD voltage has ramped up through soft start, the system switches over to voltage compensation mode and a ripple exists which allows the frequency modulation (or “dither”) to occur. In this case the

convertor is close to maximum load. If the load is reduced, the average level at which the ripple occurs (i.e. the DC component) will be at a lower level.

Shut Down Circuit

The IR2161 contains a dual mode auto-resetting shutdown circuit that detects both a short circuit or overload condition in the convertor. The load current detected at the CS pin is used to sense these conditions. If the output of the convertor is short-circuited, a very high current will flow in the half bridge and the system must shut down within a few mains half cycles, otherwise the MOSFETs will rapidly be destroyed due to excessive junction temperature. The internal CS pin has an internal threshold (V_{CSSC}). There also exists a lower threshold so that if the voltage exceeds this level for more than 50mS, the system will shut down.

A delay is included to prevent false tripping either due to lamp inrush current at switch on (this current is still higher than normal with the soft start operation) or transient currents that may occur if an external triac based phase cut dimmer is being used.

There also exists a lower threshold (V_{CSOL}), which has a much longer delay before it shuts down the system. This provides the overload protection if an excessive number of lamps is connected to the output or the output is short-circuited at the end of a length of cable that has sufficient resistance to prevent the current from being large enough to trip the short circuit protection. Also under this condition there is an excessive current in the half bridge that is sufficient to cause heating and eventual failure but over a longer period of time. The threshold for overload shutdown is approximately 50% above maximum load with a delay of approximately 0.5s. These timings are based on a current waveform that has a sinusoidal envelope and a high frequency square wave component with 50% duty cycle.

Both shutdown modes are auto resetting, which allows the oscillator to start again approximately 1.5s after shutting down. This is so that if the fault condition is removed the system can start operating normally again without the line voltage having to be switched off and back on again. It also provides a good indication of overload to the end user as all the lamps connected to the system will flash on and off continuously if too many are connected.

The shut down circuit also uses the external CSD capacitor for it's timing functions. When the 0.5V threshold (V_{CSOL}) is exceeded at CS the CSD is internally disconnected from the voltage compensation circuit and connected to the shutdown circuit.

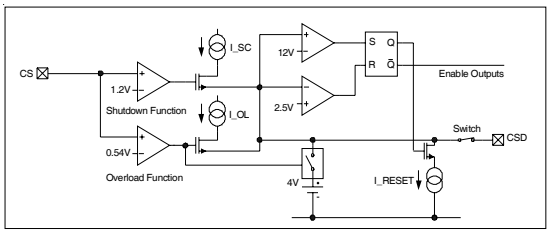


Figure 8, Shut Down Circuit.

The oscillator operates at minimum frequency when the CSD capacitor is required for shutdown circuit timing.

During soft start or run mode, if the 0.5V threshold (V_{CSOL}) is exceeded the IR2161 charges CSD rapidly to approximately 5V (V_{CSDOL}).

When the voltage at the CS input is greater than 0.5V, the CSD capacitor is charged by current source I_{OL} and when the short circuit threshold of 1.2V is exceeded it is charged by I_{SC} as well. If 1.2V is exceeded CSD will charge from 5V (V_{CSDOL}) to 12V (V_{CSDSD}), in approximately 50ms. When 0.5V is exceeded but 1.2V is not, CSD charges from 5V (V_{CSDOL}) to 12V (V_{CSDSD}) in approximately 0.5s. It should be remembered that, the timing accounts for the fact that high frequency pulses with approximately 50% duty cycle and a sinusoidal envelope appear at the CS pin.

The values of I_{SC} and I_{OL} take into account that only at the peak of the mains will the comparator outputs go high and effectively the capacitor will be charged in steps each line half cycle. Once VCSD reaches 12V (V_{CSDSD}), VCSD discharges down to 2.4V (V_{CSDRS}) and the system starts up again. If the fault mode is still present, CSD starts charging again.

If a fault is detected but goes away before CSD reaches 12V (V_{CSDSD}), then CSD will discharge to 2.4V (V_{CSDRS}) and then the system will revert to compensation mode without interruption of the output.

Following a shutdown, when the system starts up again after the delay, the CSD capacitor will be internally switched back to the voltage compensation circuit. However, if the fault is still present the system will switch CSD back to the shutdown circuit again.

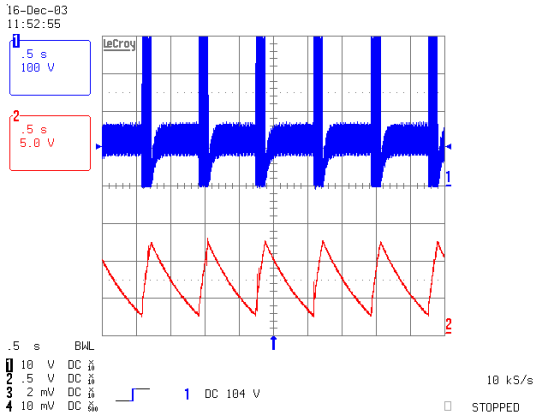


Figure 9, Short Circuit Output Current.

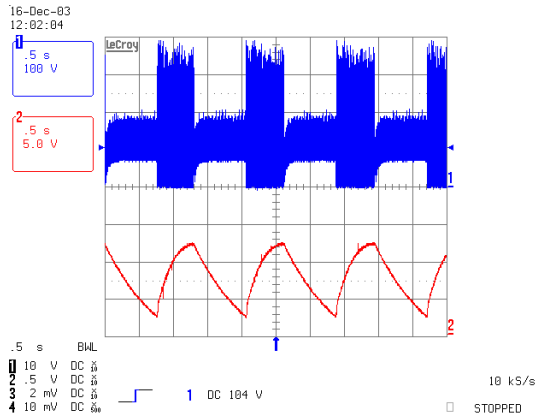


Figure 10, Overload Output Current.

In figures 9 and 10, trace (1) shows the half bridge oscillations during both types of fault mode and trace (2) shows the charging and discharging of the CSD capacitor.

The IR2161 can also be externally shut off by applying a voltage above 9V (VCSLATCH) to the CS pin. This will cause the system to go directly to a latched fault mode, after a delay of approximately 1uS to avoid the possibility of false tripping caused by transients. To restart the system, it is necessary to cycle Vcc off and on.

In addition, any time Vcs exceeds VCSLATCH (approximately half Vcc), this latching shutdown function will be triggered and the system will remain in FAULT mode until VCC is re-cycled.

The IR2161 also includes over temperature shutdown, which latches the convertor off when the die temperature of the IC exceeds 130-135°C. Experimental measurements reveal that the die temperature will be no more than 20°C above the ambient temperature at all operating frequencies inside the convertor.

Calculating Rcs

The value of the current sense resistor Rcs is critical to achieve correct operation in the IR2161 based Halogen convertor.

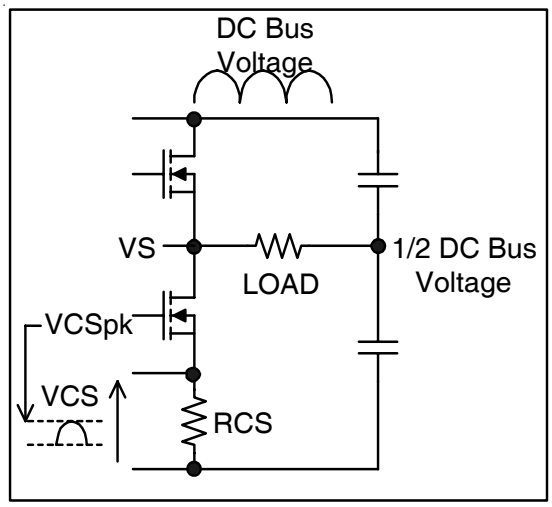


Figure 11, Calculating RCS

Ignoring the output transformer we can assume for this calculation that the load is connected from the half bridge to the mid point of the two output capacitors and that the voltage at this point will be half the DC bus voltage. The RMS voltage of the DC bus is the same as that of the AC line so we can see that the RMS voltage across the load shown in Figure 8, will be half the RMS voltage of the line. The load is the maximum rated load of the convertor. The current in Rcs will be half the load current given by :

$$I_{CS(RMS)} = \frac{P_{LOAD}}{V_{AC}}$$

Since the load is resistive the current waveform will have a sinusoidal envelope and so the peak can be easily determined taking into account that the current has a high frequency component with an approximate 50% duty cycle:

$$I_{CS(PK)} = 2\sqrt{2} \times I_{CS(RMS)}$$

Therefore:

$$V_{CS(PK)} = I_{CS(PK)} \times R_{CS}$$

For correct operation at maximum load the peak voltage should be 0.4V.

The calculation can be simplified by combining the formulae,

$$R_{CS} = \frac{0.4 \cdot V_{CS}}{2 \cdot \sqrt{2} \cdot P_{LOAD}}$$

Which can be simplified to:

$$R_{CS} = 0.141 \cdot \frac{V_{AC}}{P_{LOAD}}$$

Example

For a 100W convertor working from a 230VAC supply the current sense resistor would need to be :

$$\frac{0.141 \times 230}{100} = 0.324\Omega$$

The nearest preferred value to this would be 0.33 Ohms.

The power dissipation in Rcs should also be considered and is given by :

$$P_{CS} = \left(\frac{P_{LOAD}}{V_{AC}} \right)^2 \times R_{CS}$$

In this case :

$$\left(\frac{100}{230} \right)^2 \times 0.33 = 0.062W$$

It is important to bear in mind that the resistor must be rated to handle this current in a high ambient temperature.

IMPORTANT NOTE

The filter resistor RL should be 1K, which is needed to protect the CS input from negative going transients. CCS should be 1nF and is also necessary to filter out switching transients that can impair the operation of the shutdown circuit.

Adaptive Dead Time

Because of the fact that the DC bus voltage varies during the mains half cycle, the dead time may need to vary in order to achieve soft switching. The IR2161 has an adaptive dead time circuit (ADT) that detects the point at which the voltage at the half bridge slews to 0V (COM) and sets the LO output high at this point. There is an internal sample and hold system that allows approximately the same delay to be used to set HO high after LO has gone low. This reacts on a cycle-by-cycle basis of the oscillator and therefore will adjust the dead time as necessary regardless of external conditions.

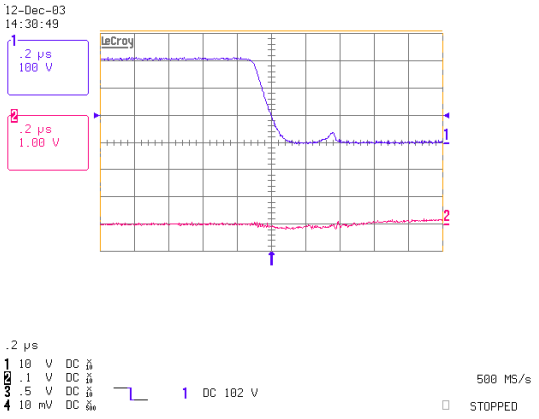


Figure 12, ADT when VS slews from VBUS to COM

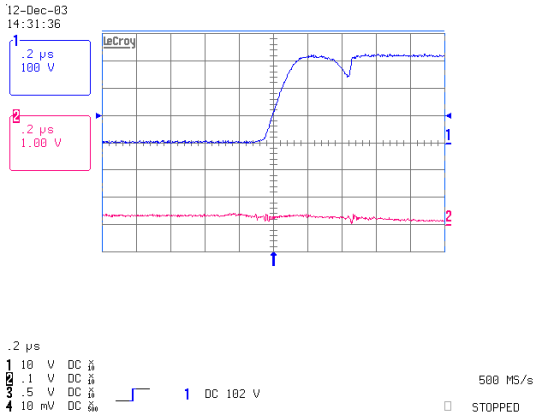


Figure 12, ADT when VS slews from COM to VBUS

The above waveforms are typical, showing the operation of the ADT circuit in either direction. In this case the design could be optimized further by increasing the snubber capacitor to slightly increase the slew time, in order to account for the propagation delays in the system. Alternatively an output transformer with a greater leakage inductance can extend the period before the VS voltage turns around and starts to go back the other way again.

The designer does not need to take into account parasitic capacitances in the MOSFETs or leakage inductance in the output transformer and fix the dead time accordingly.

The system can operate reliably down to dead times in the order of 300nS, which should be low enough to accommodate the output transformer leakage inductance and parasitic MOSFET capacitances of a practical Halogen convertor.

The slew rate can easily be increased, if necessary, by adding a small snubber capacitor across the primary of the transformer if necessary. However, should the snubber capacitor be too large, it will prevent the VS voltage from slewing all the way to the opposite rail. Consequently the ADT function will be unable to operate, causing the IR2161 to revert to the default dead time of 1µS. Snubber capacitors would normally be in the order of hundreds of pF.

When designing a halogen convertor it is desirable to optimize the system at maximum load, where the conduction losses of the power MOSFETs in the half-bridge will be at a maximum. At lighter loads there may be hard switching if the VS voltage is unable to slew all the way or it slews so rapidly that the voltage begins to turn around again before the IR2161 is able to switch on the relevant MOSFET in the half bridge.

Such a situation is not desirable but may be acceptable at lighter loads where the conduction losses are small.

With correct optimization of the output transformer and surrounding circuit it is possible to achieve a design that will not hard switch from 20% to 100% of the maximum rated load of the system.

This system avoids the need for an external resistor to program the dead time and contributes to the multi functional nature of the CSD pin to the IR2161 being realized with only 8 external pins

In any design when there is no load at the output, the VS voltage will not slew and obviously the ADT circuit is not able to function in this condition. In this case the dead time will default to approximately 1µS, the maximum allowed by the IC and there will be hard switching.

Although this will inevitably lead to some switching losses, there are no conduction losses so the temperature rise of the half bridge MOSFETs should not create a problem in this case.

Dimming

Almost any Halogen convertor available can be dimmed by an external *phase cut* dimmer that operates in *trailing edge* mode. This means that at the beginning of the line voltage half cycle, the switch inside the dimmer is *closed* and mains voltage is supplied to the convertor allowing the convertor to operate normally. At some point during the half cycle, the switch inside the dimmer is *opened* and voltage is no longer applied. The DC bus inside the convertor almost immediately drops to 0V and the output is no longer present. In this way bursts of high frequency output voltage are applied to the lamp. The RMS voltage across the lamp will naturally vary depending on the phase angle at which the dimmer switch switches off. In this way the lamp brightness may easily be varied from zero to maximum output.

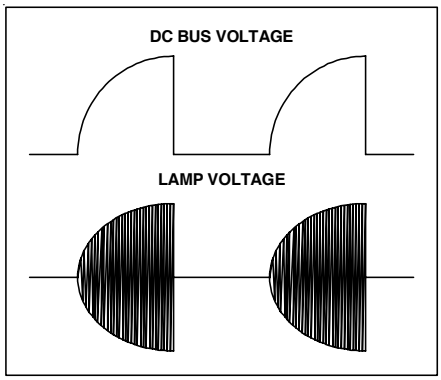


Figure 13, Trailing Edge Dimming

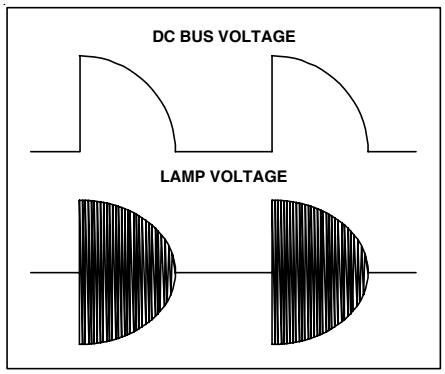


Figure 14, Leading Edge Dimming

Trailing edge dimmers are less common however than leading edge dimmers. This is because they are more expensive to make and need to incorporate a pair of MOSFETs or IGBTs whereas a leading edge dimmer is based around a single *triac*.

Conversely many Halogen convertors are not able to operate with leading edge dimmers because of the fact that they are based around a triac. It is possible, however, to design a Halogen convertor that will work effectively with a triac based dimmer by designing the input filter components correctly ensuring that at the *firing* point of the triac the oscillator can start up rapidly. In the IR2161 based system this is easy to achieve through the addition of RD and CD, which conduct a large current to VCC due to the high dv/dt that occurs when the triac fires. At the same time, the bus voltage rises rapidly from zero to the AC line voltage. If the VCC voltage falls below V_{CCUV-} during the time when the triac in the dimmer is off, the soft start will not be initiated because the soft start circuit is not reset until VCC drops approxmately 2V below V_{CCUV-}. This takes some time as the VCC capacitor discharges very slowly during UVLO micro-power operation. The intermediate period is referred to as Standby mode.

During dimming the voltage compensation circuit will cause a frequency shift upward at angles above 90° because the peak voltage at CS will be reduced (see figure 14). This will result in a reduction of voltage at CSD and thus an increase in frequency. However this will not have a noticeable effect on the light output.

The problem associated with operation of Halogen convertors with triac dimmers is due to the fact that after a triac has been fired it will conduct until the current falls below its *holding current*. If the load is purely resistive (as in a filament lamp directly connected to the dimmer) this will naturally happen at the end of the line voltage half cycle as the current has to fall to zero. In a Halogen convertor it is necessary to place a capacitor and inductor at the AC input to comply with regulations regarding EMI *conducted emissions*. This means that when the line voltage falls to zero there could still be some current flowing that is enough to keep the triac switched on and so the next cycle will follow through and not be *phase cut* as required. This can happen intermittently resulting in flickering of the lamps. The way to avoid the problem is to ensure that the product has the smallest possible filter capacitor CCS and to state a minimum load for the convertor. This would be typically one third of the maximum load to avoid problems of this kind.

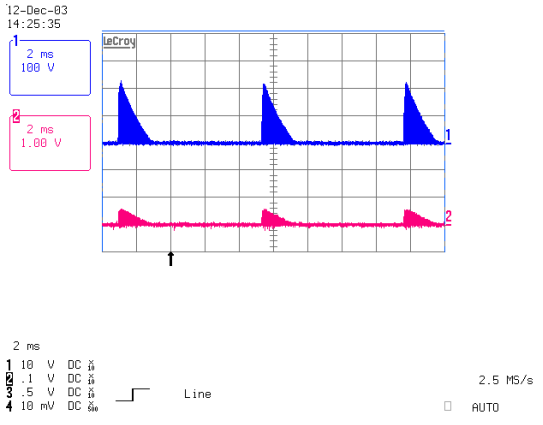
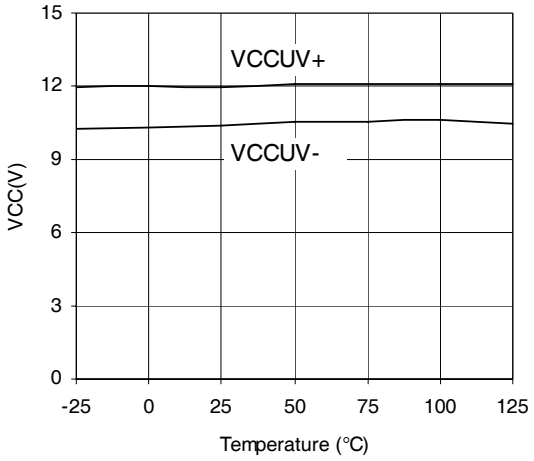
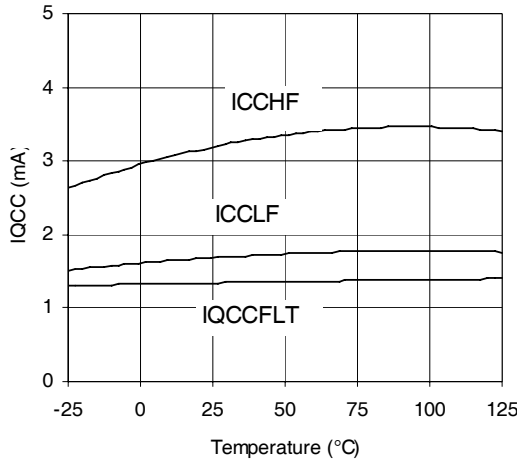


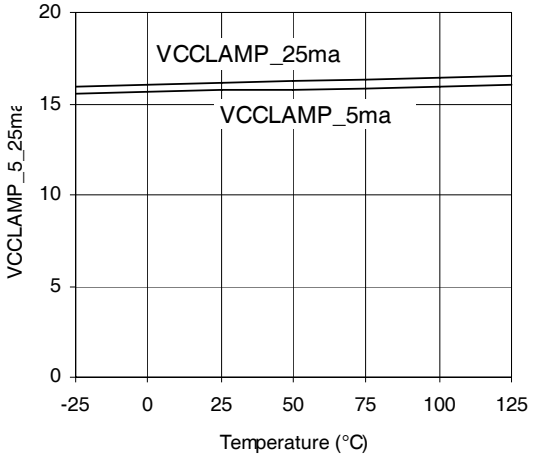
Figure 15, Half Bridge voltage and current during dimming



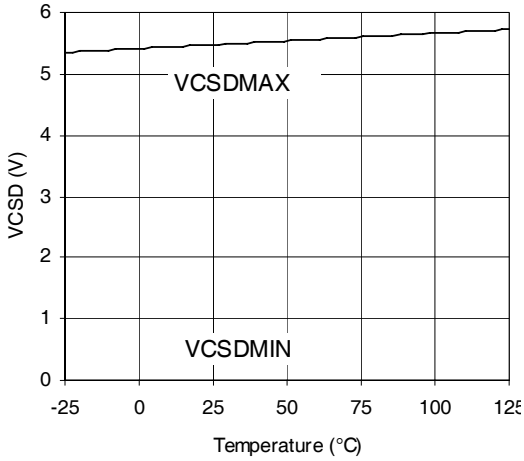
Graph : VCCUV+/- vs TEMP (IR2161)



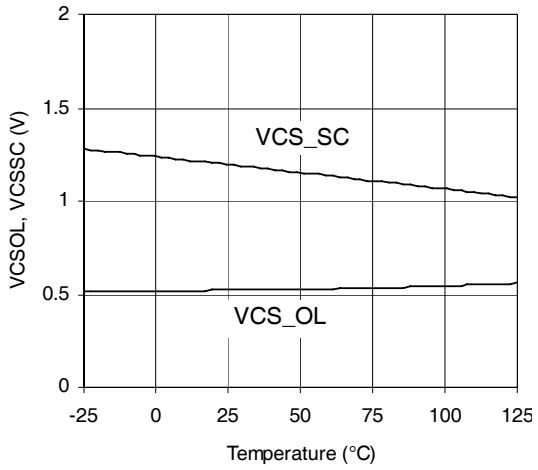
Graph : IQCC vs TEMP (IR2161)



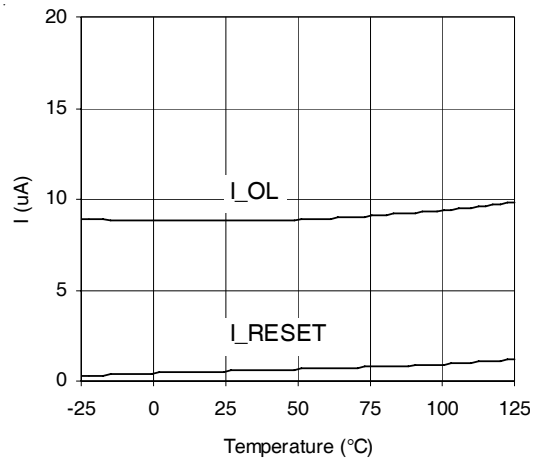
Graph : VCCLAMP_5_25ma vs TEMP (IR2161)



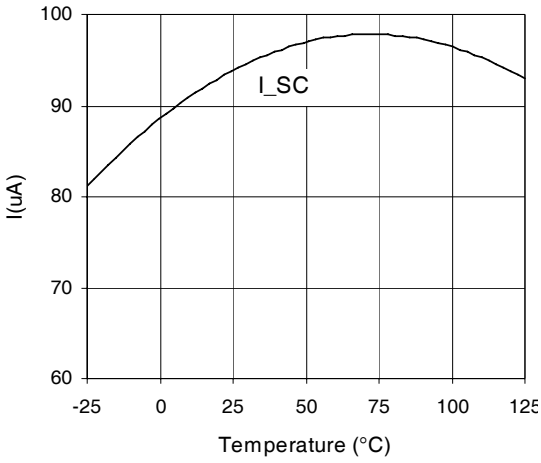
VCSDMIN,MAX vs TEMP (IR2161)



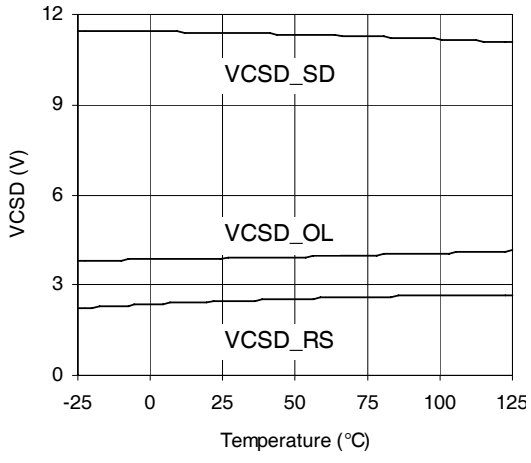
VCS_OL, VCS_SC vs TEMP (IR2161)



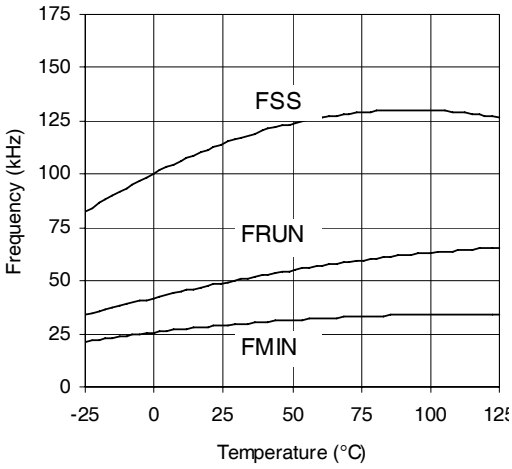
I_RESET, I_OL vs TEMP (IR2161)



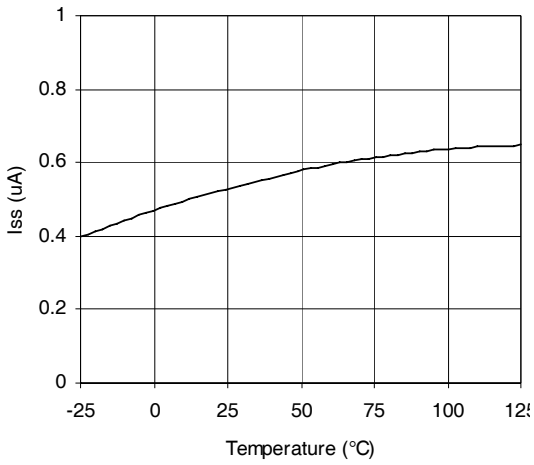
I_SC vs TEMP (IR2161)



Graph : VCSDSD,OL,RS vs TEMP (IR2161)

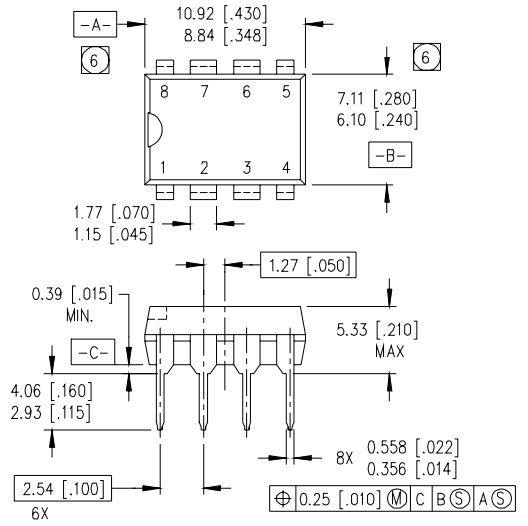


Frequency vs TEMP (IR2161)

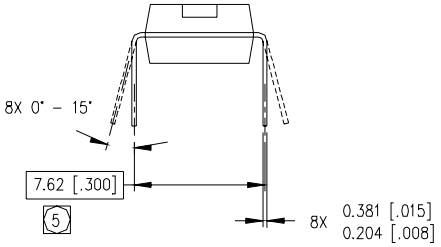


Graph : Iss (uA) vs TEMP (IR2161)

Case outlines

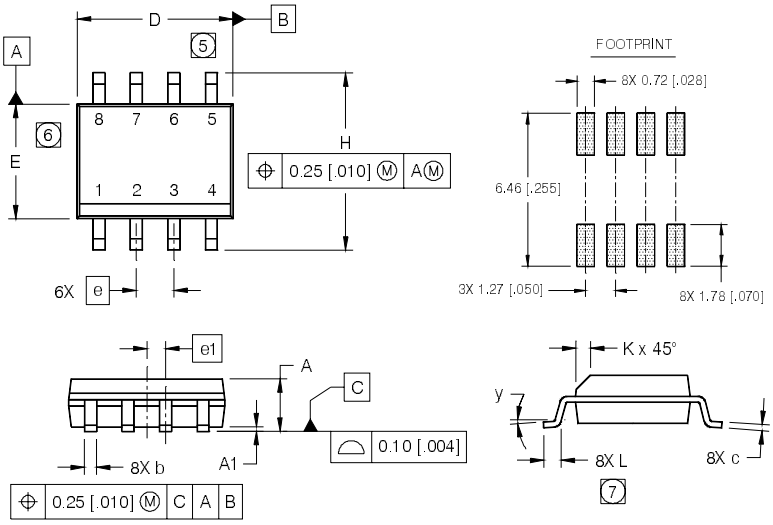


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



IR2161 8-Lead PDIP

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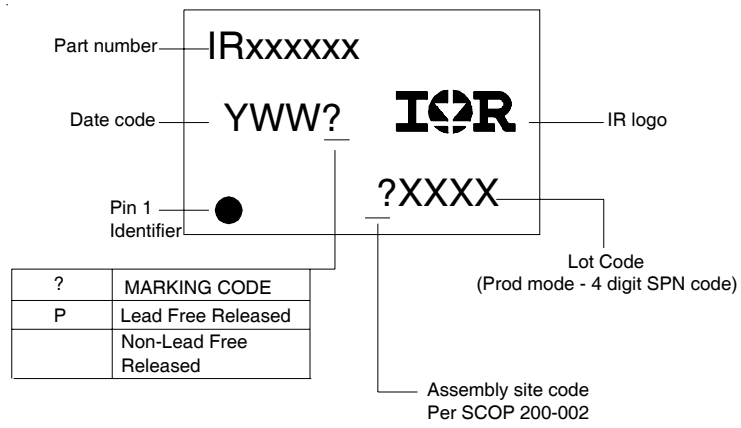
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	MIN	MAX	MIN	MAX
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A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

IR2161S 8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

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8-Lead PDIP IR2161 order IR2161
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Leadfree Part
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8-Lead SOIC IR2161S order IR2161SPbF

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