FAIRCHILD SEMICONDUCTOR™

January 1999

NMC27C16B
16,384-Bit (2048 x 8) CMOS EPROM

General Description

The NMC27C16B is a high performance 16K UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

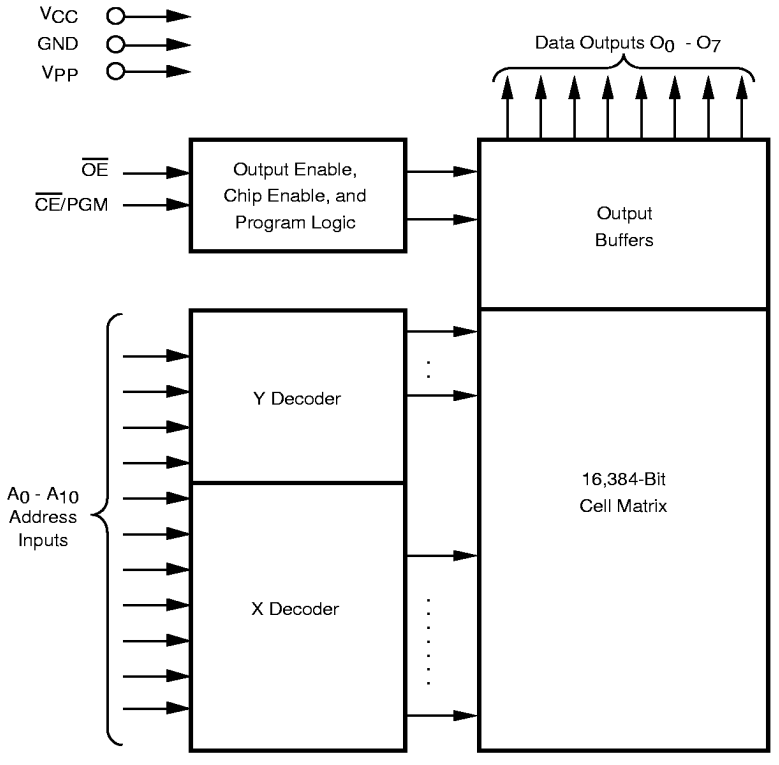
The NMC27C16B is packaged in a 24-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with Fairchild's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Low CMOS power consumption
  Active power: 55 mW max
  Standby power: 0.55 mW max
- Extended temperature range available, -40°C to +85°C
- Fast and reliable programming (100 µs for most bytes)
- TTL compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming equipment
- High current CMOS level output drivers
- Upgrade for NMOS 2716

Block Diagram



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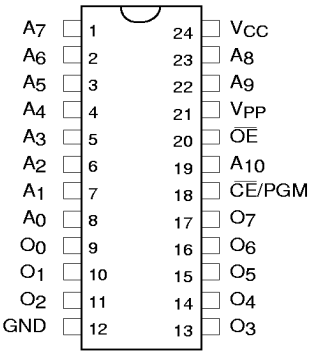
Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732
V_{PP}	V_{PP}	V_{PP}	
A_{12}	A_{12}	A_{12}	
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

NMC27C16B
Dual-in-line-package



27C32 2732	27C64 2764	27C128 27128	27C256 27256
	V_{CC} / PGM	V_{CC} / PGM	V_{CC}
			A_{14}
V_{CC}	NC	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C16B pins.

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Top View
Order Number NMC27C16BQ
See Package Number J24AQ

Pin Names

A0–A10	Addresses
$\overline{CE}/\overline{PGM}$	Chip Enable/Program
$\overline{OE}$	Output Enable
O0 –O7	Outputs
NC	No Connect

Commercial Temp. Range (0°C to 70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C16BQ150	150
NMC27C16BQ200	200

Extended Temp. Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C16BQE200	200

Absolute Maximum Ratings (Note 1)

Temperature Under Bias
- Commercial Parts: -10°C to +80°C
- Extended Temp. Parts: -40°C to +85°C

Storage Temperature: -65°C to +150°C

V_{CC} Supply with Respect to Ground: +7.0V to -0.6V

All Input Voltages except A9 with Respect to Ground (Note 10): +6.5V to -0.6V

All Output Voltages with Respect to Ground (Note 10): V_{CC} +1.0V to GND - 0.6V

V_{PP} Supply and A9 Voltage with Respect to Ground: +14.0V to -0.6V

Power Dissipation: 1.0W

Lead Temp. (Soldering, 10 sec.): 300°C

Operating Conditions (Note 8)

Temperature Range
- NMC27C16BQ150, 200: 0°C to +70°C
- NMC27C16BQE 200: -40°C to +85°C

V_{CC} Power Supply: +5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 11)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.1	1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$	0.1	1	µA	
I_{CC1} (Note 3)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f=5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		5	20	mA
I_{CC2} (Note 3)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	V_{PP} Load Current	V_{PP} = 5.5V			10	µA
V_{IL}	Input Low Voltage		-0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 mA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = -10 µA	V_{CC} - 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C16B				Units
			Q150		Q200, QE200		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{OE} = \overline{OE} = V_{IL}$	0		0		ns

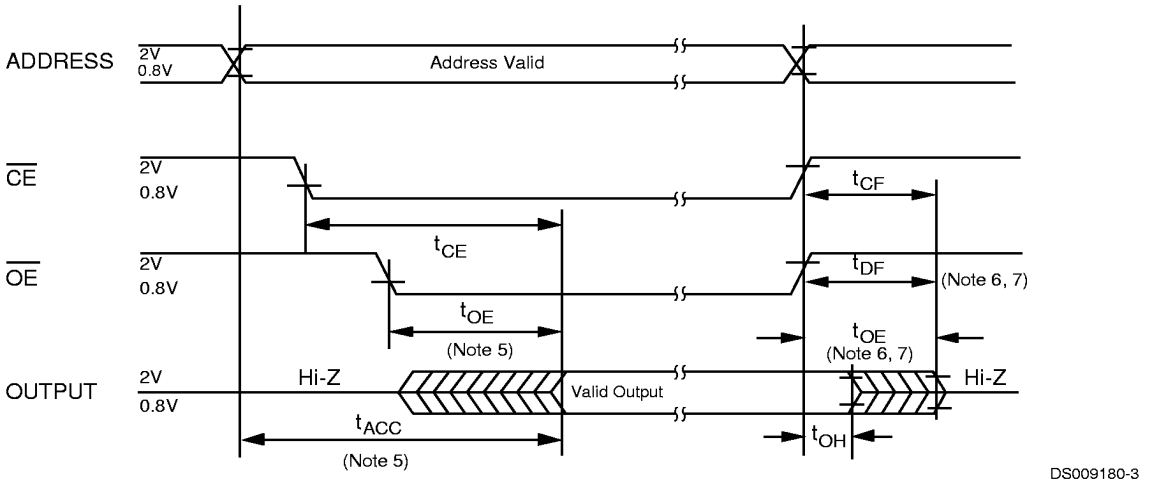
Capacitance T_A =+25°C, f = 1 MHz (Note 4)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Output Load (Note 12)	1 TTL Gate and C_L = 100 pF
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 2) (Note 9)



Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. I_{CC1} ≤ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: This parameter is only sampled and is not 100% tested.

Note 5: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 6: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 7: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 8: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 9: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns maximum.

Note 11: Typical values are for T_A = 25°C and nominal supply voltages.

Note 12: 1 TTL Gate: I_{DL} = 1.6 mA, I_{OH} = 400 µA.
C_L: 100 pF includes fixture capacitance

Programming Characteristics (Note 13) (Note 14) (Note 15) (Note 16)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/PGM = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IH}$ $\overline{OE} = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		3.0	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

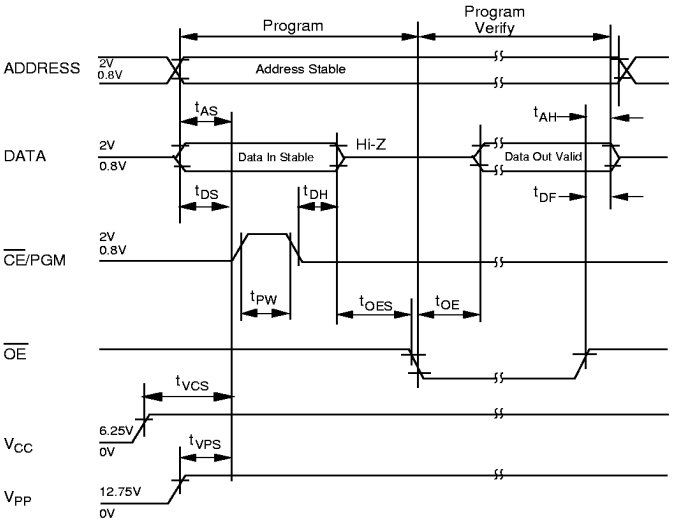
Note 13: Fairchild's standard product warranty applies only to devices programmed to specifications described herein.

Note 14: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 15: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 16: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Programming Waveforms



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Fast Programming Algorithm Flow Chart

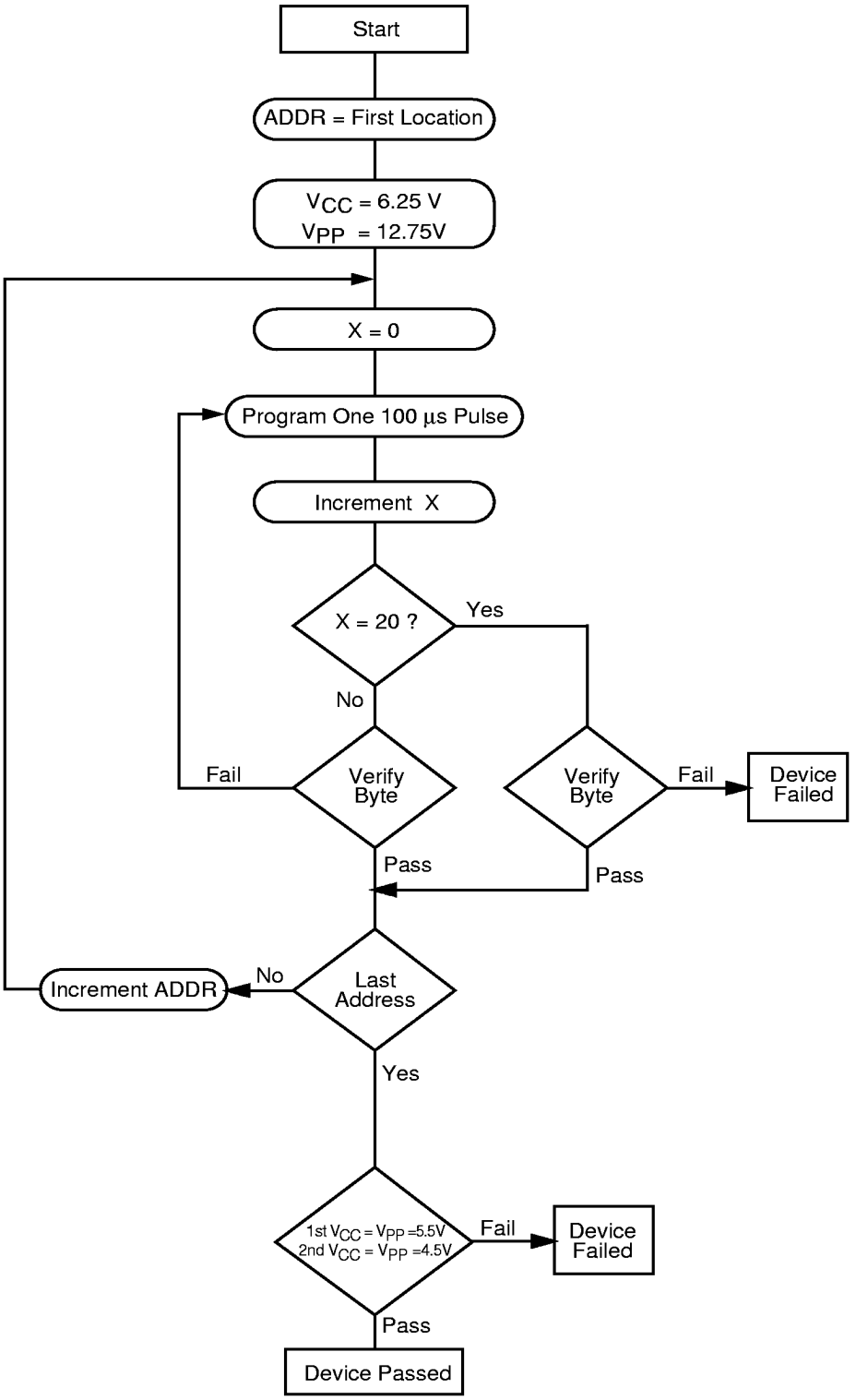

FIGURE 1.

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Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C16B are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at V_{CC} in the other modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other modes.

Read Mode

The NMC27C16B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C16B has a standby mode which reduces the active power dissipation by 99%, from 100 mW to 0.50 mW. The NMC27C16B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C16Bs are usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 21 (V_{PP}) will damage the NMC27C16B.

Initially, and after each erasure, all bits of the NMC27C16B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C16B is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins.

When the address and data are stable, an active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. The NMC27C16B is programmed with the Fast Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 100 µs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 µs pulse.

The NMC27C16B must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming multiple NMC27C16Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C16Bs may be connected together when they are programmed with the same data. A high level TTL pulse applied to the CE/PGM input programs the paralleled NMC27C16Bs.

TABLE 1. Mode Selection

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11), (13-17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{CC}	5	Hi-Z
Program	V_{IH}	V_{IH}	12.75V	6.25	D_{IN}
Program Verify	V_{IL}	V_{IL}	12.75V	6.25	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	12.75V	6.25	Hi-Z

Program Inhibit

Programming multiple NMC27C16Bs in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM all like inputs (including $\overline{OE}$) of the parallel NMC27C16Bs may be common. A TTL high level program pulse applied to an NMC27C16B's $\overline{CE}$/PGM input with V_{PP} at 12.75V will program that NMC27C16B. A TTL low level $\overline{CE}$/PGM input inhibits the other NMC27C16Bs from being programmed.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. Except during programming and program verify, V_{PP} must be at V_{CC}.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C16B has a manufacturer's identification code to aid in programming. The code, shown in Table 3, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C16B is, "8F80", where "8F" designates that it is made by Fairchild Semiconductor, and "80" designates a 16k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10, CE , and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C16B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å – 4000Å range. After programming, opaque labels should be placed over the NMC27C16B window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C16B is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a mimimum of 15 W-sec/cm^2.

The NMC27C16B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table 2 shows the minimum NMC27C16B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

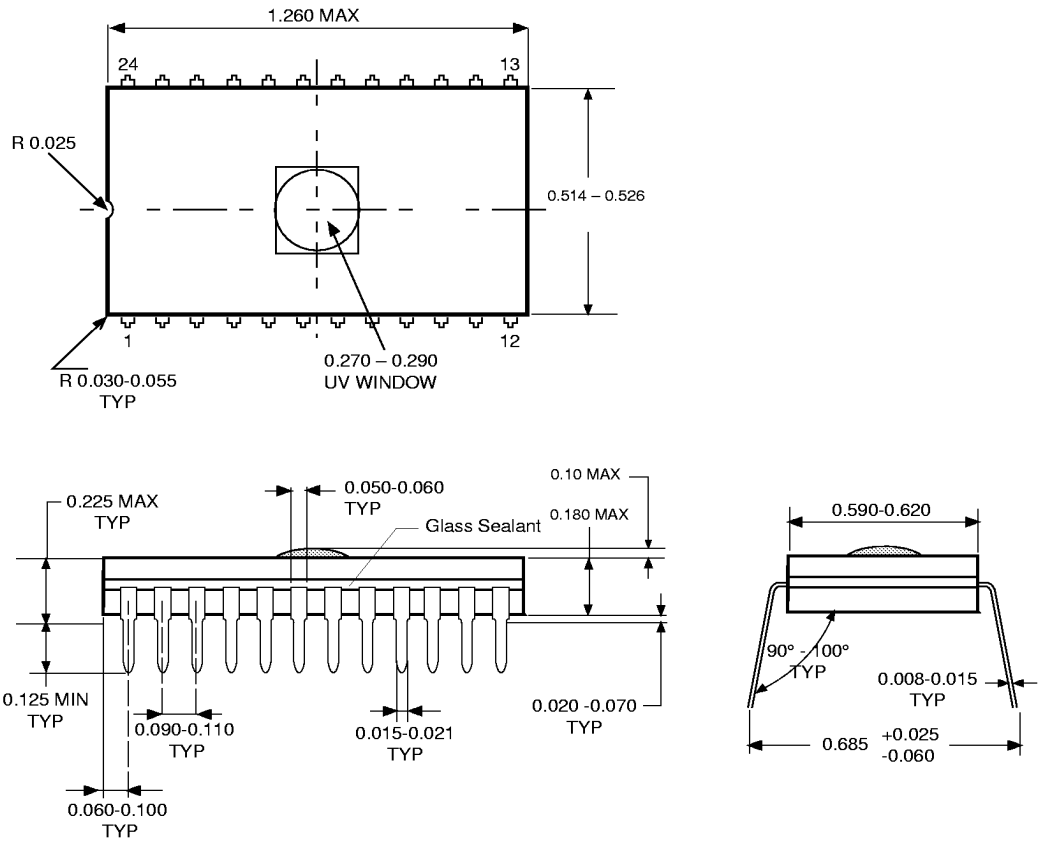
TABLE 2. Minimum NMC27C16B Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

TABLE 3. Manufacturer's Identification Code

Pins	A0 (8)	O7 (17)	O6 (16)	O5 (15)	O4 (14)	O3 (13)	O2 (11)	O1 (10)	O0 (9)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80

Physical Dimensions inches (millimeters) unless otherwise noted



UV Window Cavity Dual-In-Line Package (Q)
Order Number NMC27C16BQ
Package Number J24AQ

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Americas
Customer Response Center
Tel. 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +44 (0) 1793-856858
Deutsch Tel: +49 (0) 8141-6102-0
English Tel: +44 (0) 1793-856856
Français Tel: +33 (0) 1-6930-3696
Italiano Tel: +39 (0) 2-249111-1

Fairchild Semiconductor Hong Kong
8/F, Room 808, Empire Centre
68 Mody Road, Tsimshatsui East
Kowloon. Hong Kong
Tel; +852-2722-8338
Fax: +852-2722-8383

Fairchild Semiconductor Japan Ltd.
4F, Natsume Bldg.
2-18-6, Yushima, Bunkyo-ku
Tokyo, 113-0034 Japan
Tel: 81-3-3818-8840
Fax: 81-3-3818-8841