XRT7288

CEPT1
Line Interface

May 1998-2

FEATURES

- Fully Integrated 2.048Mbits/s Line Interface
- Intended For Use In Systems That Must Comply With CCITT Specifications G.703, G.823, I.431, G.732, G.735, G.739
- Pin-Selectable 75Ω or 120Ω Operation
- Monolithic Clock Recovery
- Low Power Dissipation:
  100mW for 120Ω Twisted Pair, Typical
  108mW for 75Ω Coaxial, Typical
- Minimal External Circuitry Required
- Robust Frequency Acquisition/Phase-Locked Loop
- Pin-Selectable HDB3 Encoder and Decoder
- Loopback Modes for Fault Isolation
- Multiple Link-Status and Alarm Features
- Single-Rail/Dual-Rail Interface

GENERAL DESCRIPTION

The XRT7288 CEPT1 Line Interface is an integrated circuit that provides a 2.048 Mbits/s line interface to either twisted-pair or coaxial cable as specified in CCITT requirements G.703, G.823, I.431, G.732, and G.735 G.739. The device performs receive pulse regeneration, timing recovery, and transmit pulse driving functions. The XRT7288 device is manufactured by using low-power CMOS technology and is available in a 28-pin, plastic DIP or in a 28-pin, plastic SOJ package for surface mounting. The XRT7288 device is functionally compatible with the LC1135B device. The digital circuitry is shown in *Figure 1.*; the analog circuitry is shown in *Figure 5.*

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRT7288IP	28 Lead 600 Mil PDIP	-40°C to +85°C
XRT7288IW	28 Lead 300 Mil Jedec SOJ	-40°C to +85°C

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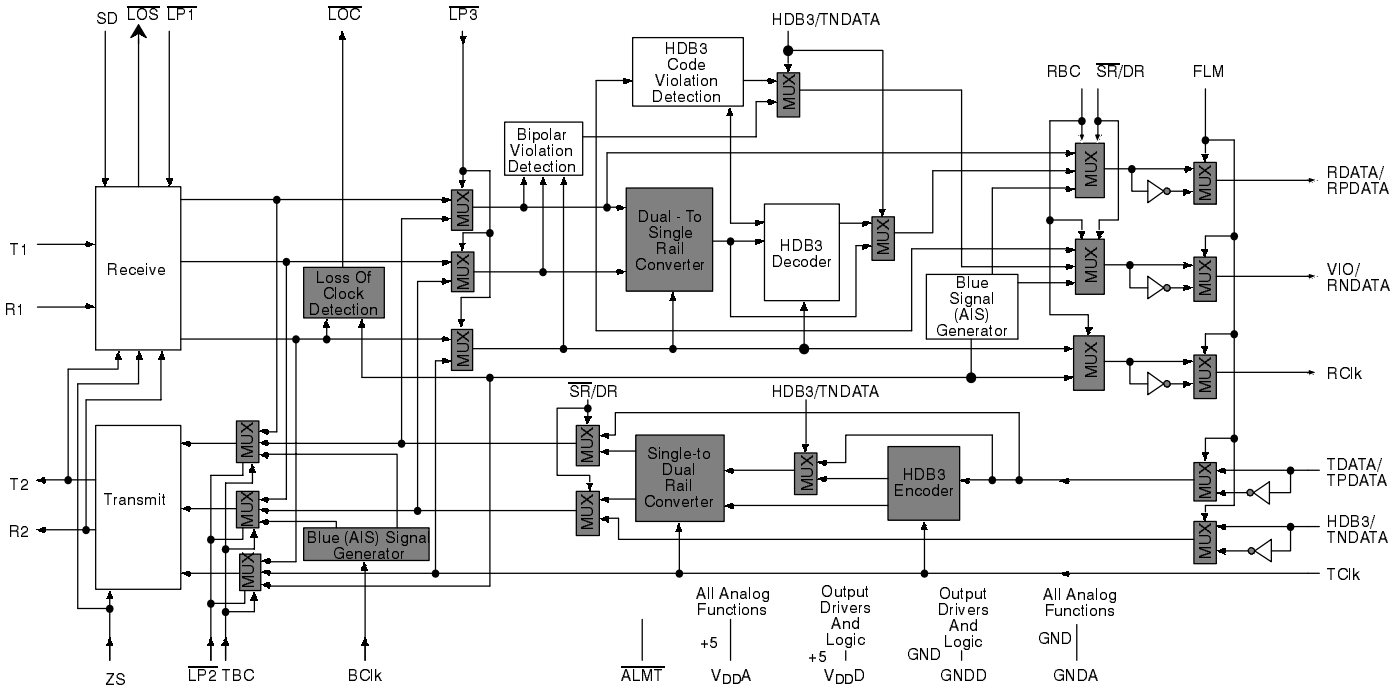
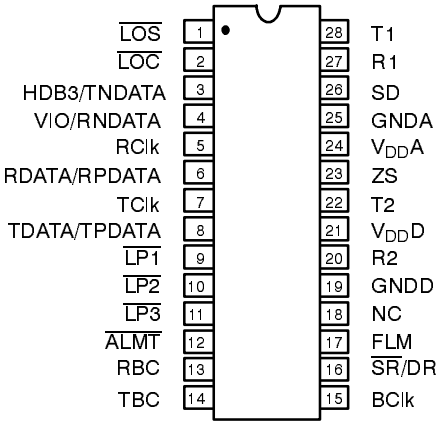
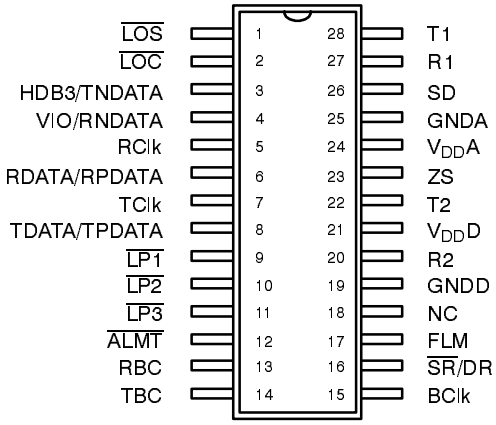


Figure 1. Digital Block Diagram

PIN CONFIGURATION



28 Lead PDIP (0.600")



28 Lead SOJ (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	$\overline{LOS}$	O	**Loss of Signal (Active-Low).** This pin is cleared (0) upon loss of the data signal at the receiver inputs.
2	$\overline{LOC}$	O	**Loss of Clock (Active-Low).** This pin is cleared when SD = 1 and $\overline{LOS}$= 0, indicating that a loss of clock has occurred. When $\overline{LOC}$= 0, no transitions occur on the RClk and on either RDATA (for single-rail) or RPDATA and RNDATA (for dual-rail operation) outputs. A valid clock must be present at BClk for this function to operate properly.
3	HDB3/ TNDATA	I	**HDB3 Enable/N-Rail Transmit Data.** If $\overline{SR}$/DR = 0, this pin is set (1) to insert an HDB3 substitution code on the transmit side and to remove the substitution code on the receive side. If $\overline{SR}$/DR = 1, this pin is used as the n-rail transmit input data (internal pull-down is included).
4	VIO/ RNDATA	O	**Violation/N-Rail Receive Data.** If $\overline{SR}$/DR = 0 and HDB3 = 0, bipolar violations on the receive side input are detected, causing VIO to be set; if HDB3 = 1, HDB3 code violations cause VIO to be set. If $\overline{SR}$/DR =1, this pin is used as the n-rail receive output data.
5	RClk	O	**Receive Clock.** Output receive clock signal to the terminal equipment.
6	RDATA/ RPDATA	O	**Receive Data/P-Rail Receive Data.** If $\overline{SR}$/DR = 0, this pin is used for 2.048 Mbits/s unipolar output data with a 100% duty cycle. If $\overline{SR}$/DR = 1, this pin is used as the p-rail receive output data.
7	TClk	I	**Transmit Clock.** Input clock signal (2.048 MHz ±80 ppm).
8	TDATA/ TPDATA	I	**Transmit Data/P-Rail Transmit Data.** If $\overline{SR}$/DR = 0, this pin is used as 2.048 Mbits/s unipolar input data. If $\overline{SR}$/DR = 1, this pin is used as the p-rail transmit input data.
9	$\overline{LP1}$	I	**Loopback 1 Enable (Active-Low).** This pin is cleared for a full local loopback (transmit converter output to receive converter input). Most of the transmit and receive analog circuitry is exercised in this loopback (internal pull-up is included).
10	$\overline{LP2}$	I	**Loopback 2 Enable (Active-Low).** This pin is cleared for a remote loopback. In loopback 2, a high on TBC (pin 14) inserts the blue signal (AIS) on the transmit side (internal pull-up is included).

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Type	Description
11	$\overline{LP3}$	I	**Loopback 3 Enable (Active-Low).** This pin is cleared for a digital local loopback. Only the transmit and receive digital sections are exercised in this loopback (internal pull-up is included).
12	$\overline{ALMT}$	I	**Alarm Test Enable (Active-Low).** This pin is cleared, forcing $\overline{LOS}$ = 0, $\overline{LOC}$= 0, and VIO = 1 for testing without affecting data transmission (internal pull-up is included).
13	RBC	I	**Receive Blue Control.** This pin is set to insert the blue signal (AIS) on the receive side (internal pull-down is included).
14	TBC	I	**Transmit Blue Control.** This pin is set to insert the blue signal (AIS) on the transmit side. This control has priority over a loopback 2 if both are operated (internal pull-down is included).
15	BClk	I	**Blue Clock.** Blue clock (AIS) input signal (2.048MHz ±80ppm). This clock can be independent of the transmit clock.
16	$\overline{SR}$/DR	I	**Single-Rail (Active-Low)/Dual-Rail Operation.** If $\overline{SR}$/DR = 0 (internal pull-down is included), single-rail operation is selected; if $\overline{SR}$/DR = 1, dual-rail operation is selected (*see Tables 3-5*).
17	FLM	I	**Framer Logic Mode.** If FLM = 0 (internal pull-down is included), logic mode 1 operation occurs. If FLM = 1, logic mode 2 operation occurs (*see Tables 3-5*).
18	NC		**No Connection.** Test pin for manufacturing purposes only. This pin must be left floating or tied to GNDD.
19	GNDD		**Digital Ground.**
20	R2	O	**Transmit Bipolar Ring.** Negative bipolar transmit output.
21	V_{DD}D		**5V Digital Supply (±10%).**
22	T2	O	**Transmit Bipolar Tip.** Positive bipolar transmit output.
23	ZS	I	**Impedance Select.** This pin is cleared for 75Ω coaxial cable operation and set for 120Ω shielded twisted-pair operation (internal pull-down is included)
24	V_{DD}A		**5V Analog Supply (±10%).**
25	GNDA		**Analog Ground.**
26	SD	I	**Shutdown Enable.** If this pin is high, a loss-of-signal detection ($\overline{LOS}$= 0) forces $\overline{LOC}$ low and causes the following (see *Table 2*): For single-rail operation: RClk high, RDATA low. For dual-rail, logic mode 1 operation RClk high, RPDATA and RNDATA low. For dual-rail, logic mode 2 operation: RClk low, RPDATA and RNDATA high (internal pull-down is included).
27	R1	I	**Receive Bipolar Ring.** Negative bipolar receive input
28	T1	I	**Receive Bipolar Tip.** Positive bipolar receive input.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = -40°C to +85°C; V_{DD} = 5V ±10%

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Logic Interface Electrical Characteristics						
	Input Voltage					
V_{IL}	Low	GNDD		0.8	V	
V_{IH}	High	2.0		V_{DD}D	V	
	Output Voltage[1]					
V_{OL}	Low	GNDD		0.4	V	2.0mA Sink
V_{OH}	High	2.4		V_{DD}D	V	80µA Source
C_I	Input Capacitance			20	pF	
C_L	Load Capacitance			40	pF	
Transmitter Specifications						
	Output Pulse Amplitude					
	75Ω (ZS = 0)	2.14	2.37	2.60	V	
	120Ω (ZS = 1)	2.70	3.00	3.30	V	
	Pulse Width (50%)	219	244	269	ns	
	Positive/Negative Pulse Imbalance			±5	%	
	Zero Level			±10[2]	%[2]	
	Output Transformer Turns Ratio	1:1.33	1:1.36	1:1.39		
Receiver Specifications						
	Receiver Sensitivity[3]	0.7		4.2	Vp	
	Allowed Cable Loss at BER 10^{-9}					
	No Interference		10	7	dB	
	Interfering PBRS, 18dB			6	dB	
	Below Transmitted PBRS					
	PLL[4]					
	3dB Bandwidth		28		kHz	
	Peaking		0.24	0.5	dB	
	ICO Free-running Frequency Error			±7	%	

Notes

[1] Digital outputs drive purely capacitive loads to full output levels (V_{DD}D, GNDD)

[2] Percentage of the nominal pulse amplitude.

[3] Measured at T1, R1 (V peak-to-zero, GND reference)

[4] Transfer characteristics (1/4 input)

[5] All measurements are with a matched-impedance transmit interface (see Figure 2. and Figure 3.) and with V_{DD} or GND applied to digital input leads.

Internal pull-up devices are provided on the following input leads: $\overline{LP1}$, $\overline{LP2}$, $\overline{LP3}$ and $\overline{ALMT}$. Internal pull-down devices are provided on the following leads: SD, RBC, HDB3/TNDATA, TBC, $\overline{SR}$/DR, FLM, and ZS. The internal pull-up or pull-down devices require the input to source or sink to be no more than 20µA.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Receiver Specifications (Cont'd)						
	Input Transformer Turns Ratio	1:1.9	1:2.0	1:2.1		
	Input Resistance, RI or TI, Each Input to Ground	0.9		3.0	kΩ	
Jitter (20Hz-100kHz)						
	Receive Plus Transmit Jitter at T2/R2		0.06	0.09		U.I. peak-to-peak
	Transmit Jitter at T2/R2		0.012	0.04		U.I. peak-to-peak
Power Dissipation[5] (TA=-40°C to +85°C, V_{DD}=5.0 V ±10%)						
	Power Dissipation					
Pdis	75 (ZS = 0)		190	290	mW	All 1s transmit and
Pdis	120 (ZS = 1)		170	260	mW	receive data, V_{DD}=5.5V
	Power Dissipation:					
Pdis	75 (ZS = 0)		170		mW	All 1s transmit and
Pdis	120 (ZS = 1)		150		mW	receive data, V_{DD}=5.0V
	Power Dissipation:					
Pdis	75 (ZS = 0)		108		mW	PRBS (50% 1s) transmit and
Pdis	120 (ZS = 1)		100		mW	receive data, V_{DD}=5.0V

Notes

[1] Digital outputs drive purely capacitive loads to full output levels (V_{DD}D, GNDD)

[2] Percentage of the nominal pulse amplitude.

[3] Measured at T1, R1 (V peak-to-zero, GND reference)

[4] Transfer characteristics (1/4 input)

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Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (V_{DD}) . . . . . -0.5V to +6.5V
Power Dissipation (Pdis) 500mW
Storage Temperature (Tstg) . . . . . -65°C to +125°C

Maximum Voltage (any pin) with Respect to V_{DD} 0.5V
Minimum Voltage (any pin) with Respect to GND . . . . . -0.5V
Maximum Allowable Voltages (T1, R1) with Respect to GND . . . . . -5.0V to 5.0V

Note:

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operation sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.
pin assignment ordering information

SYSTEM DESCRIPTION

The XRT7288 device is a fully integrated line interface that requires only two transformers, three input termination resistors, and two output impedance-matching resistors to provide a bidirectional line interface between a 2.048 Mbits/s CEPT datalink and terminal equipment. Typical application diagrams are shown in *Figure 2.* and *Figure 3.* for 75Ω coaxial cable and 120Ω shielded twisted-pair operation, respectively.

The circuit is divided into three main blocks: transmit converter, receive converter, and logic. The transmit and receive converters process information signals through the device in the transmit and receive directions, respectively; the logic is the control and status interface for the device. *Figure 2.* and *Figure 3.* include a matched-impedance transmit-interface section in order to match the output impedance of the transmitter to the line. See *Table 1* for the G.703/CH-PTT specifications for transmit-interface return loss.

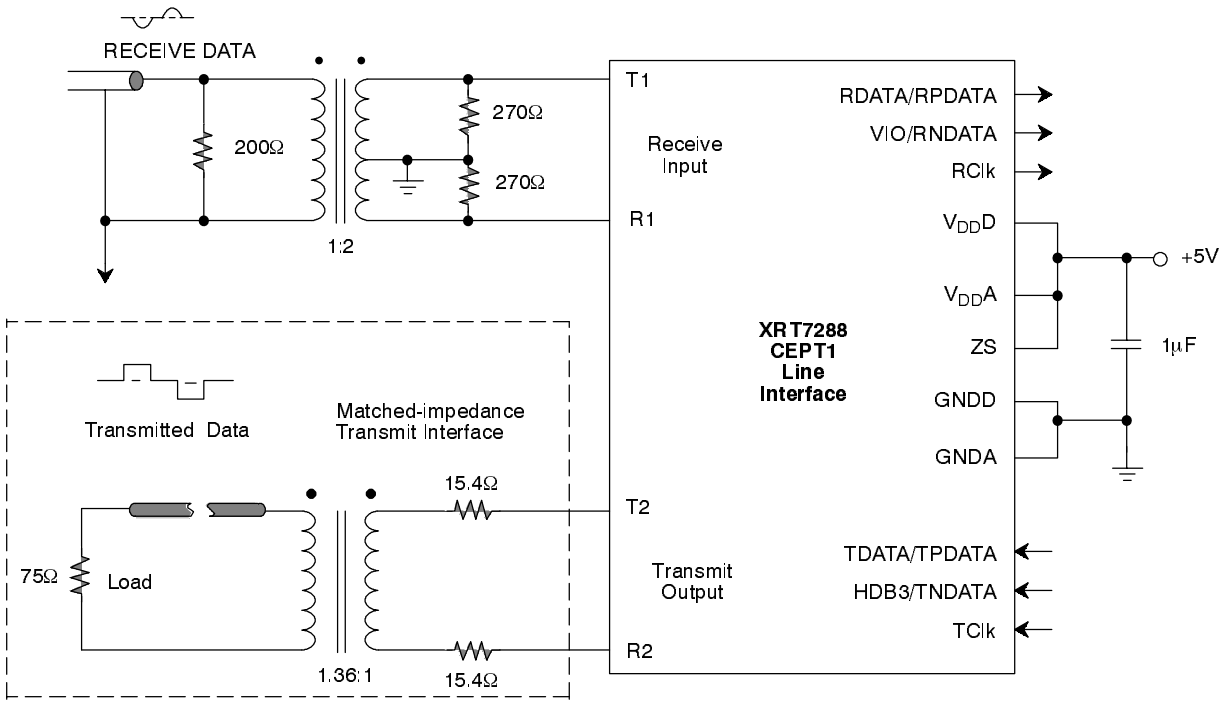


Figure 2. Typical Application Diagram for Coaxial Environment

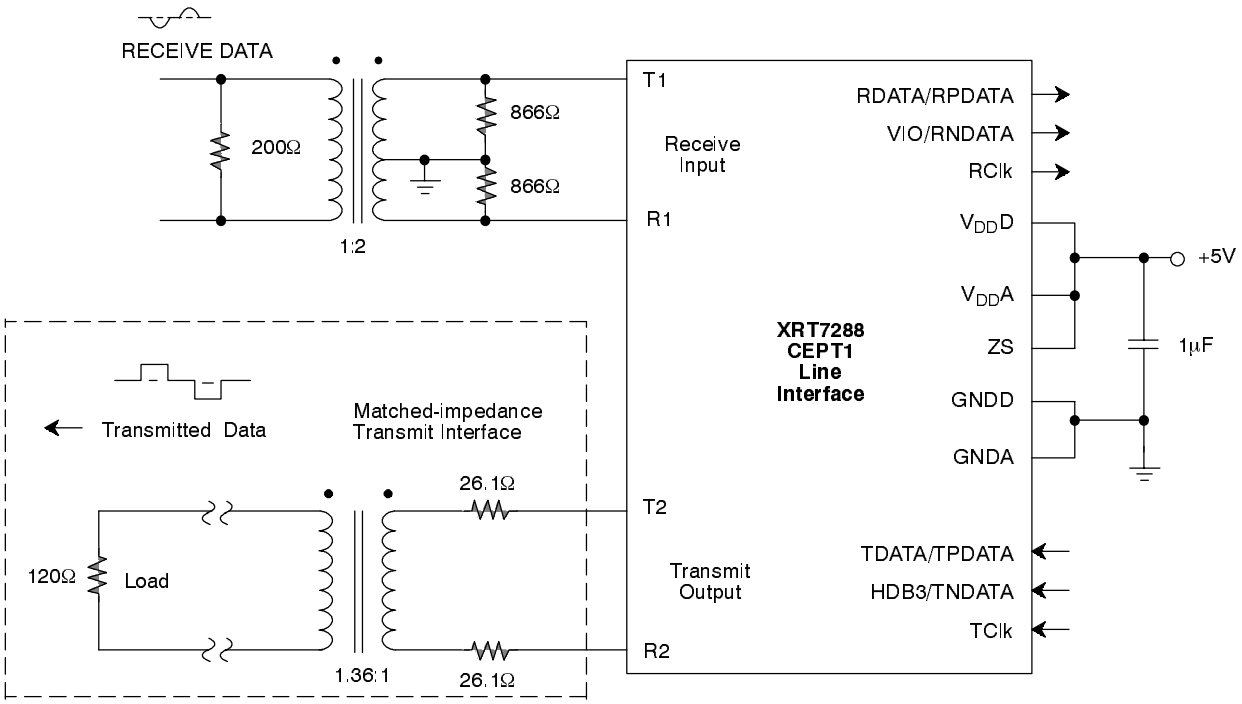


Figure 3. Typical Application Diagram for Shielded Twisted-Pair Environment

Interface	Min	Typ	Max	Units
Transmit				
51 kHz to 102 kHz	8	28		dB
102 kHz to 2.048 MHz	14	26		dB
2.048 MHz to 3.072 MHz	10	24		dB
Receive				
51 kHz to 102 kHz	12	32		dB
102 kHz to 2.048 MHz	18	31		dB
2.048 MHz to 3.072 MHz	14	30		dB

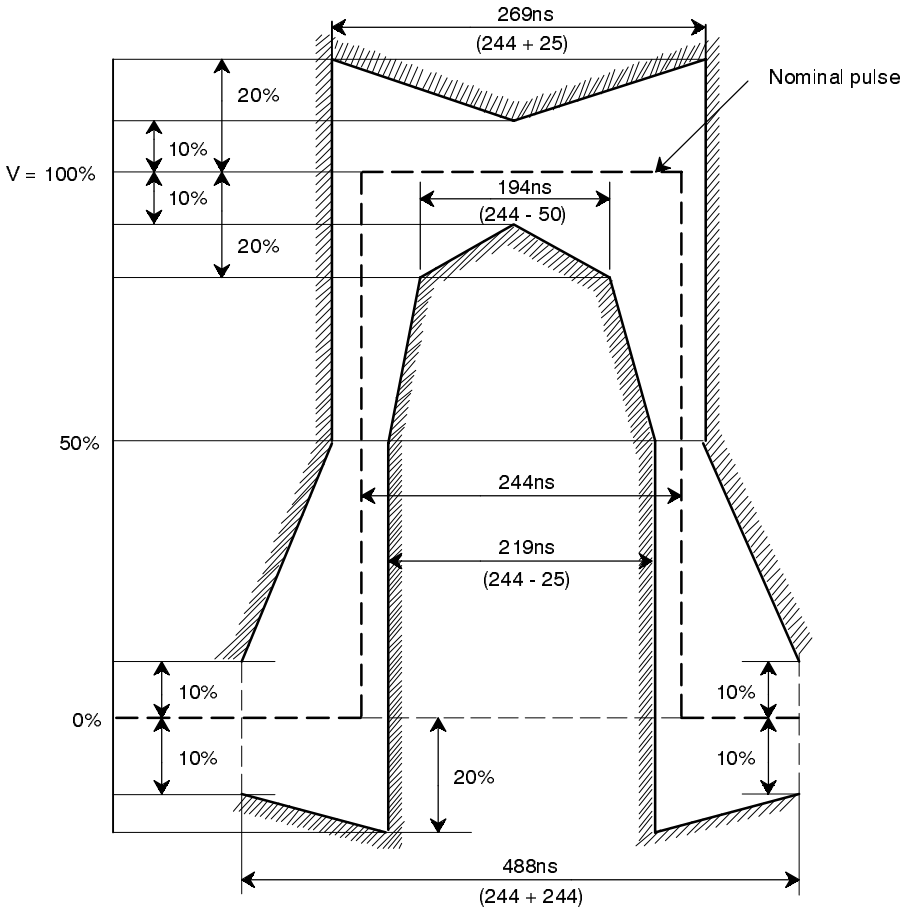
Table 1. Return Loss (resistor tolerance: 1% on transmit side, 2% on receive side)

Transmit Converter

The line-interface transmission format is return-to-zero, bipolar alternate mark inversion (AMI), requiring transmission and sensing of alternately positive and negative pulses. The transmit converter accepts unipolar data and clock and converts the signal to a balanced bipolar data signal. Binary 1s in the data stream become pulses of alternating polarity transmitted between the two output rails, T2 and R2. Binary 0s are transmitted as null pulses.

The output pulse waveform is nominally rectangular. The pulses are produced by a high-speed D/A converter and are driven onto the line by low-impedance output buffers. The positive and negative pulses meet CCITT specification G.703 template requirements. The normalized pulse template is shown in *Figure 4.* A block diagram of the analog circuitry is shown in *Figure 5.*

The clock multiplier shown in *Figure 5.* uses a phase-locked loop (PLL) to produce the high-speed timing waveforms needed to produce a well-controlled pulse width. The clock multiplier also eliminates the need for the tightly.controlled transmit clock duty cycle usually required in discrete implementations. Transmitter specifications are shown in the Electrical Characteristics table.



Note: *V corresponds to the nominal peak value*

Figure 4. CCITT G.703 Pulse Template

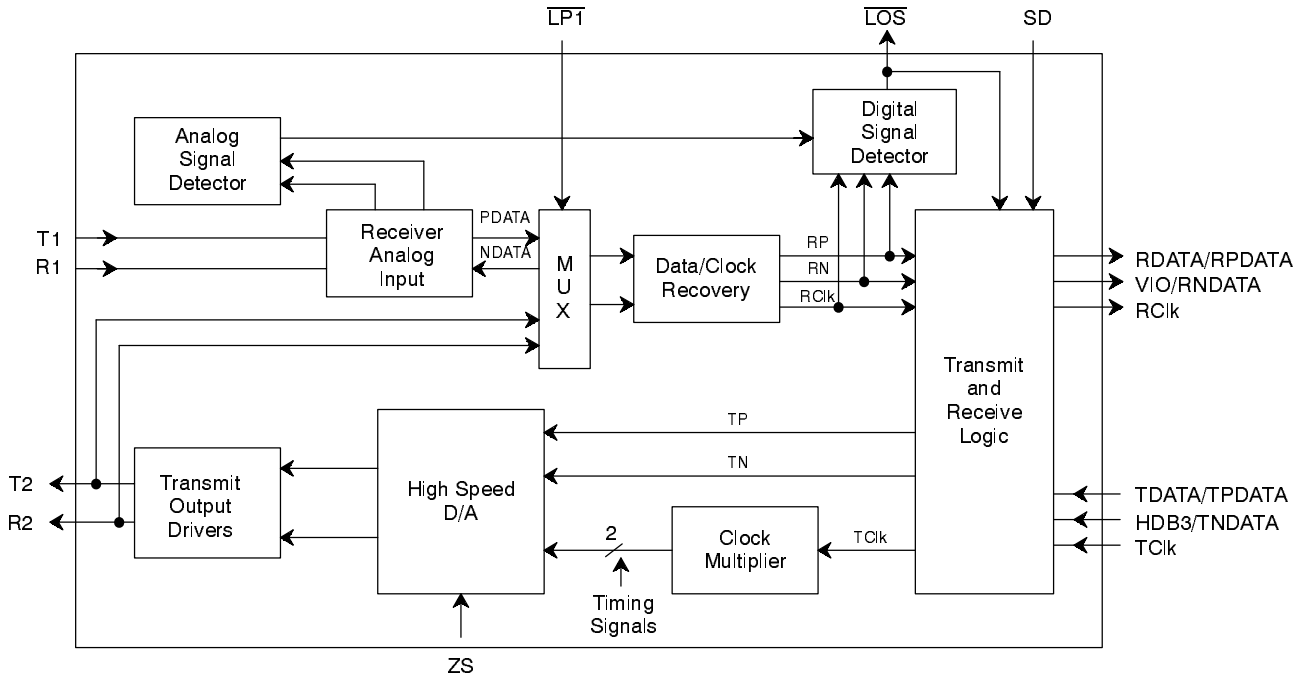


Figure 5. XRT7288 Analog Block Diagram

RECEIVE CONVERTER

The receive converter accepts bipolar input signals (T1, R1), with a maximum of 6dB loss at 1024kHz, through the interconnection cable. The received signal is rectified while the amplitude and rise time are restored. These input signals are peak-detected and sliced by the receiver front end, producing the digital signals PDATA and NDATA (see *Figure 5.*) Receive decision levels are automatically adjusted to be 50% of peak-to-zero signal levels. The timing is extracted by means of PLL circuitry that locks an internal, free-running, current-controlled oscillator (ICO) to the 2.048MHz component.

The PLL employs a 3-state phase detector and a low-voltage/temperature coefficient ICO. The ICO free-running frequency is trimmed to within ±2.5% of the data rate at wafer probe, with V_{DD} = 5.0 V and TA = 25°C. For all operating conditions (see Operating Conditions section), the free-running oscillator frequency deviates from the data rate by less than ±7%, alleviating the problem of harmonic lock.

For robust operation, the PLL is augmented with a frequency-acquisition capability. This feature detects if the recovered PLL clock (RClk) deviates by more than +1.7/-1.6% in frequency from a 2.048 MHz reference clock, which must be provided at BClk. If the RClk frequency is not within the prescribed range of the BClk frequency, the XRT7288 device enters a training mode in which receive input data is disconnected from the PLL, and the RClk frequency is steered to equal the BClk frequency. After frequency acquisition is completed, the PLL reconnects to receive input data to acquire proper phase-lock and timing of RClk with respect to the incoming T1, R1 data. Valid data is available when proper phase-lock has been achieved.

The frequency acquisition circuitry is intended to avoid improper harmonic locking during start-up situations, such as power-up or data interruption. Once the XRT7288 device is phase-locked to data, the frequency-acquisition mode will not be activated.

A continuous (i.e., ungapped, unswitched) 2.048 MHz reference clock must be present at BClk to enable the frequency-acquisition circuitry. However, the receive PLL will operate even in the absence of a 2.048 MHz clock at BClk. The 2.048 MHz clock at TClk can also be used to provide the 2.048 MHz reference at BClk.

Because the clock output of the receive converter is derived from the ICO, a free-running clock can be present at the output of the receive converter without data being present at the input. A shutdown pin (SD) is provided to block this clock, if desired, to eliminate the free-running clock upon loss of the input signal.

Both analog and digital methods of loss of signal detection are used in the XRT7288 device. The analog signal detector shown in *Figure 5.* uses the output of the receiver peak detector to determine if a signal is present at T1 and R1. If the input amplitude drops below 0.25 V, typical, the analog detector output becomes active. Analog loss-of-signal is registered, at most, several milliseconds after a drop in signal level, depending on a variety of factors, such as initial signal amplitude. Hysteresis (140 mV, typical) is provided in the analog detector to eliminate $\overline{LOS}$ chattering. The digital signal detector counts 0s in the recovered data. If more than 32 consecutive 0s occur, the digital signal detector becomes active. In normal operation, the detector outputs are ORed together to form $\overline{LOS}$; however, in loopback 1, only the digital signal detector is used to monitor the looped signal. *Table 2* describes the operation of the shutdown, $\overline{LOS}$, and $\overline{LOC}$ functions in normal operation and in loopback 1.

The PLL is designed to accommodate large amounts of input jitter with high power supply rejection for operation in noisy environments. Low jitter sensitivity to power supply noise allows compact line-card layouts that employ many line interfaces on one board. The minimum input jitter tolerance, as specified in CCITT specification G.823, and the measured XRT7288 device jitter tolerance are shown in *Figure 6.* Receiver specifications are shown on page 4. The XRT7288 device satisfies the CCITT jitter transfer function requirement of recommendations G.735 G.739 (see *Figure 7.*)

Inputs							Outputs		
							Receive Side		
$\overline{LP1}$	SD	$\overline{ALMT}$	Input Signal at T1, R1	Loopback 1 Signal	$\overline{LOS}$	$\overline{LOC}$	Receive Data[1]	RClk[1]	Active LOS Detectors
1	0	1	Active	x	1	1	Normal	Normal	Analog & Digital
1	0	1	No Signal	x	0	1	Low[2]	Free-running ICO[2]	Analog & Digital
1	1	1	Active	x	1	1	Normal	Normal	Analog & Digital
1	1	1	No Signal	x	0	0	Low[3]	High	Analog & Digital
0	0	1	x	Active	1	1	Normal Loopback	Normal Loopback	Digital Only
0	0	1	x	No Signal	0	1	Low[4]	Free-running ICO[4]	Digital Only
0	1	1	x	Active	1	1	Normal Loopback	Normal Loopback	Digital Only
0	1	1	x	No Signal	0	0	Low	High	Digital Only
x	x	0	x	x	0	0	Unaffected	Unaffected	x

Notes:

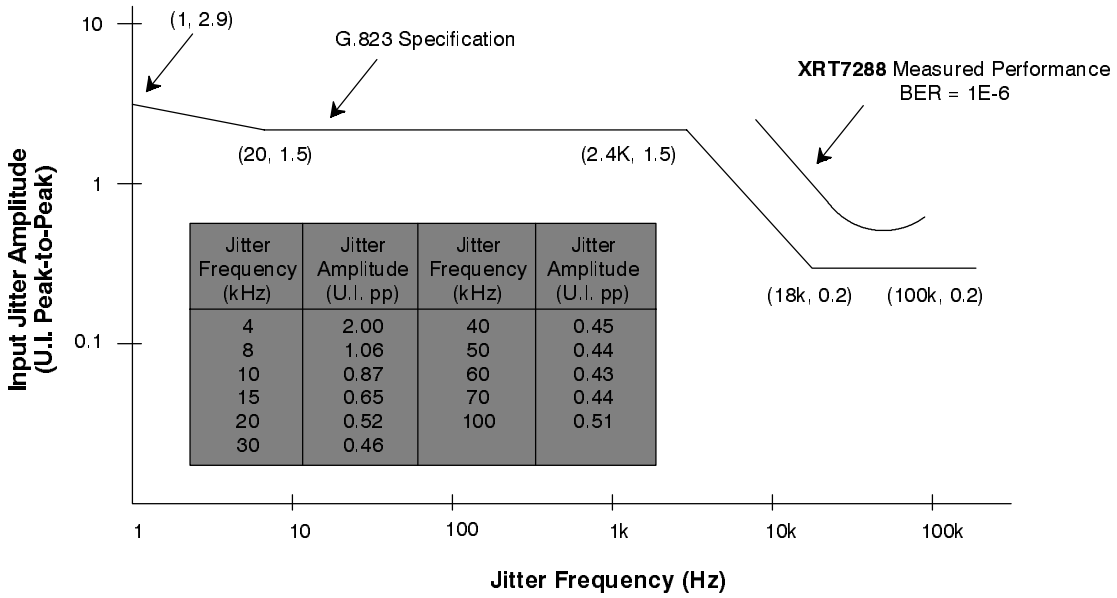
[1] *These values apply for single-rail or dual-rail/logic mode 1. For dual-rail/logic mode 2, all logic-level outputs except for looped back data are the inverse of that shown above.*

[2] *Activated by analog loss-of-signal (LOS) detection.*

[3] *Digital LOS detection forces receive data low . Analog LOS detection merely forces receive data to stop transitions; receive data will be forced either high or low with analog LOS detection.*

[4] *All-0s looped back data, no HDB3 operation. Sufficiently sparse looped back data (not HDB3 encoded) also causes the receive ICO to free run; therefore, properly timed loopback data is not guaranteed.*

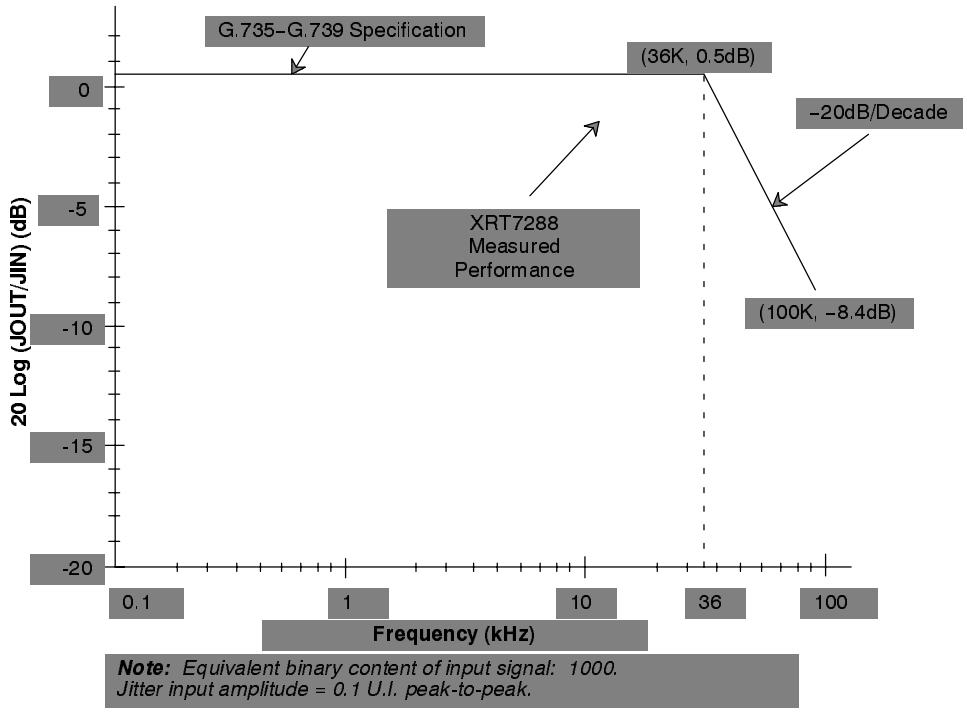
Table 2. Shutdown LOS and LOC Truth~Table
x = don't care.



Jitter Frequency (kHz)	Jitter Amplitude (U.I. pp)	Jitter Frequency (kHz)	Jitter Amplitude (U.I. pp)
4	2.00	40	0.45
8	1.06	50	0.44
10	0.87	60	0.43
15	0.65	70	0.44
20	0.52	100	0.51
30	0.46		

Note: *Measurement conditions random data, TA = 25°C, V_{DD} = 5V, 6dB cable loss, BClk clock present*

Figure 6. Random Input Data Jitter Tolerance (HDB3 Encoded)



Note: *Equivalent binary content of input signal: 1000. Jitter input amplitude = 0.1 U.I. peak-to-peak.*

Figure 7. Receive Jitter Transfer Function

Digital Logic

The logic provides alarms, optional HDB3 coding, blue signal (AIS) insertion circuits, and maintenance loopbacks. It also optionally performs dual-rail to single-rail conversion of the data and provides an alternate logic polarity (logic mode 2) in dual-rail mode for receive clock and receive and transmit data.

Single-Rail/Dual-Rail Interface and Alternate Logic Mode

The XRT7288 device supports either single-rail or dual-rail operation by setting the control pin $\overline{SR}$/DR. In the single-rail mode ($\overline{SR}$/DR = 0), the XRT7288 receiver converts bipolar input signals (T1, R1) to a unipolar output signal on RDATA. The XRT7288 transmitter converts a unipolar input signal on TDATA to a balanced bipolar data signal on pins T2 and R2. If desired, the HDB3 control pin can be used to set HDB3 encoding/decoding. Violation information is available on output pin VIO.

In the dual-rail mode ($\overline{SR}$/DR = 1), the XRT7288 receiver converts bipolar input signals (T1, R1) to p-rail and n-rail, nonreturn-to-zero output data on pins RPDATA and RNDATA, respectively. The XRT7288 transmitter converts non-return-to-zero p-rail and n-rail input data on pins TPDATA and TNDATA, respectively, to a balanced bipolar data signal on pins T2 and R2. In the dual-rail mode, HDB3 encoding/decoding and bipolar violation output functions are unavailable.

In the dual-rail mode, an alternate-logic polarity mode is available via control pin FLM. If FLM = 1, the XRT7288 device operates in logic mode 2; RClk is inverted with respect to logic mode 1, and input and output data (TPDATA, TNDATA, RPDATA, and RNDATA) are active-low (see *Figures 10-13*).

Internal pull-downs on signals $\overline{SR}$/DR and FLM set default operation to single-rail, logic mode 1 (see *Table 3*)

FLM	$\overline{SR}$/DR	Single-/Dual-Rail	Logic Mode
0[1]	0[1]	Single	1
0	1	Dual	1
1	0	X[2]	X[2]
1	1	Dual	2

Notes:
[1] Default operation (identical with LC1135B) if both pins are unconnected.
[2] X = illegal option

Table 3. Rail Interface and Logic Mode Options

Pin	Name	Function
3	HDB3/TNDAT	HDB3 Enable
4	VIO/RNDATA	VIO Violation
6	RDATA/RPDATA	RDATA Receive Data
8	TDATA/TPDATA	TDATA Transmit Data

Table 4. Single-Rail Operation (Default State) $\overline{SR}$/DR = 0 (or left unconnected internal pull-down circuitry).

Pin	Name	Function
3	HDB3/TNDATA	N-rail Transmit Input Data
4	VIO/RNDATA	N-rail Receive Output Data
6	RDATA/RPDATA	P-rail Receive Output Data
8	TDATA/TPDATA	P-rail Transmit Input Data

Table 5. Dual-Rail Operation $\overline{SR}$/DR = 1

Alarms

An independent loss-of-clock ($\overline{LOC}$) output is provided so that loss of clock is detected when the shutdown option is in effect. $\overline{LOS}$ and $\overline{LOC}$ can be wire-ORed to produce a single alarm.

A bipolar violation output is included if HDB3 = 0, giving an alarm (VIO) each time a violation occurs (two or more successive 1s on a rail). The violation alarm output is held in a latch for one cycle of the internal clock (RClk). In the HDB3 mode, HDB3 code violations are detected and an alarm is produced.

An alarm test pin ($\overline{ALMT}$) is provided to test the alarm outputs, $\overline{LOS}$, $\overline{LOC}$ and VIO. Clearing this pin forces the alarm outputs to the alarm state without affecting data transmission.

HDB3 Option

The XRT7288device contains an HDB3 encoder and decoder (for single-rail mode only, i.e., $\overline{SD}$/DR = 0) that can be selected by setting the HDB3 pin. This allows the encoder to substitute a zero-substitution code for four consecutive 0s detected in the data stream, as illustrated in *Table 6* A "V" represents a violation of the HDB3 code, and a "B" represents a bipolar pulse of correct polarity. The decoder detects the zero-substitution code and reinserts four 0s in the data stream.

Case 1: Preceding mark has a polarity opposite the polarity of the preceding violation and is not a violation itself.

Case 2: Preceding mark has a polarity the same as the polarity of the preceding violation or is a violation itself.

	Case 1	Case 2
Before HDB3	0000	0000
After HDB3	000V	B00V

Table 6. HDB3 Substitution Code

Blue Signal (AIS) Generators

There are two blue signal (AIS) generators in this device. One (RBC = 1) substitutes an all-1s signal on RDATA output ($\overline{SR}$/DR = 0) or RPDATA and RNDATA ($\overline{SR}$/DR = 1) toward the terminal equipment. The other (TBC = 1) substitutes a bipolar, all-1s signal for the bipolar data out of the transmit converter which can be used to keep line repeaters active.

Loopback Paths

The XRT7288 device has three independent loopback paths that are activated by clearing the respective control inputs, $\overline{LP1}$, $\overline{LP2}$ or $\overline{LP3}$. Loopback 1 bridges the data stream from the transmit converter (transmit converter included) to the input of the receive converter. This maintenance loop includes most of the internal circuitry.

Loopback 2 provides a loopback of data and recovered clock from the bipolar inputs (T1, R1) to the bipolar outputs of the transmit converter (T2, R2). The receive front end, receive PLL, and transmit driver circuitry are all exercised. The loop can be used to isolate failures between systems. TBC = 1 overrides this function.

Loopback 3 loops the data stream as in loopback 1 but bypasses the transmit and receive converters. The blue signal (AIS) can be transmitted to the line when in this loopback. Loopbacks 2 and 3 can be operated simultaneously to provide transmission loops in both directions.

Current Pulses

With all other pins grounded, current pulses of maximum value and time widths are allowed on the T1/R1 and T2/R2 pins without damaging the device, as shown in *Table 7*. Also, to help ensure long-term reliability, the average value of a current-pulse train is specified.

Pin	Max Value	Width	Avg Value
T1, R1	±20 mA	1µs to 1s	±6 mA
T2, R2	±200 mA	1µs to 1s	±40 mA

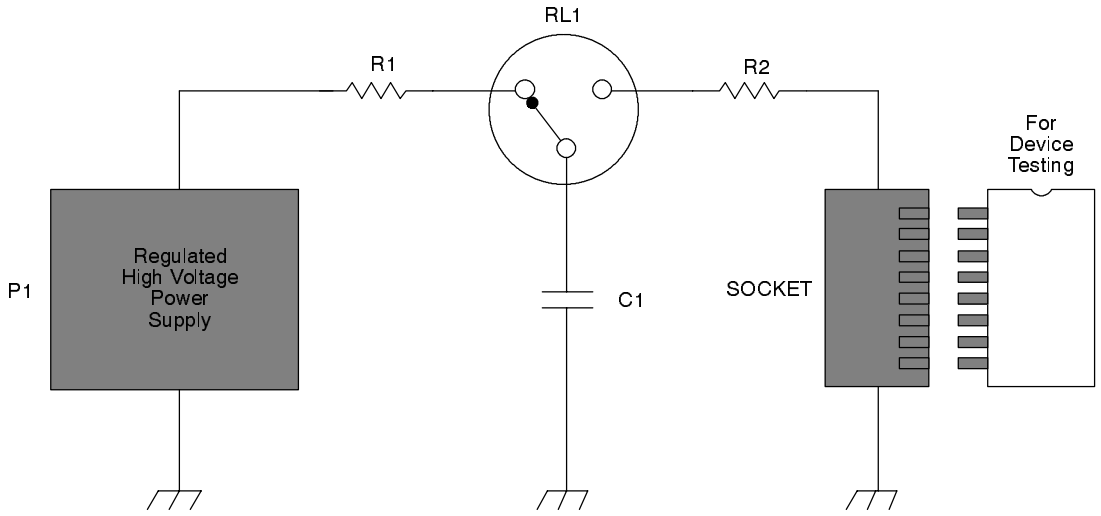
Table 7. Maximum Allowable Current

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. EXAR employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

HBM ESD Threshold	
Device	Voltage
XRT7288	>2500 V

Table 8.



Notes:
P1—0kV to 5kV DC power supply.
R1—At least 10 MΩ, high-voltage, 1W carbon composition.
RL1—High-voltage (5 kV) relay of a bounceless type (mercury-wetted or equivalent).
C1—100pF, 5kV capacitor.
R2—1500 Ω ±5%, 1W carbon composition < 1pF shunt capacitance.

Figure 8. Circuit Schematic of Human-Body ESD Simulator

Timing Characteristics

All duty−cycle and timing relationships are in reference to a TTL, 1.4V threshold level.

Loss−of−Clock Indication Timing

The clock must be absent 6.4 s to guarantee a loss−of−clock indication. However, a loss−of−clock indication can occur if the clock is absent for as little as 1.95μs, depending on the timing relationship of the interruption with respect to the timing cycle.

The returning clock must be present 3.91μs to guarantee a normal condition on the loss−of−clock pin (LOC). However, the loss−of−clock indication can return to normal immediately, depending on the timing relationship of the signal return with respect to the timing cycle.

T_A = −40°C to ±85°C; V_{DD} = 5 V±10%; load capacitance = 40 pF.

Symbol	Description	Min	Typ	Max	Unit
tTCLTCL	TCLK Clock Period	[1]	488	[1]	ns
tTCHTCL	TCLK Duty Cycle	40	50	60	%
tTDVTCL	Data Setup Time, TDATA[2] to TCLK	50			ns
tTCLTDV	Data Hold Time, TCLK to TDATA[2]	40			ns
tr	Clock Rise Time (10% 90%)			40	ns
tf	Clock Fall Time (10% 90%)			40	ns
tRCLRCL	RCLK Duty Cycle	40	50	60	%
tRCHRDV	Data Hold Time, RCLK to RDATA, VIO[3]	171			ns
tRDVRCH	Data Setup Time, RDATA, VIO to RCLK[3]	131			ns
tRCLRDV	Propagation Delay, RCLK to RDATA, VIO[3]			40	ns

Table 9. Clock Timing Relationships

Notes

[1] *A tolerance of 80 ppm.*

[2] *DATA for single−rail mode; TPDATA and TNDATA for dual−rail mode.*

[3] *RDATA and VIO for single−rail mode; RPDATA and RNDATA for dual−rail mode.*

TIMING DIAGRAMS (Single-Rail or Dual-Rail, Logic Mode 1)

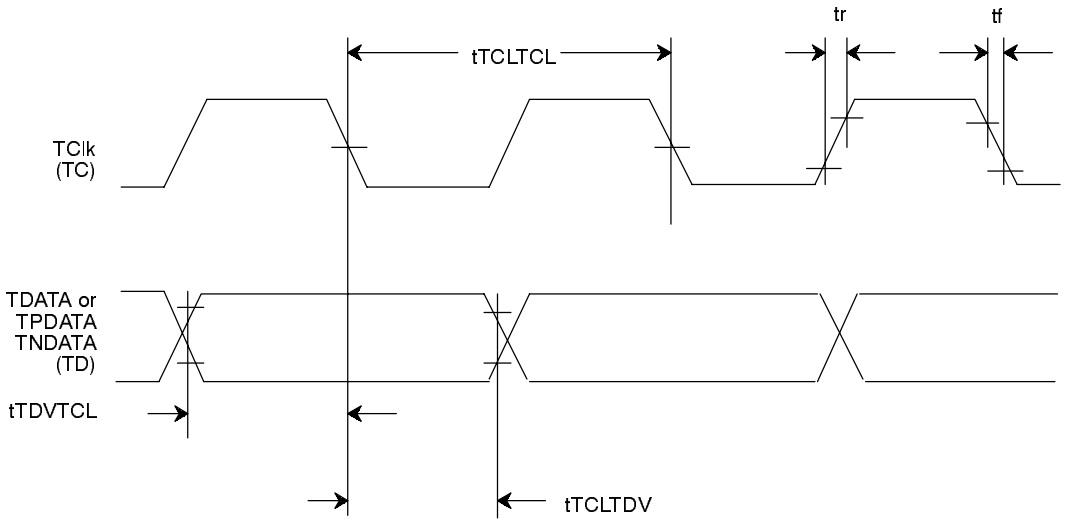


Figure 9. Transmit Timing

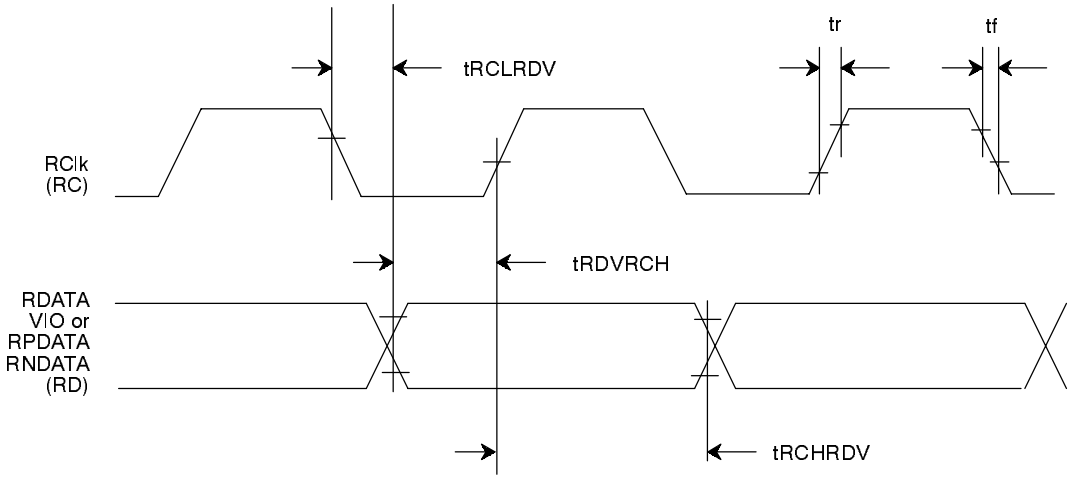


Figure 10. Receive Timing

TIMING DIAGRAMS (Dual-Rail, Logic Mode 2)

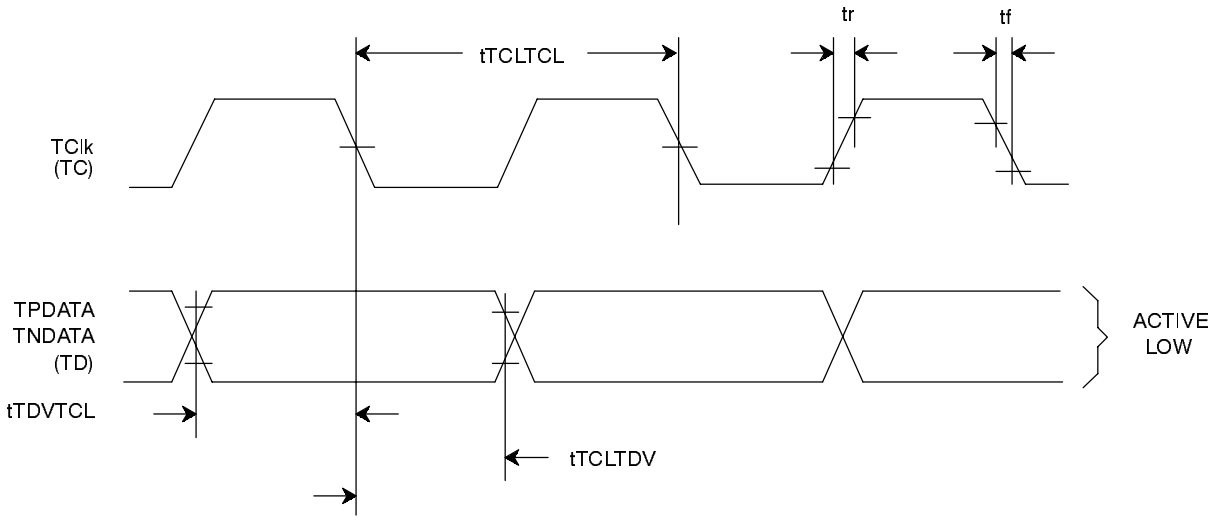


Figure 11. Transmit Timing

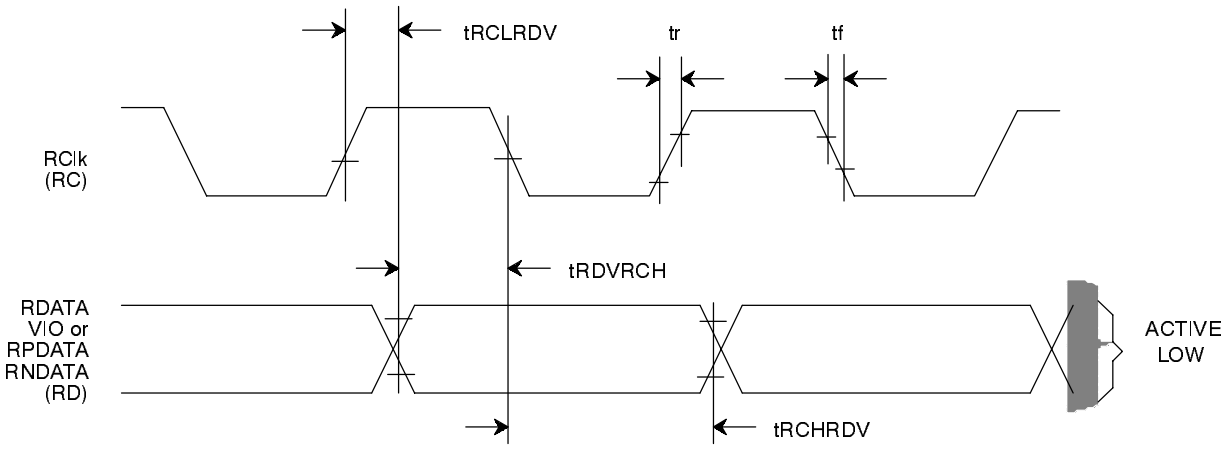


Figure 12. Receive Timing

TRANSFORMER REQUIREMENTS

Part Number	Isolation Rating	Turns Ratio
PE-65415	1500 VRMS	1CT:2CT
PE-65351	1500 VRMS	1:2CT
PE-65885	3000 VRMS	1CT:2CT

Table 10. Input Transformer Requirements

Part Number	Isolation Rating	Turns Ratio
PE-64937	1500 VRMS	1:1.36
PE-65586	1500 VRMS	1:1.36CT
PE-65882	3000 VRMS	1:1.37CT

Table 11. Output Transformer Requirements

Magnetic Supplier Information:

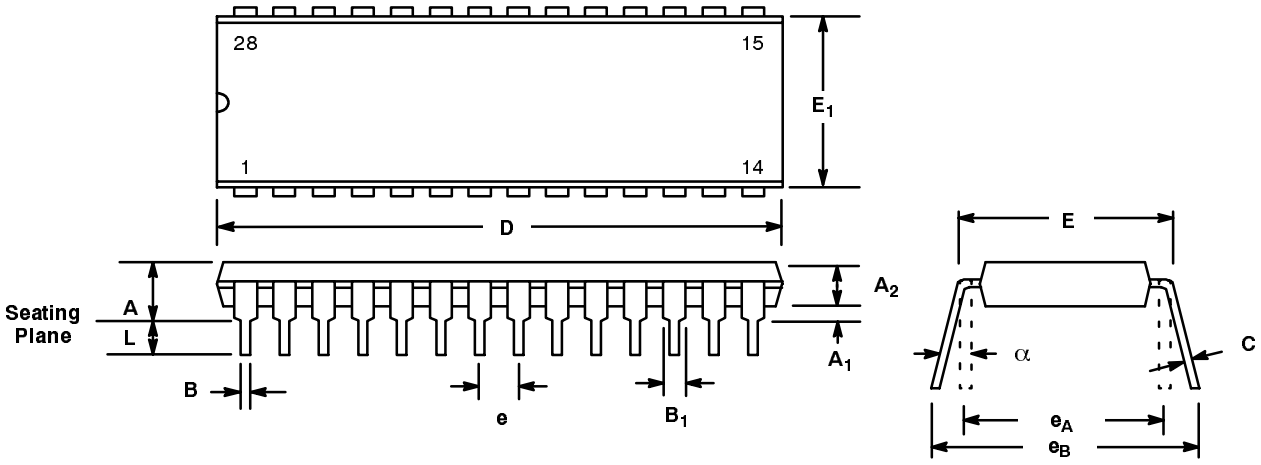
Pulse
Telecom Product Group
P.O. Box 12235
San Diego, CA 92112
Tel. (619) 674-8100
Fax. (619) 674-8262

Note:

The user is urged to consult the Transformer Manufacturer's data sheets in order to verify that it meets all of their system requiremnets.

28 LEAD PLASTIC DUAL-IN-LINE (600 MIL PDIP)

Rev. 1.00

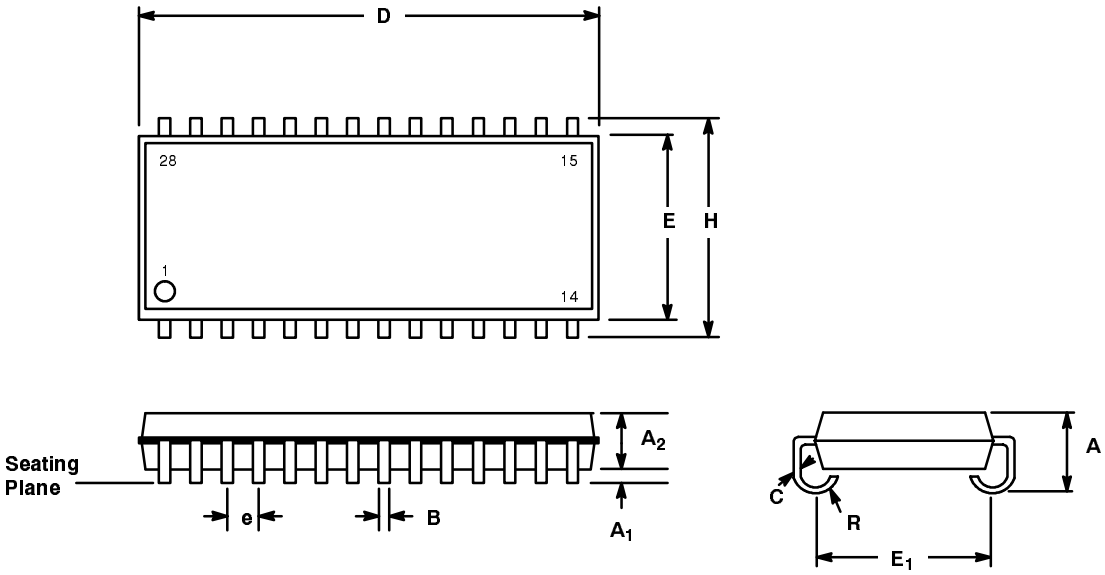


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.250	4.06	6.35
A_1	0.015	0.070	0.38	1.78
A_2	0.125	0.195	3.18	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.380	1.565	35.05	39.75
E	0.600	0.625	15.24	15.88
E_1	0.485	0.580	12.32	14.73
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	0.600	0.700	15.24	17.78
L	0.115	0.200	2.92	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

28 LEAD SMALL OUTLINE J LEAD (300 MIL JEDEC SOJ)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.200	3.60	5.08
A_1	0.025	---	0.64	---
A_2	0.120	0.140	3.05	3.56
B	0.014	0.020	0.36	0.51
C	0.008	0.013	0.20	0.30
D	0.697	0.712	17.70	18.08
E	0.292	0.300	7.42	7.62
E_1	0.262	0.272	6.65	6.91
e	0.050 BSC		1.27 BSC	
H	0.335	0.347	8.51	8.81
R	0.030	0.040	0.76	1.02

Note: The control dimension is the inch column

Notes

Notes

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