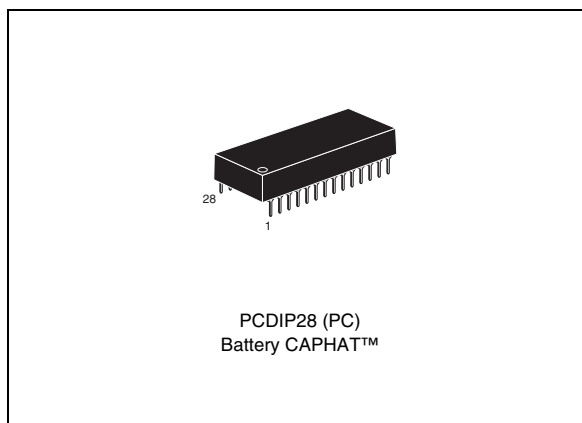

5 V, 64 Kbit (8 Kb x 8) ZEROPOWER[®] SRAM

Features

- Integrated, ultra low power SRAM and power-fail control circuit
- Unlimited WRITE cycles
- READ cycle time equals WRITE cycle time
- Automatic power-fail chip deselect and WRITE protection
- WRITE protect voltages (V_{PFD} = power-fail deselect voltage):
 - M48Z08: $V_{\text{CC}} = 4.75$ to 5.5 V
 4.5 V $\leq V_{\text{PFD}} \leq 4.75$ V
 - M48Z18: $V_{\text{CC}} = 4.5$ to 5.5 V
 4.2 V $\leq V_{\text{PFD}} \leq 4.5$ V
- Self-contained battery in the CAPHAT[™] DIP package
- Pin and function compatible with JEDEC standard 8 K x 8 SRAMs
- RoHS compliant
 - Lead-free second level interconnect



Contents

| | | |
|----------|---|-----------|
| 1 | Description | 5 |
| 2 | Operation modes | 7 |
| 2.1 | READ mode | 7 |
| 2.2 | WRITE mode | 8 |
| 2.3 | Data retention mode | 10 |
| 2.4 | V _{CC} noise and negative going transients | 11 |
| 3 | Maximum ratings | 12 |
| 4 | DC and AC parameters | 13 |
| 5 | Package mechanical data | 16 |
| 6 | Part numbering | 17 |
| 7 | Environmental information | 18 |
| 8 | Revision history | 19 |

List of tables

| | | |
|-----------|---|----|
| Table 1. | Signal names | 5 |
| Table 2. | Operating modes | 7 |
| Table 3. | READ mode AC characteristics | 8 |
| Table 4. | WRITE mode AC characteristics | 10 |
| Table 5. | Absolute maximum ratings | 12 |
| Table 6. | Operating and AC measurement conditions | 13 |
| Table 7. | Capacitance | 13 |
| Table 8. | DC characteristics | 14 |
| Table 9. | Power down/up AC characteristics | 15 |
| Table 10. | Power down/up trip points DC characteristics | 15 |
| Table 11. | PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package mech. data | 16 |
| Table 12. | Ordering information scheme | 17 |
| Table 13. | Document revision history | 19 |

List of figures

| | | |
|------------|--|----|
| Figure 1. | Logic diagram | 5 |
| Figure 2. | DIP connections | 6 |
| Figure 3. | Block diagram | 6 |
| Figure 4. | READ mode AC waveforms | 8 |
| Figure 5. | WRITE enable controlled, WRITE mode AC waveform | 9 |
| Figure 6. | Chip enable controlled, WRITE mode AC waveforms | 9 |
| Figure 7. | Supply voltage protection | 11 |
| Figure 8. | AC testing load circuit | 13 |
| Figure 9. | Power down/up mode AC waveforms | 14 |
| Figure 10. | PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package outline | 16 |
| Figure 11. | Recycling symbols | 18 |

1 Description

The M48Z08/18 ZEROPOWER® RAM is an 8 K x 8 non-volatile static RAM which is pin and function compatible with the DS1225.

The monolithic chip provides a highly integrated battery-backed memory solution.

The M48Z08/18 is a non-volatile pin and function equivalent to any JEDEC standard 8 K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28-pin, 600 mil DIP CAPHAT™ houses the M48Z08/18 silicon with a long-life lithium button cell in a single package.

Figure 1. Logic diagram

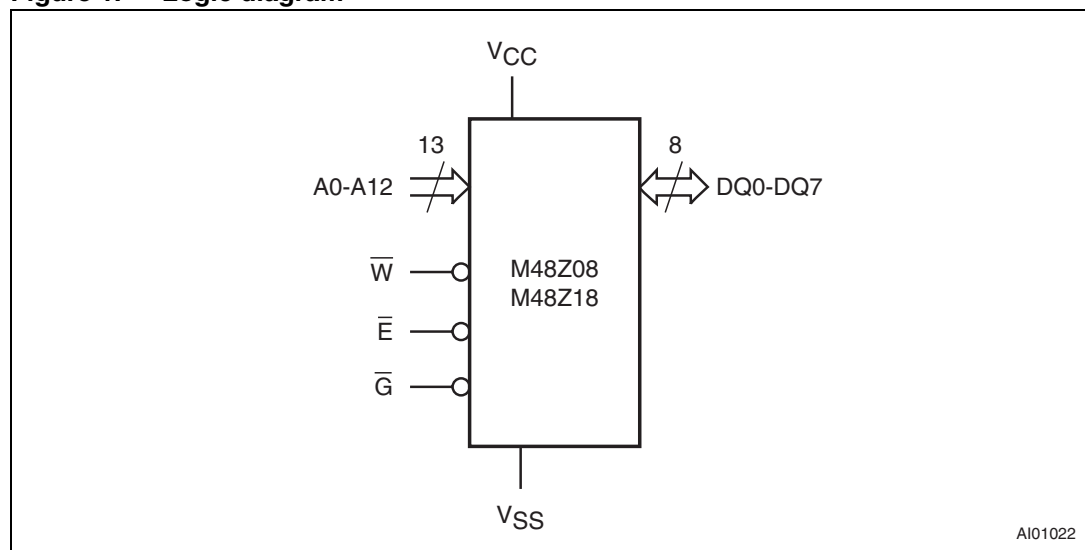


Table 1. Signal names

| | |
|-----------------|--------------------------|
| A0-A12 | Address inputs |
| DQ0-DQ7 | Data inputs / outputs |
| \bar{E} | Chip enable |
| \bar{G} | Output enable |
| \bar{W} | WRITE enable |
| V _{CC} | Supply voltage |
| V _{SS} | Ground |
| NC | Not connected internally |

Figure 2. DIP connections

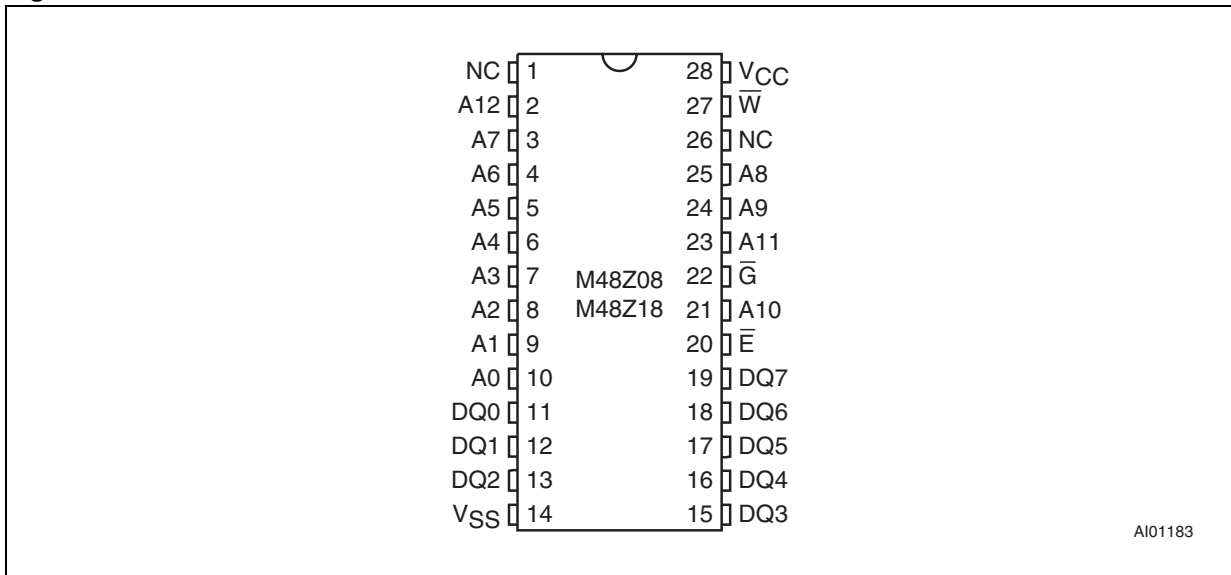
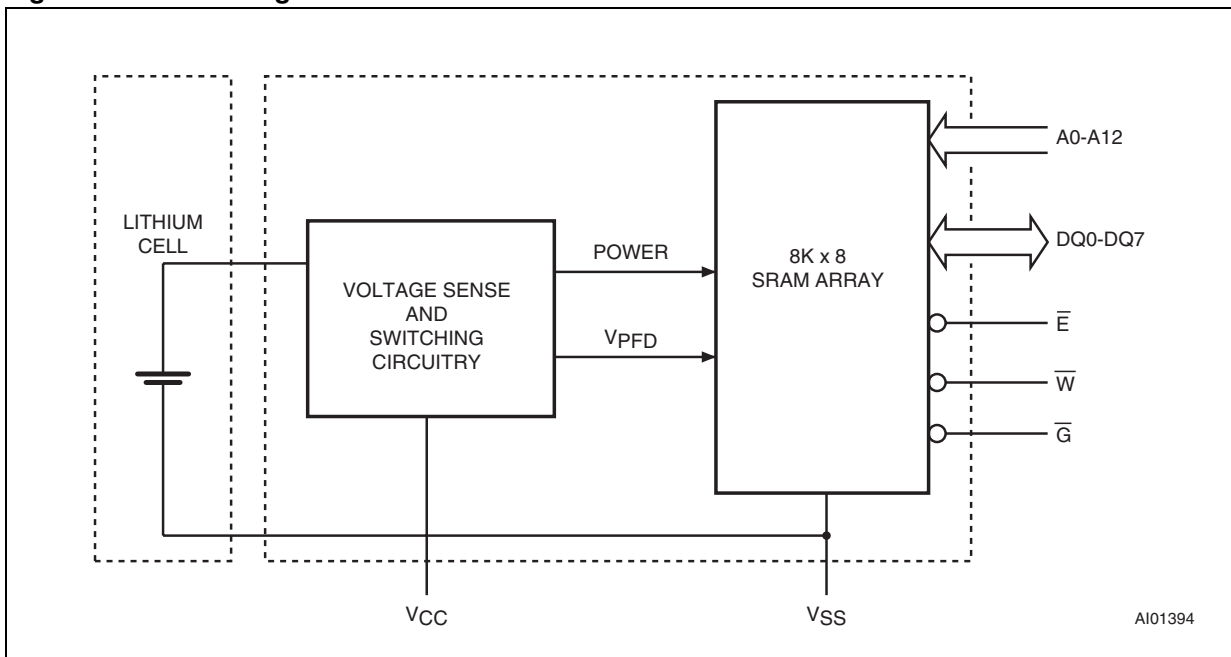


Figure 3. Block diagram



2 Operation modes

The M48Z08/18 also has its own power-fail detect circuit. The control circuitry constantly monitors the single 5 V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC} . As V_{CC} falls below approximately 3 V, the control circuitry connects the battery which maintains data until valid power returns.

Table 2. Operating modes

| Mode | V_{CC} | E | G | W | DQ0-DQ7 | Power |
|----------|-------------------------------------|----------|----------|----------|-----------|---------------------|
| Deselect | 4.75 to 5.5 V or 4.5 to 5.5 V | V_{IH} | X | X | High Z | Standby |
| WRITE | | V_{IL} | X | V_{IL} | D_{IN} | Active |
| READ | | V_{IL} | V_{IL} | V_{IH} | D_{OUT} | Active |
| READ | | V_{IL} | V_{IH} | V_{IH} | High Z | Active |
| Deselect | V_{SO} to $V_{PFD(min)}^{(1)}$ | X | X | X | High Z | CMOS standby |
| Deselect | $\leq V_{SO}^{(1)}$ | X | X | X | High Z | Battery backup mode |

1. See [Table 10 on page 15](#) for details.

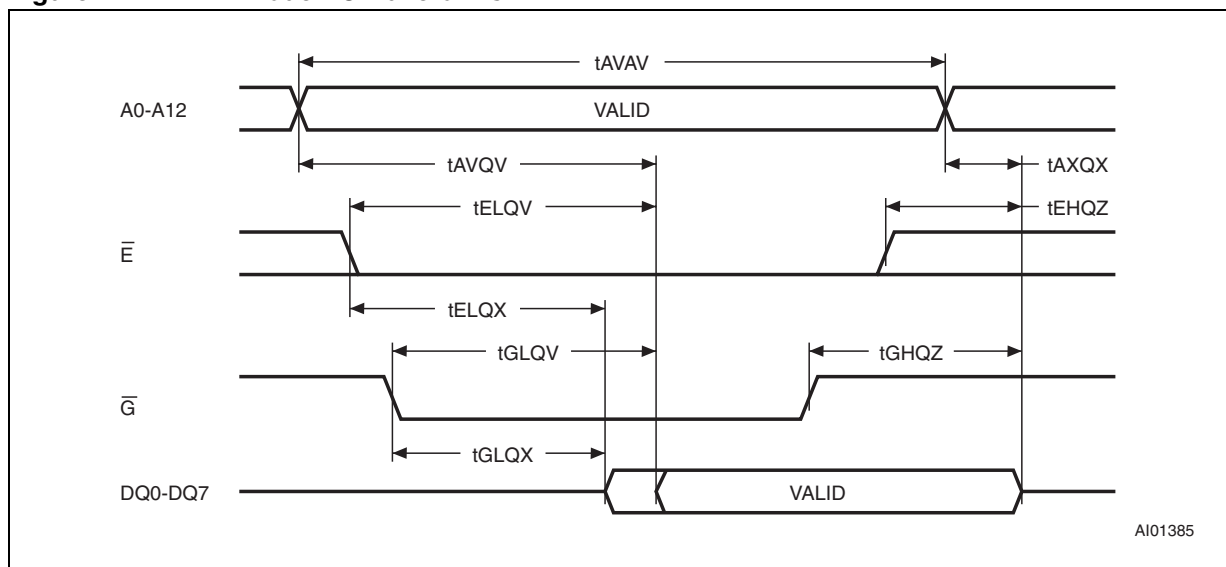
Note: $X = V_{IH}$ or V_{IL} ; V_{SO} = Battery backup switchover voltage.

2.1 READ mode

The M48Z08/18 is in the READ mode whenever \overline{W} (WRITE enable) is high and \overline{E} (chip enable) is low. The device architecture allows ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 address inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the \overline{E} and \overline{G} access times are also satisfied. If the \overline{E} and \overline{G} access times are not met, valid data will be available after the latter of the chip enable access time (t_{ELQV}) or output enable access time (t_{GLQV}).

The state of the eight three-state data I/O signals is controlled by \overline{E} and \overline{G} . If the outputs are activated before t_{AVQV} , the data lines will be driven to an indeterminate state until t_{AVQV} . If the address inputs are changed while \overline{E} and \overline{G} remain active, output data will remain valid for output data hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 4. READ mode AC waveforms



Note: WRITE enable (\bar{W}) = high.

Table 3. READ mode AC characteristics

| Symbol | Parameter ⁽¹⁾ | M48Z08/M48Z18 | | Unit |
|------------------|---|---------------|-----|------|
| | | Min | Max | |
| t_{AVAV} | READ cycle time | 100 | | ns |
| t_{AVQV} | Address valid to output valid | | 100 | ns |
| t_{ELQV} | Chip enable low to output valid | | 100 | ns |
| t_{GLQV} | Output enable low to output valid | | 50 | ns |
| $t_{ELQX}^{(2)}$ | Chip enable low to output transition | 10 | | ns |
| $t_{GLQX}^{(2)}$ | Output enable low to output transition | 5 | | ns |
| $t_{EHQZ}^{(2)}$ | Chip enable high to output Hi-Z | | 50 | ns |
| $t_{GHQZ}^{(2)}$ | Output enable high to output Hi-Z | | 40 | ns |
| t_{AXQX} | Address transition to output transition | 5 | | ns |

1. Valid for ambient operating temperature: $T_A = 0$ to 70 °C; $V_{CC} = 4.75$ to 5.5 V or 4.5 to 5.5 V (except where noted).

2. $C_L = 30$ pF.

2.2 WRITE mode

The M48Z08/18 is in the WRITE mode whenever \bar{W} and \bar{E} are active. The start of a WRITE is referenced from the latter occurring falling edge of \bar{W} or \bar{E} .

A WRITE is terminated by the earlier rising edge of \bar{W} or \bar{E} . The addresses must be held valid throughout the cycle. \bar{E} or \bar{W} must return high for a minimum of t_{EHAX} from chip enable or t_{WHAX} from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. \bar{G} should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on \bar{E} and \bar{G} , a low on \bar{W} will disable the outputs t_{WLQZ} after \bar{W} falls.

Figure 5. WRITE enable controlled, WRITE mode AC waveform

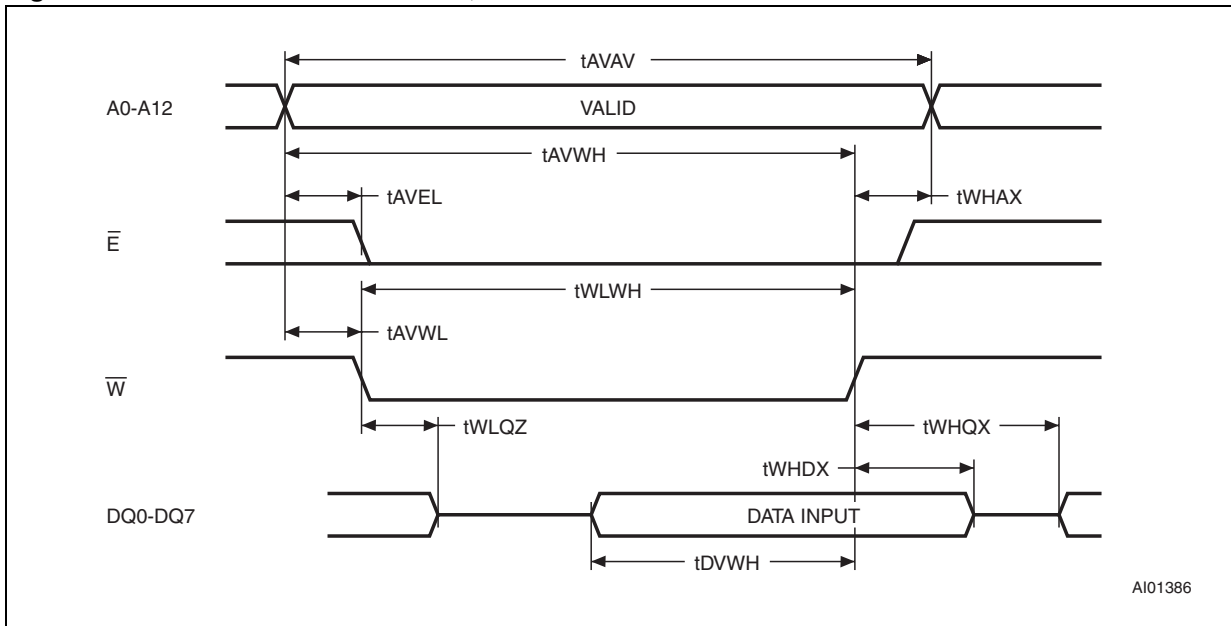


Figure 6. Chip enable controlled, WRITE mode AC waveforms

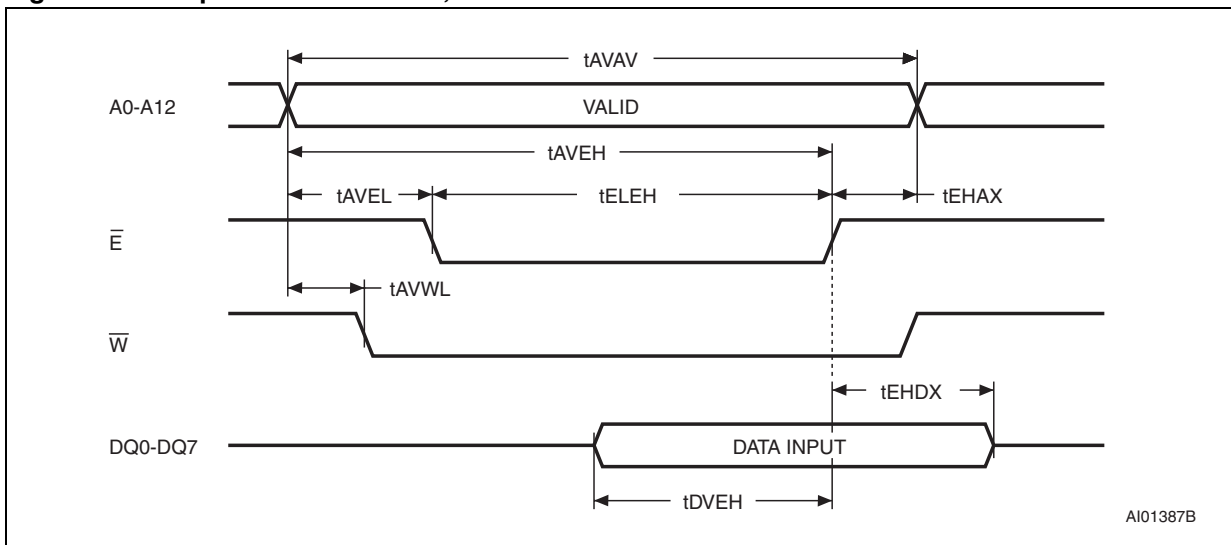


Table 4. WRITE mode AC characteristics

| Symbol | Parameter ⁽¹⁾ | M48Z08/M48Z18 | | Unit |
|-------------------------------------|---|---------------|-----|------|
| | | Min | Max | |
| t _{AVAV} | WRITE cycle time | 100 | | ns |
| t _{AVWL} | Address valid to WRITE enable low | 0 | | ns |
| t _{AVEL} | Address valid to chip enable 1 low | 0 | | ns |
| t _{WLWH} | WRITE enable pulse width | 80 | | ns |
| t _{ELEH} | Chip enable low to chip enable 1 high | 80 | | ns |
| t _{WHAX} | WRITE enable high to address transition | 10 | | ns |
| t _{EHAX} | Chip enable high to address transition | 10 | | ns |
| t _{DVWH} | Input valid to WRITE enable high | 50 | | ns |
| t _{DVEH} | Input valid to chip enable 1 high | 30 | | ns |
| t _{WHDX} | WRITE enable high to input transition | 5 | | ns |
| t _{EHDX} | Chip enable high to input transition | 5 | | ns |
| t _{WLQZ} ⁽²⁾⁽³⁾ | WRITE enable low to output Hi-Z | | 50 | ns |
| t _{AVWH} | Address valid to WRITE enable high | 80 | | ns |
| t _{AVEH} | Address valid to chip enable high | 80 | | ns |
| t _{WHQX} ⁽²⁾⁽³⁾ | WRITE enable high to output transition | 10 | | ns |

- Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
- C_L = 30 pF.
- If \bar{E} goes low simultaneously with \bar{W} going low, the outputs remain in the high impedance state.

2.3 Data retention mode

With valid V_{CC} applied, the M48Z08/18 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as “Don't care.”

Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z08/18 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z08/18 for an accumulated period of at least 11 years when V_{CC} is less than V_{SO}.

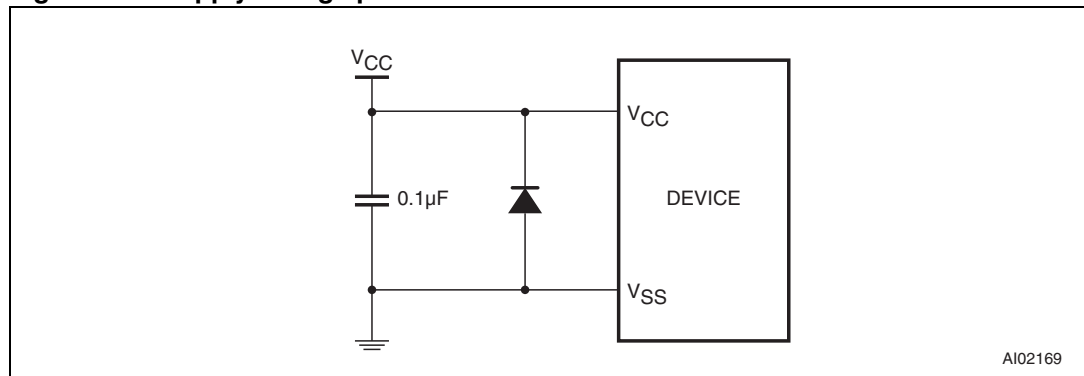
As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD} (min) plus t_{rec} (min). \bar{E} should be kept high as V_{CC} rises past V_{PFD} (min) to prevent inadvertent write cycles prior to system stabilization. Normal RAM operation can resume t_{rec} after V_{CC} exceeds V_{PFD} (max). For more information on battery storage life refer to the application note AN1012.

2.4 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of $0.1 \mu\text{F}$ (as shown in [Figure 7](#)) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a Schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC} , anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBR5120T3 is recommended for surface mount.

Figure 7. Supply voltage protection



3 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------------|---|-----------|------|
| T_A | Ambient operating temperature | 0 to 70 | °C |
| T_{STG} | Storage temperature (V_{CC} off, oscillator off) | -40 to 85 | °C |
| $T_{SLD}^{(1)}$ | Lead solder temperature for 10 seconds | 260 | °C |
| V_{IO} | Input or output voltages | -0.3 to 7 | V |
| V_{CC} | Supply voltage | -0.3 to 7 | V |
| I_O | Output current | 20 | mA |
| P_D | Power dissipation | 1 | W |

1. Soldering temperature of the IC leads is to not exceed 260 °C for 10 seconds. In order to protect the lithium battery, preheat temperatures must be limited such that the battery temperature does not exceed +85 °C. Furthermore, the devices shall not be exposed to IR reflow.

Caution: *Negative undershoots below -0.3 V are not allowed on any pin while in the battery backup mode.*

4 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 6. Operating and AC measurement conditions

| Parameter | M48Z08 | M48Z18 | Unit |
|---|-------------|------------|------|
| Supply voltage (V_{CC}) | 4.75 to 5.5 | 4.5 to 5.5 | V |
| Ambient operating temperature (T_A) | 0 to 70 | 0 to 70 | °C |
| Load capacitance (C_L) | 100 | 100 | pF |
| Input rise and fall times | ≤ 5 | ≤ 5 | ns |
| Input pulse voltages | 0 to 3 | 0 to 3 | V |
| Input and output timing ref. voltages | 1.5 | 1.5 | V |

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 8. AC testing load circuit

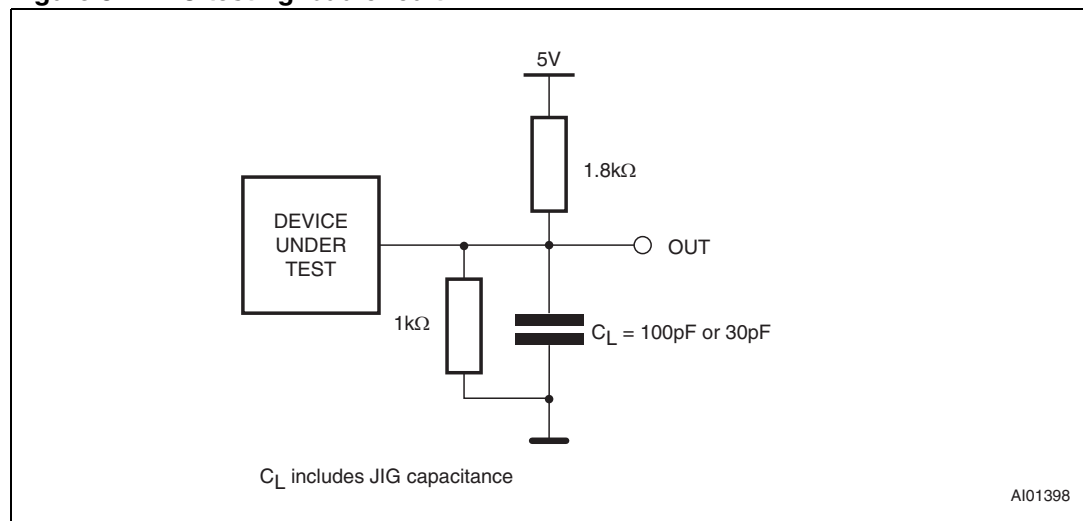


Table 7. Capacitance

| Symbol | Parameter ⁽¹⁾⁽²⁾ | Min | Max | Unit |
|----------------|-----------------------------|-----|-----|------|
| C_{IN} | Input capacitance | - | 10 | pF |
| $C_{IO}^{(3)}$ | Input / output capacitance | - | 10 | pF |

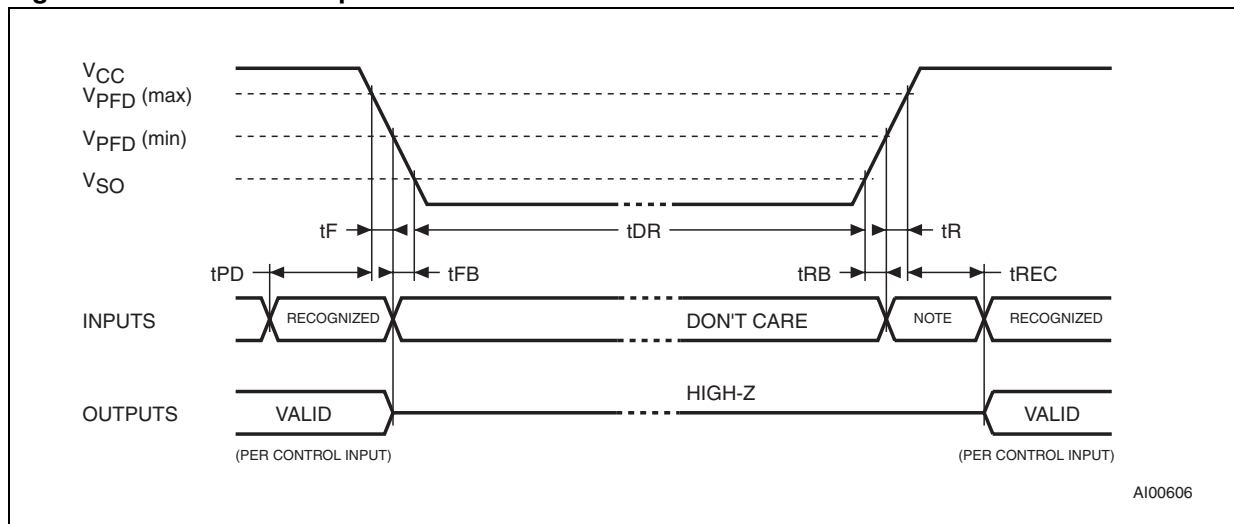
1. Effective capacitance measured with power supply at 5 V; sampled only, not 100% tested.
2. At 25 °C, $f = 1$ MHz.
3. Outputs deselected.

Table 8. DC characteristics

| Symbol | Parameter | Test condition ⁽¹⁾ | Min | Max | Unit |
|----------------|-------------------------------|---------------------------------------|------|----------------|---------------|
| I_{LI} | Input leakage current | $0\text{ V} \leq V_{IN} \leq V_{CC}$ | | ± 1 | μA |
| $I_{LO}^{(2)}$ | Output leakage current | $0\text{ V} \leq V_{OUT} \leq V_{CC}$ | | ± 1 | μA |
| I_{CC} | Supply current | Outputs open | | 80 | mA |
| I_{CC1} | Supply current (standby) TTL | $\bar{E} = V_{IH}$ | | 3 | mA |
| I_{CC2} | Supply current (standby) CMOS | $\bar{E} = V_{CC} - 0.2\text{ V}$ | | 3 | mA |
| V_{IL} | Input low voltage | | -0.3 | 0.8 | V |
| V_{IH} | Input high voltage | | 2.2 | $V_{CC} + 0.3$ | V |
| V_{OL} | Output low voltage | $I_{OL} = 2.1\text{ mA}$ | | 0.4 | V |
| V_{OH} | Output high voltage | $I_{OH} = -1\text{ mA}$ | 2.4 | | V |

- Valid for ambient operating temperature: $T_A = 0$ to $70\text{ }^\circ\text{C}$; $V_{CC} = 4.75$ to 5.5 V or 4.5 to 5.5 V (except where noted)
- Outputs deselected.

Figure 9. Power down/up mode AC waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep \bar{E} high as V_{CC} rises past V_{PPFD} (min). Some systems may perform inadvertent WRITE cycles after V_{CC} rises above V_{PPFD} (min) but before normal system operations begin. Even though a power on reset is being applied to the processor, a reset condition may not occur until after the system is running.

Table 9. Power down/up AC characteristics

| Symbol | Parameter ⁽¹⁾ | Min | Max | Unit |
|----------------|--|-----|-----|---------|
| t_{PD} | \overline{E} or \overline{W} at V_{IH} before power down | 0 | - | μs |
| $t_F^{(2)}$ | V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time | 300 | - | μs |
| $t_{FB}^{(3)}$ | V_{PFD} (min) to V_{SS} V_{CC} fall time | 10 | - | μs |
| t_R | V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time | 0 | - | μs |
| t_{RB} | V_{SS} to V_{PFD} (min) V_{CC} rise time | 1 | - | μs |
| t_{rec} | \overline{E} or \overline{W} at V_{IH} before power-up | 2 | - | ms |

- Valid for ambient operating temperature: $T_A = 0$ to 70 °C; $V_{CC} = 4.75$ to 5.5 V or 4.5 to 5.5 V (except where noted).
- V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until $200 \mu s$ after V_{CC} passes V_{PFD} (min).
- V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 10. Power down/up trip points DC characteristics

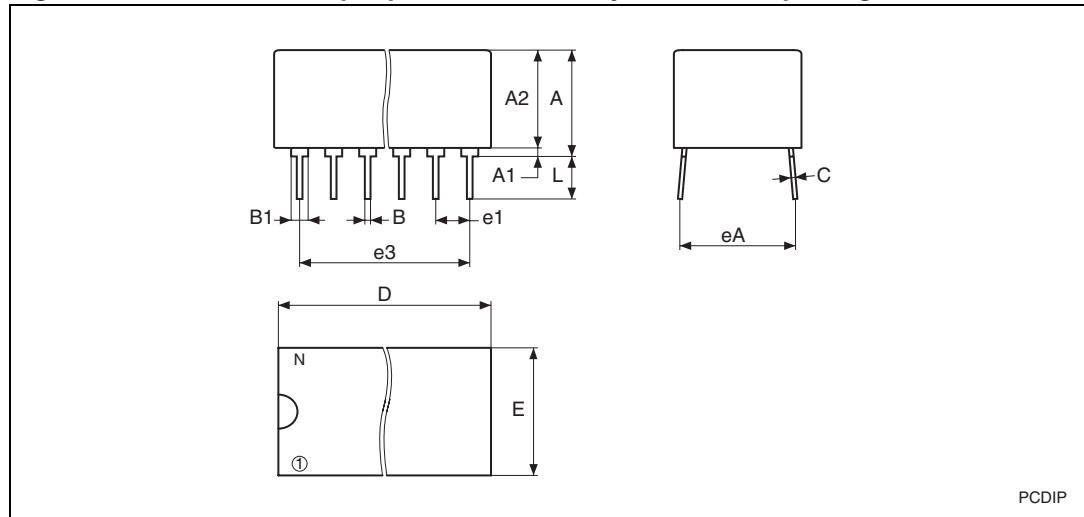
| Symbol | Parameter ⁽¹⁾⁽²⁾ | Min | Typ | Max | Unit | |
|----------------|-----------------------------------|--------|-----|-----|-------|---|
| V_{PFD} | Power-fail deselect voltage | M48Z08 | 4.5 | 4.6 | 4.75 | V |
| | | M48Z18 | 4.2 | 4.3 | 4.5 | V |
| V_{SO} | Battery backup switchover voltage | | 3.0 | | V | |
| $t_{DR}^{(3)}$ | Expected data retention time | 11 | | | Years | |

- All voltages referenced to V_{SS} .
- Valid for ambient operating temperature: $T_A = 0$ to 70 °C; $V_{CC} = 4.75$ to 5.5 V or 4.5 to 5.5 V (except where noted).
- At 25 °C, $V_{CC} = 0$ V.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark

Figure 10. PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package outline



Note: Drawing is not to scale.

Table 11. PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package mech. data

| Symb | mm | | | inches | | |
|------|-------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 8.89 | 9.65 | | 0.350 | 0.380 |
| A1 | | 0.38 | 0.76 | | 0.015 | 0.030 |
| A2 | | 8.38 | 8.89 | | 0.330 | 0.350 |
| B | | 0.38 | 0.53 | | 0.015 | 0.021 |
| B1 | | 1.14 | 1.78 | | 0.045 | 0.070 |
| C | | 0.20 | 0.31 | | 0.008 | 0.012 |
| D | | 39.37 | 39.88 | | 1.550 | 1.570 |
| E | | 17.83 | 18.34 | | 0.702 | 0.722 |
| e1 | | 2.29 | 2.79 | | 0.090 | 0.110 |
| e3 | 33.02 | | | 1.3 | | |
| eA | | 15.24 | 16.00 | | 0.600 | 0.630 |
| L | | 3.05 | 3.81 | | 0.120 | 0.150 |
| N | | 28 | | | 28 | |

6 Part numbering

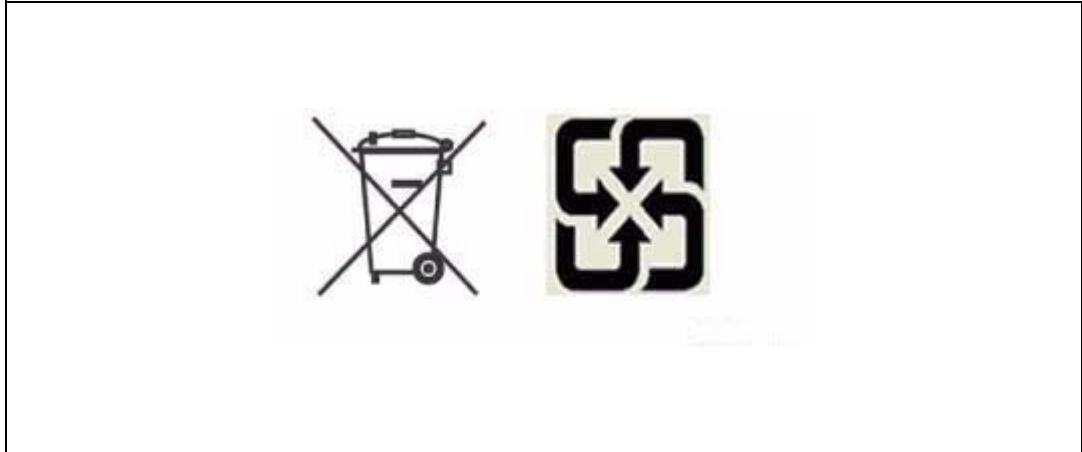
Table 12. Ordering information scheme

| Example: | M48Z | 08 | -100 | PC | 1 | TR |
|---|------|--|---------------|--------------|----------------|---|
| Device Type | M48Z | | | | | |
| Supply voltage and write protect voltage | | 08 = $V_{CC} = 4.75$ to 5.5 V; $V_{PFD} = 4.5$ to 4.75 V 18 = $V_{CC} = 4.5$ to 5.5 V; $V_{PFD} = 4.2$ to 4.5 V | | | | |
| Speed | | | -100 = 100 ns | | | |
| Package | | | | PC = PCDIP28 | | |
| Temperature range | | | | | 1 = 0 to 70 °C | |
| Shipping method | | | | | | blank = ECOPACK® package, tubes TR = ECOPACK® package, tape & reel |

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

7 Environmental information

Figure 11. Recycling symbols



This product contains a non-rechargeable lithium (lithium carbon monofluoride chemistry) button cell battery fully encapsulated in the final product.

Recycle or dispose of batteries in accordance with the battery manufacturer's instructions and local/national disposal and recycling regulations.

Please refer to the following web site address for additional information regarding compliance statements and waste recycling.

Go to www.st.com/nvram, then select "Lithium Battery Recycling" from "Related Topics".

8 Revision history

Table 13. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| Mar-1999 | 1 | First issue |
| 19-Jul-2001 | 2 | 2-socket SOH and 2-pin SH packages removed; reformatted; temperature information added to tables (Table 7 , 8 , 3 , 4 , 9 , 10) |
| 19-Dec-2001 | 2.1 | Remove all references to “clock” |
| 21-Dec-2001 | 2.2 | Changes to text to reflect addition of M48Z08Y option |
| 20-May-2002 | 2.3 | Modify reflow time and temperature footnotes (Table 5) |
| 10-Sep-2002 | 2.4 | Remove all references to “SNAPHAT” and M48Z08Y part (Figure 1 ; Table 5 , 6 , 3 , 4 , 10 , 12) |
| 01-Apr-2003 | 3 | v2.2 template applied; updated test condition (Table 10) |
| 28-Aug-2004 | 4 | Reformatted; removed references to ‘crystal’ (Figure 1) |
| 14-Dec-2005 | 5 | Updated template, Lead-free text, removed footnote (Table 8 , 12) |
| 24-Mar-2009 | 6 | Reformatted document; added text to Section 5: Package mechanical data ; added Section 7: Environmental information . |
| 27-May-2010 | 7 | Updated Section 3: Maximum ratings , Table 11 ; reformatted document; minor textual changes. |

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