MAX17620

4MHz, Miniature 600mA, Synchronous Step-Down DC-DC Converter with Integrated MOSFETs

General Description

The MAX17620 is a high-frequency, high-efficiency synchronous step-down DC-DC converter with integrated MOSFETs that operates over a 2.7V to 5.5V input voltage range. The device supports up to 600mA load current and 1.5V to 100% V_{IN} output voltage. High-frequency operation enables the use of small, low-cost inductors and capacitors.

The device features selectable PWM/skip mode of operation at light loads and operates at a 4MHz fixed-frequency in PWM mode. Skip mode improves system efficiency at light loads, while PWM mode maintains a constant switching frequency over the entire load. In skip mode, the device draws only 40µA of quiescent current from the supply input. In shutdown mode, the current consumption is reduced to 0.1µA.

The device also features a soft-start feature to reduce the inrush current during startup, and also incorporates an enable (EN) pin to turn on/off the device. An open-drain PGOOD pin provides power-good signal to the system upon achieving successful regulation of the output voltage.

The MAX17620 is available in an 8-pin, 2mm x 2mm TDFN package and operates over the -40°C to +125°C temperature range.

Applications

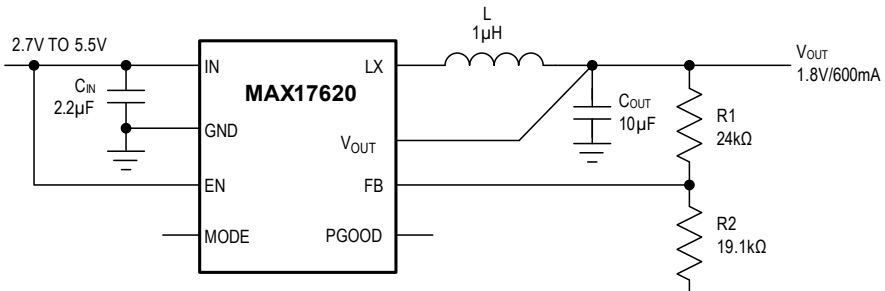
- Point-of-Load Power Supply
- Standard 5V Rail Supplies
- Battery-Powered Instruments
- Distributed Power Systems

Benefits and Features

- Minimizes External Components, Reducing Total Cost
  - Synchronous Operation for High Efficiency and Reduced Cost
  - Internal Compensation for Stable Operation at Any Output Voltage
  - All-Ceramic Capacitor Solution
  - 4MHz Operation
  - Only 5 External Components Required
  - Total Solution Size is 12mm^2 (Sum of the Components Area)
- Reduces Number of DC-DC Regulators to Stock
  - Wide 2.7V to 5.5V Input Voltage Range
  - Adjustable 1.5V to 100% V_{IN} Output Voltage Range
  - Delivers Up to 600mA Load Current
  - 100% Duty-Cycle Operation
  - +1%/-0.75% Reference Voltage Accuracy
  - Available in a 2mm x 2mm TDFN Package
- Reduces Power Dissipation
  - Peak Efficiency 91%
  - Skip Mode for High Light-Load Efficiency
  - Shutdown Current = 0.1µA
- Operates Reliably
  - Peak Current-Limit Protection
  - Soft-Start Reduces Inrush Current During Startup
  - Built-In Output-Voltage Monitoring (Open-Drain PGOOD Pin)
  - -40°C to +125°C Operation

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit—1.8V, 600mA Step-Down Regulator



C_{IN}: 2.2µF/10V/0603/X7R,GRM188R71A225KE15D, MURATA
L1: 1µH, 60mΩ, MAKK2016H1ROM, TAIYO-YUDEN
C_{OUT}: 10µF/6.3V/0805/X7R, GRM21BR70J106KE76K, MURATA

maxim integrated™

Absolute Maximum Ratings

IN to GND ..... -0.3V to 6V
LX to GND ..... -0.3V to 6V
MODE ..... -0.3V to V_{IN} + 0.3V
EN, PGOOD, FB, V_{OUT} to GND ..... -0.3V to 6V
Continuous Power Dissipation (up to T_A = +70°C)
(derate 9.8mW/°C above T_A = +70°C) 784.3mW

Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (Reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 102°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

V_{IN} = +3.6V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = T_J = +25°C. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)						
Input Voltage Range	V_{IN}		2.7		5.5	V
Input Supply Current	I_{IN-SH}	V_{EN} = 0V, shutdown mode		0.1		µA
	I_{Q_SKIP}	Nonswitching		40		µA
	I_{Q-PWM}	PWM mode (switching)		6		mA
Undervoltage-Lockout Threshold (UVLO)	V_{IN_UVLO}	V_{IN} rising	2.55	2.6	2.65	V
UVLO Hysteresis	$V_{IN_UVLO_HYS}$			200		mV
ENABLE (EN)						
EN Low Threshold	V_{EN_LOW}	V_{EN} falling			0.8	V
EN High Threshold	V_{EN_HIGH}	V_{EN} rising	2			V
EN Hysteresis	V_{EN_HYS}			220		mV
EN Input Leakage	I_{EN}	V_{EN} = 5.5V, T_A = T_J = +25°C		10	50	nA
POWER MOSFETS						
High-Side pMOS On-Resistance	R_{DS-ONH}	V_{IN} = 3.6V, I_{LX} = 190mA		120	200	mΩ
High-Side pMOS On-Resistance	R_{DS-ONH}	V_{IN} = 5.0V, I_{LX} = 190mA		100	160	mΩ
Low-Side nMOS On-Resistance	R_{DS-ONL}	V_{IN} = 3.6V, I_{LX} = 190mA		80	145	mΩ
Low-Side nMOS On-Resistance	R_{DS-ONL}	V_{IN} = 5.0V, I_{LX} = 190mA		70	130	mΩ
LX Leakage Current	I_{LX_LKG}	LX = GND or IN, T_A = +25°C		0.1	1	µA
High-Side Peak Current Limit	I_{LIM_PEAK}		1150	1450	1800	mA
Low-Side Valley Current Limit	I_{LIM_VALLEY}		920	1170	1450	mA
Low-Side Negative Current Limit	I_{LIM_NEG}	Current entering into LX pin		1050		mA
Low-Side Zero-Crossing Current Limit	I_{LIM_ZX}	MODE = IN, current leaving out of LX pin		100		mA

Electrical Characteristics (continued)

V_{IN} = +3.6V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = T_J = +25°C. (Note 2)

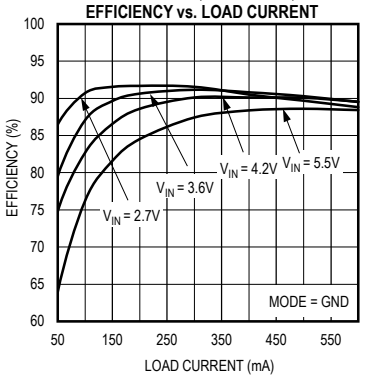
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING FREQUENCY						
Switching Frequency	f_{SW}	MODE = GND	3.84	4	4.16	MHz
Minimum Controllable On-Time	t_{ON_MIN}			40		ns
LX Dead Time				3		ns
Soft-Start Time	t_{SS}	t_{SS} = 4096 CLK cycles		1		ms
FEEDBACK (FB)						
FB Voltage Accuracy	V_{FB}	PWM mode	-0.75		+1	%
FB Input Bias Current	I_{FB}	FB = 0.6V, T_A = T_J = 25°C		50	120	nA
POWER GOOD (PGOOD)						
PGOOD Rising Threshold		FB rising	91.5	93.5	95.5	%
PGOOD Falling Threshold		FB falling	88	90	92	%
PGOOD Output Low		I_{PGOOD} = 5mA			200	mV
PGOOD Output Leakage Current	I_{PGOOD_LKG}	PGOOD = 5.5V, T_A = T_J = 25°C			100	nA
MODE						
MODE Pullup Current		V_{MODE} = GND		5		µA
THERMAL SHUTDOWN						
Thermal-Shutdown Rising Threshold		Temperature rising		165		°C
Thermal-Shutdown Hysteresis				10		°C

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

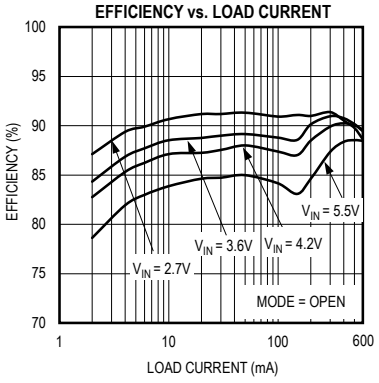
Typical Operating Characteristics

(See the Typical Application Circuits, T_A = +25°C, V_{IN} = 3.6V, unless otherwise noted.)

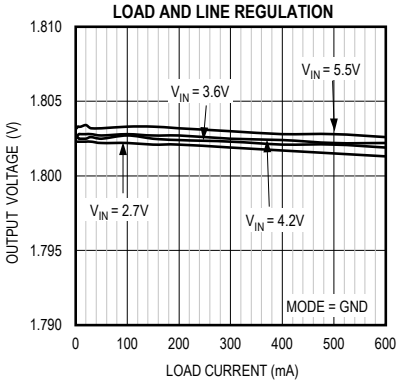
1.8V OUTPUT, PWM MODE, EFFICIENCY vs. LOAD CURRENT



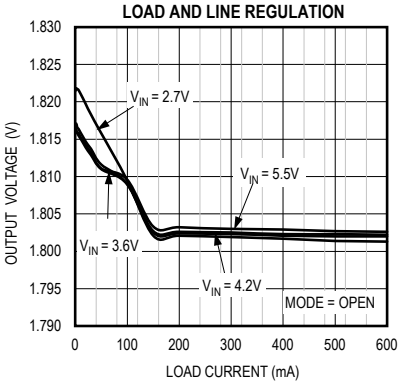
1.8V OUTPUT, SKIP MODE, EFFICIENCY vs. LOAD CURRENT



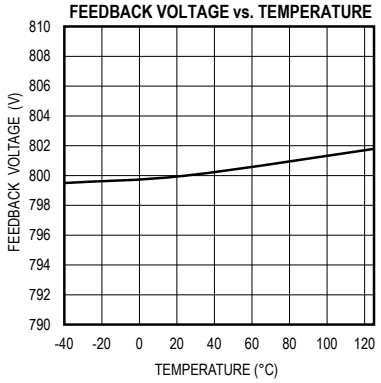
1.8V OUTPUT, PWM MODE, LOAD AND LINE REGULATION



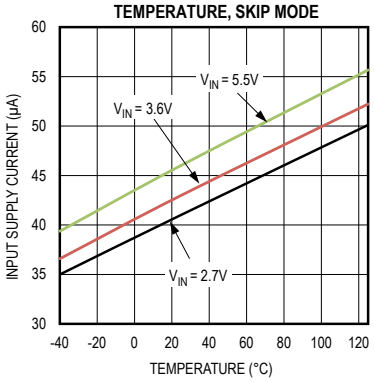
1.8V OUTPUT, SKIP MODE, LOAD AND LINE REGULATION



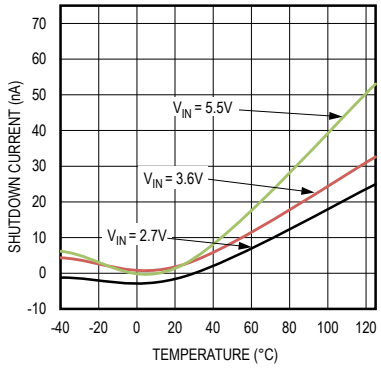
FEEDBACK VOLTAGE vs. TEMPERATURE



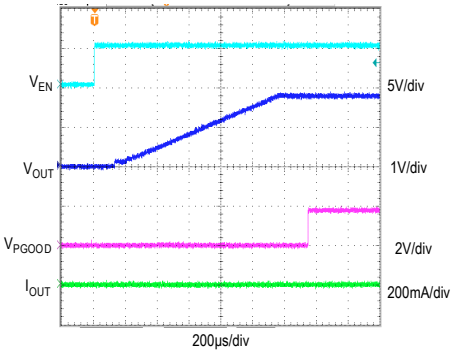
INPUT SUPPLY CURRENT vs. TEMPERATURE, SKIP MODE



SHUTDOWN CURRENT vs. TEMPERATURE



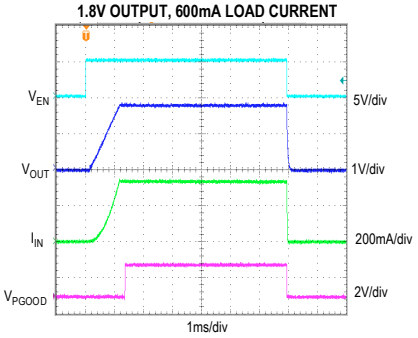
SOFT-START FROM EN, PWM MODE, 1.8V OUTPUT, NO LOAD CURRENT



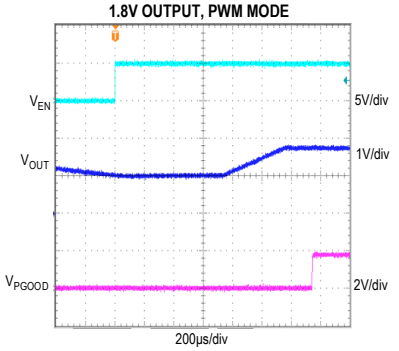
Typical Operating Characteristics (continued)

(See the Typical Application Circuits, T_A = +25°C, V_{IN} = 3.6V, unless otherwise noted.)

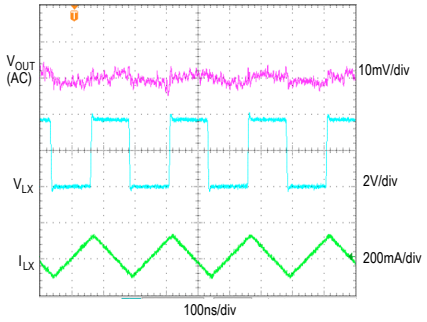
SOFT-START/SHUTDOWN FROM EN, 1.8V OUTPUT, 600mA LOAD CURRENT



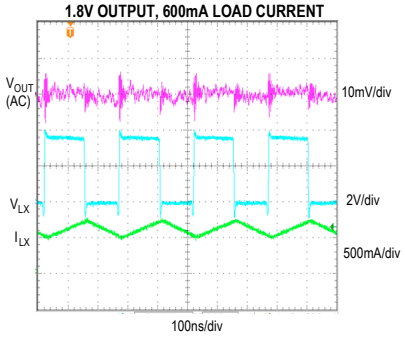
SOFT-START WITH 1V PREBIAS, 1.8V OUTPUT, PWM MODE



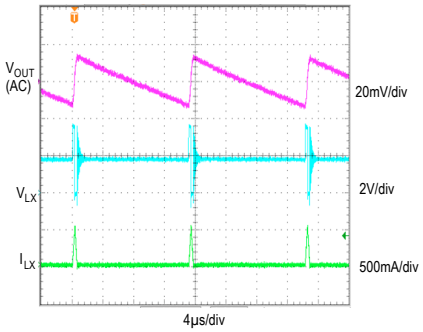
STEADY-STATE SWITCHING WAVEFORMS, 1.8V OUTPUT, NO LOAD, PWM MODE



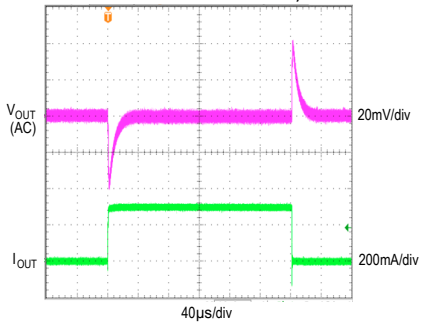
STEADY-STATE SWITCHING WAVEFORMS, 1.8V OUTPUT, 600mA LOAD CURRENT



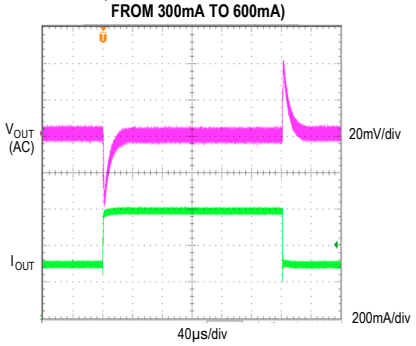
STEADY-STATE SWITCHING WAVEFORMS, 1.8V OUTPUT, 10mA LOAD, SKIP MODE



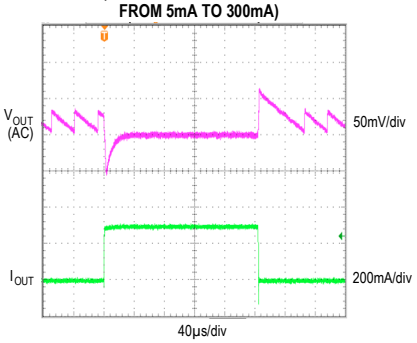
1.8V OUTPUT, PWM MODE, (LOAD CURRENT STEPPED FROM NO LOAD TO 300mA)



1.8V OUTPUT, (LOAD CURRENT STEPPED FROM 300mA TO 600mA)



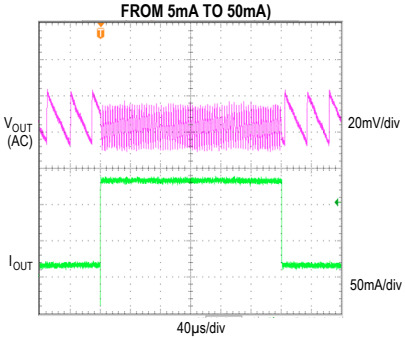
1.8V OUTPUT, SKIP MODE, (LOAD CURRENT STEPPED FROM 5mA TO 300mA)



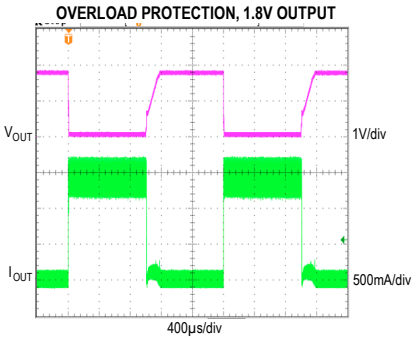
Typical Operating Characteristics (continued)

(See the Typical Application Circuits, T_A = +25°C, V_{IN} = 3.6V, unless otherwise noted.)

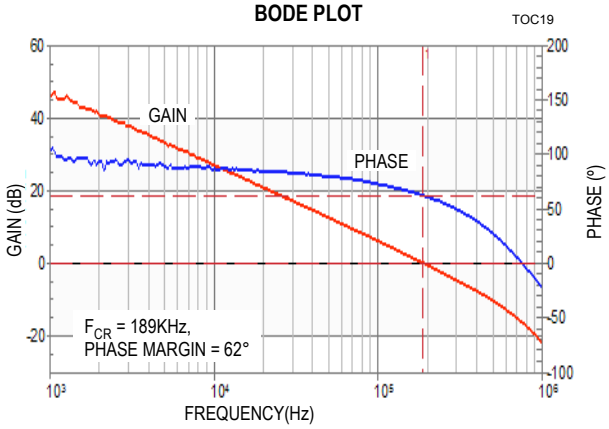
1.8V OUTPUT, SKIP MODE, (LOAD CURRENT STEPPED FROM 5mA TO 50mA)



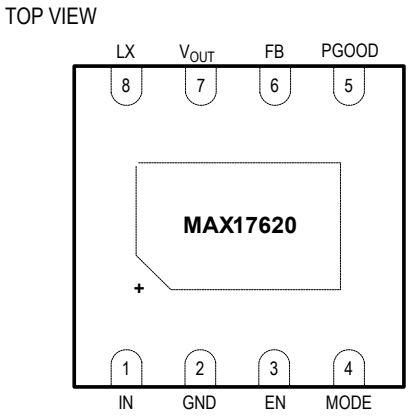
OVERLOAD PROTECTION, 1.8V OUTPUT



BODE PLOT



Pin Configuration

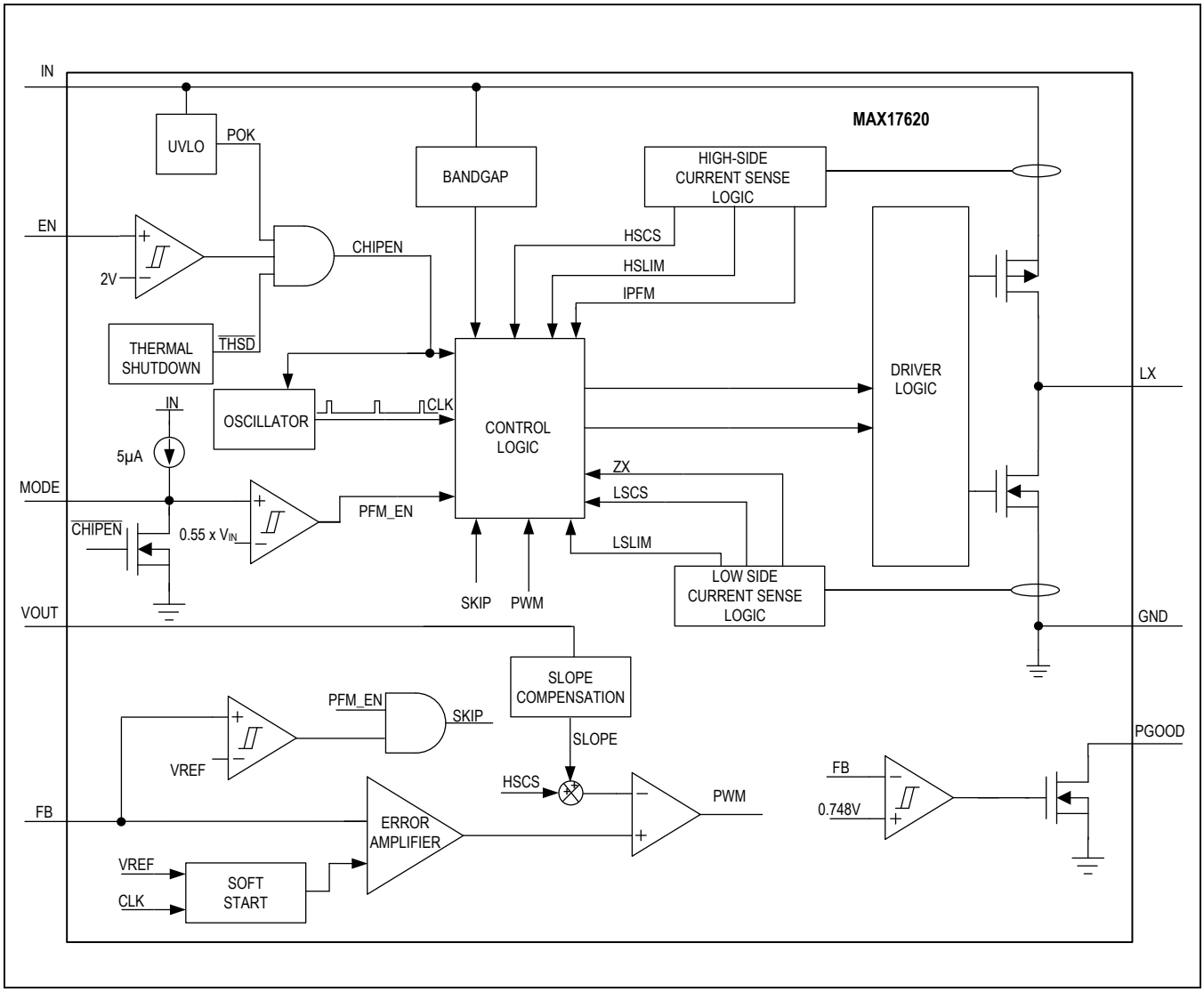


TDFN
(2mm x 2mm)

Pin Description

PIN	NAME	FUNCTION
1	IN	Power Supply Input. Connect a minimum 1µF ceramic capacitor from IN to GND for bypassing high-frequency noise on IN pin to ground.
2	GND	Ground Pin. Connect to system ground.
3	EN	Enable Input. Logic-high voltage on EN pin enables the device, while logic-low voltage disables the device.
4	MODE	PWM or Skip Mode Selection Input. Connect the MODE pin to GND to enable PWM mode operation. Leave the MODE pin unconnected to enable skip mode operation.
5	PGOOD	Open-Drain Power Good Output. Connect PGOOD pin to output voltage or IN pin through an external pullup resistor to generate a “high” level if the output voltage is above 93% of the target regulated voltage. If not used, leave this pin unconnected. The PGOOD is driven low if the output voltage is below 90% of the target regulated voltage.
6	FB	Feedback Input. Connect FB to the center of the external resistor-divider from output to GND to set the output voltage.
7	V_{OUT}	Output Voltage Input. Connect the positive terminal of the output voltage to the V_{OUT} pin.
8	LX	Switching Node. Connect LX pin to the switching node of the inductor.
—	EP	Exposed Pad. Connect exposed pad to the system ground.

Block Diagram



Detailed Description

The MAX17620 is a high-frequency, high-efficiency synchronous step-down DC-DC converter with integrated MOSFETs that operates over a 2.7V to 5.5V input voltage range. The device supports up to 600mA load current and 1.5V to 100% V_{IN} output voltage. High-frequency operation allows the use of small, low-cost inductors and capacitors.

The device features a MODE pin to set the device to operate in PWM or skip mode under light-load conditions. In PWM Mode, the device operates with its nominal switching frequency of 4MHz over entire load current range. In skip mode, the device skips some cycles at light loads thereby reducing the switching frequency and achieving high efficiency. The device features a soft-start, open-drain power-good signal (PGOOD) and enable input (EN).

Control Architecture

The device uses an internally compensated, peak-current-mode-control architecture. The high-side MOSFET is turned on at each clock edge and the low-side MOSFET is turned off. The high-side MOSFET remains on until the sum of the high-side MOSFET current-sense voltage and the internal slope compensating ramp voltage hits the control voltage generated by the error amplifier. At this moment, the high-side MOSFET is turned off and the low-side MOSFET is turned on.

During the high-side MOSFET on-time, the inductor current ramps up and stores energy. During the low-side MOSFET on-time, the inductor current ramps down and releases the stored energy to the output.

Enable Input (EN)

The device is enabled by setting the EN pin to a logic-high. Accordingly, a logic-low disables the device. When the device is enabled, an internal soft-start circuitry monotonically ramps up the error amplifier's reference voltage from 0 to 0.8V in fixed soft-start time of 1ms. This causes the output voltage to ramp monotonically from 0V to set voltage. It also avoids excessive inrush current and prevents excessive voltage drop of batteries with high internal impedance.

Driving EN low disables the switching and output is discharged with a typical discharge resistor of 225Ω. The same happens when the device gets disabled by thermal shutdown or undervoltage-lockout trigger.

Mode Selection (MODE)

The device can be set to operate in either PWM mode or skip mode under light-load conditions by connecting the MODE pin to ground or leaving it unconnected. Connecting the MODE pin to ground sets the device to PWM mode and leaving it unconnected sets the device to skip mode.

In PWM mode, the device operates with its nominal switching frequency of 4MHz over the entire load current range and the inductor current is allowed to go negative. PWM mode is useful in applications where constant switching frequency is desired.

In skip mode, the device skips pulses at light loads for high efficiency and the inductor current is not allowed to go negative. In this mode, when the output voltage falls below the target value, the internal high-side MOSFET is turned on until the inductor current reaches to peak current threshold in skip mode. Once the high-side FET is turned off, the low-side FET is turned on until the inductor current falls to zero. The device enters into PWM mode if the output voltage is below the target voltage during the next 3 clock cycles after the inductor current falls to zero. If the output voltage is above the target value during the next 3 clock cycles, then both the high-side and low-side FETs are turned off and the device enters hibernation mode until the load discharges the output below the target value.

The peak current threshold in skip mode is a function of the output inductor and is (375/L)mA, where L is the output inductor value in µH. The advantage of the skip mode is higher efficiency at light loads because of lower quiescent current drawn from the supply. The disadvantage is that the output-voltage ripple is higher compared to that of the PWM mode operation and the switching frequency is not constant at light loads. The device always operates in skip mode during soft-start under light loads independent of the MODE pin status. The peak current threshold in skip mode during soft-start is reduced to 50% of the value during steady-state operation.

Power-Good Indicator (PGOOD)

The device includes an open-drain power good output that indicates the output voltage status. PGOOD goes high impedance when the output voltage is above 93.5% of the target value, and goes low when the output voltage is below 90% of the target value.

Startup Into a Prebiased Output

The device is capable of soft-starting into a prebiased output without discharging the output. The device ramps up the output voltage monotonically from the prebiased level to the target level during the soft-start period if the prebiased voltage is less than the target output voltage. If the prebiased voltage is more than the target output voltage, no switching happens during the soft-start period. The device operation after the completion of the soft-start period under prebiased output condition (where the prebiased voltage is higher than the target output voltage) depends on the PWM/skip mode. In PWM Mode, the device tries to regulate the output voltage to the target level by sinking current from the prebiased source. In skip mode, the device does not initiate switching until the output voltage falls below the target output voltage.

100% Duty-Cycle Operation

The device can provide 100% duty-cycle operation. In this mode, the high-side switch is constantly turned on, while the low-side switch is turned off. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery-voltage range. The minimum input voltage to maintain the output-voltage regulation can be calculated as:

$$V_{IN_MIN} = V_{OUT} + (I_{OUT} \times R_{ON})$$

where,

V_{IN_MIN} is the minimum input voltage

V_{OUT} is the target output voltage

I_{OUT} is the load current

R_{ON} is the sum of the high-side FET on-resistance and the output inductor DCR

Undervoltage Lockout

The device features an integrated input undervoltage lockout (UVLO) feature that turns the device on/off based on the voltage at the IN pin. The device turns on if the IN pin voltage is higher than the UVLO threshold (V_{IN_UVLO}) of 2.6V (typ) (assuming EN is at logic-high) and turns off when the IN pin voltage is 200mV ($V_{IN_UVLO_HYS}$) below the V_{IN_UVLO}.

Overcurrent Protection

The device features a robust overcurrent-protection scheme that protects the device and inductor under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET and turns on the low-side MOSFET whenever the high-side MOSFET current exceeds the internal peak current limit of 1.45A (typ). The low-side MOSFET remains on until the next clock cycle. The high-side MOSFET is turned on again, if the inductor current is less than the valley current limit at the next clock rising edge. Otherwise, the low-side MOSFET is kept on for the next clock cycle as well. Under severe overload conditions, the current will not exceed 1.45A. If the overload condition is removed, the part recovers smoothly to target output voltage with no overshoot.

Thermal Shutdown

Thermal-shutdown protection limits the total power dissipation in the device. When the device junction temperature exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing it to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C.

Applications information

Inductor Selection

Three key inductor parameters must be specified to select output inductor:

1) Inductor value

2) Inductor saturation current

3) DC resistance of the Inductor

The device's internal slope compensation and current limit are optimized for 1µH output inductor. Select 1µH inductor with a saturation current rating higher than the maximum peak current limit of 1.9A. Inductor with low DC resistance improves the efficiency of the system. Selecting ferrite-cored inductors reduces the core losses and improves efficiency. Table 1 lists recommended inductors for use in designs.

Output Capacitor Selection

X7R ceramic capacitors are preferred as output capacitors due to their stability over temperature in industrial applications. The device's internal loop-compensation parameters are optimized for 10µF output capacitors. The device requires a minimum of 10µF (typ) capacitance for stability. Table 2 lists the recommended output capacitors. Capacitors rated less than 4V can be selected for output voltages less than 3V.

Table 1. List of Recommended Inductors

INDUCTANCE (µH)	CURRENT RATING (A)	DC RESISTANCE (TYP) (mΩ)	DIMENSIONS L x W x H (mm^3)	PART NUMBER	MANUFACTURER
1	2.6	37	2.5 x 2 x 1.2	IFSC1008ABER1R0M01	Vishay Dale
1	3.2	50	2.5 x 2 x 1	252010CDMCDS-1R0MC	Sumida
1	2.3	48	2.5 x 2 x 0.9	CIG22E1R0MNE	Samsung Electro-Mechanics America
1	2.3	48	2.5 x 2 x 1.2	MLP2520K1R0MT0S1	TDK Corporation
1	2.7	60	2 x 1.6 x 1	MAKK2016H1ROM	Taiyo Yuden

Table 2. List of Recommended Output Capacitors

CAPACITANCE (µF)	DIELECTRIC TYPE	VOLTAGE RATING (V)	PACKAGE	PART NUMBER	MANUFACTURER
10	X7R	6.3	0805	C2012X7R0J106K125AB	TDK Corporation
10	X7R	6.3	0805	GRM21BR70J106KE76K	Murata Americas
10	X7R	6.3	0805	JMK212B7106KG-T	Taiyo Yuden

Input Capacitor Selection

The input filter capacitor reduces peak current drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current (I_{RMS}) is defined by the following equation:

$$I_{RMS_CIN} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where:

$I_{OUT(MAX)}$ is the maximum load current

V_{IN} is the input voltage

V_{OUT} is the output voltage

Use low-ESR ceramic capacitors as the input capacitor. X7R temperature coefficient capacitors are recommended in industrial applications for their stability over temperature. Calculate the input capacitor value using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times V_{OUT} \times (V_{IN} - V_{OUT})}{\eta \times f_{SW} \times \Delta V_{IN} \times V_{IN}^2}$$

where:

f_{SW} is the switching frequency (= 4MHz)

η is the efficiency

In applications where the input source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input cable and the ceramic capacitor.

Adjusting the Output voltage

The MAX17620 supports output voltages from 1.5V to 100% V_{IN}. Set the output voltage with a resistor-divider connected from the positive terminal of the output voltage to the ground (see Figure 1). Choose R2 in the range of 10kΩ to 100kΩ and calculate the R1 using the following equation:

$$R1 = R2 \times \left[\frac{OUT}{.8} - 1\right]$$

Power Dissipation

Ensure that the junction temperature of the device does not exceed +125°C under the operating conditions. At a particular operating condition, the power losses that lead to the temperature rise of the device are estimated as follows:

$$P_{LOSS} = \left[P_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right] - \left(I_{OUT}^2 \times R_{DCR}\right)$$

where,

P_{OUT} is the output power given by the following equation:

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

See the Typical Operating Characteristics for the power-conversion efficiency or measure the efficiency to determine the total power losses.

The junction temperature (T_J) of the device can be estimated at any ambient temperature (T_A) from the following equation:

$$T_J = T_A + (\theta_{JA} \times P_{LOSS})$$

where θ_{JA} is the junction-to-ambient thermal resistance of the package (102°C/W for a four-layer board measured using JEDEC specification JESD51-7).

If the application has a thermal-management system that ensures the exposed pad of the device is maintained at a given temperature (T_{EP}), the junction temperature can be estimated using the following formula:

$$T_J = T_{EP} + (\theta_{JC} \times P_{LOSS})$$

where θ_{JC} is the junction-to-case thermal resistance of the device (8°C/W)

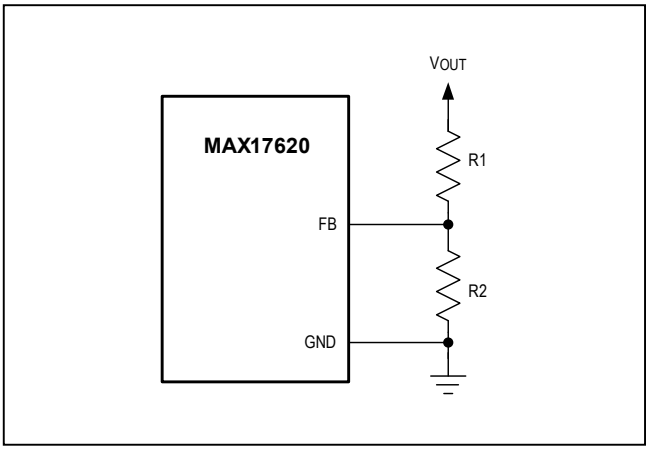


Figure 1. Adjusting the Output Voltage

PCB Layout Guidelines

Careful PCB layout is critical to achieve clean and stable operation. In particular, the traces that carry pulsating current should be short and wide so that the parasitic inductance formed by these traces can be minimized. Follow the following guidelines for good PCB layout.

- Place the input capacitor as close as possible to the IN and GND pins. Use a wide trace to connect the input capacitor to the IN and GND pins to reduce the trace inductance.
- Minimize the area formed by the LX pin and the inductor connection to reduce the radiated EMI.
- Ensure that all the feedback connections are short.
- Route the LX node away from the FB, VOUT and MODE pins.

For a sample PCB layout that ensures first-pass success, refer to the MAX17620 evaluation kit layout available at http://www.maximintegrated.com

Typical Application Circuit

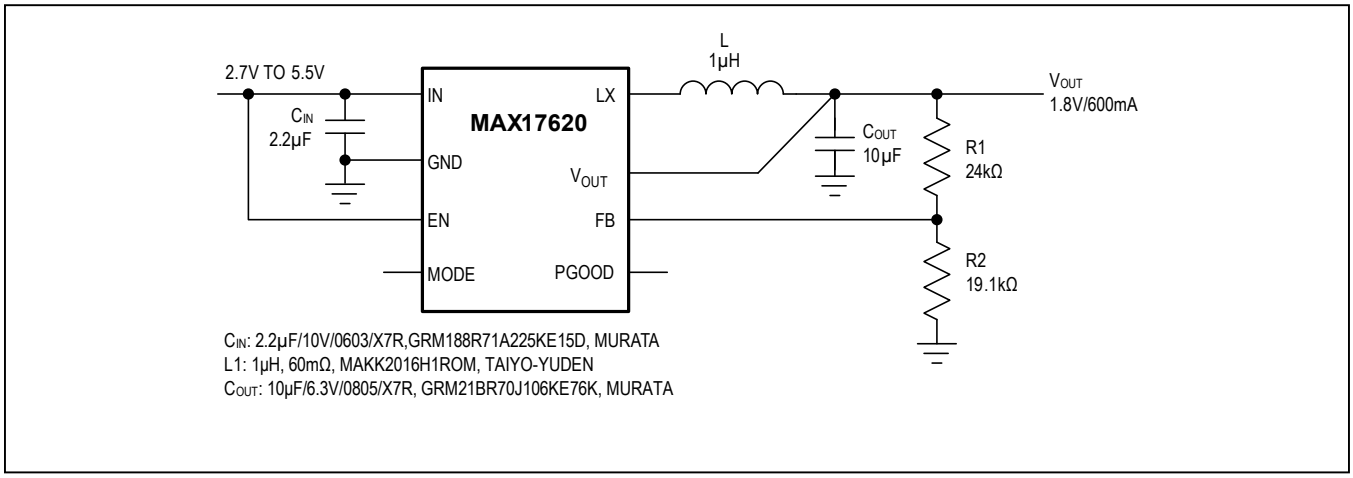


Figure 2. 1.8V, 600mA Step-Down Regulator

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17620ATA+T	-40°C to +125°C	8 TDFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN	T822+3C	**21-0168**	**90-0065**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/15	Initial release	—
1	6/15	Updated MODE pin description, updated global specifications for the *Typical Operating Characteristics* section, and updated table 1 and table 2	4–6, 7, 9, 11
2	10/15	Updated Typical Applications Circuit, replaced/added plots in *Typical Operating Characteristics* section, and updated *Block Diagram*	1-6, 8, 10–11, 13
3	7/16	Fixed minor text errors	9, 11

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