GENERAL DESCRIPTION

The XR18W753 is a low-power, single-chip RF transceiver designed to operate in license-free European 868 MHz SRD, North American / Australian 915 MHz ISM bands. Digital I/Q modulation, demodulation and direct sequence spread spectrum techniques were employed to provide robust data transmission in signal congested RF environments.

The device provides extensive hardware support for packet handling such as frame timing, data buffering, RSSI/ED/LQI for clear channel assessment, and FCS and CRC hardware for error detection. TX output power is programmable from -24 dBm to 0 dBm with 100 Kbps and 250 Kbps O-QPSK data supported.

APPLICATIONS

- Industrial/Home automation, monitoring and control
- Point of sales and data collection terminals
- Entertainment, game, toy, robot, and remote control
- Active RFID, asset tracking and keyless entry
- Lighting, HVAC energy management
- Automatic meter reading
- Wireless sensor and telemetry networks

FEATURES

- 2.2 to 3.6 Volt Operation
- 868 MHz to 956 MHz
- Direct-Sequence-Spread-Spectrum Transceiver
- Direct-up-conversion I/Q modulator
- Low-IF I/Q digital receiver
- Superior blocking/desensitization performance
- RSSI / ED / LQI for clear channel assessment
- FCS computation and CRC for error detection
- Low BOM cost and ease of production
- I^2C Interface to data buffer and internal registers
- Fully integrated loop filter with few external components needed (crystal, capacitors, antenna and matching networks)
- Programmable TX output power in 3 dB steps
- Receiver sensitivity of -94 dBm at 100 Kbps
- Supports O-QPSK 100 Kbps and 250 Kbps data
- Industrial temperature (-40 to +85 ^oC)
- 48-pin QFN package

FIGURE 1. RF TRANSCEIVER BLOCK DIAGRAM

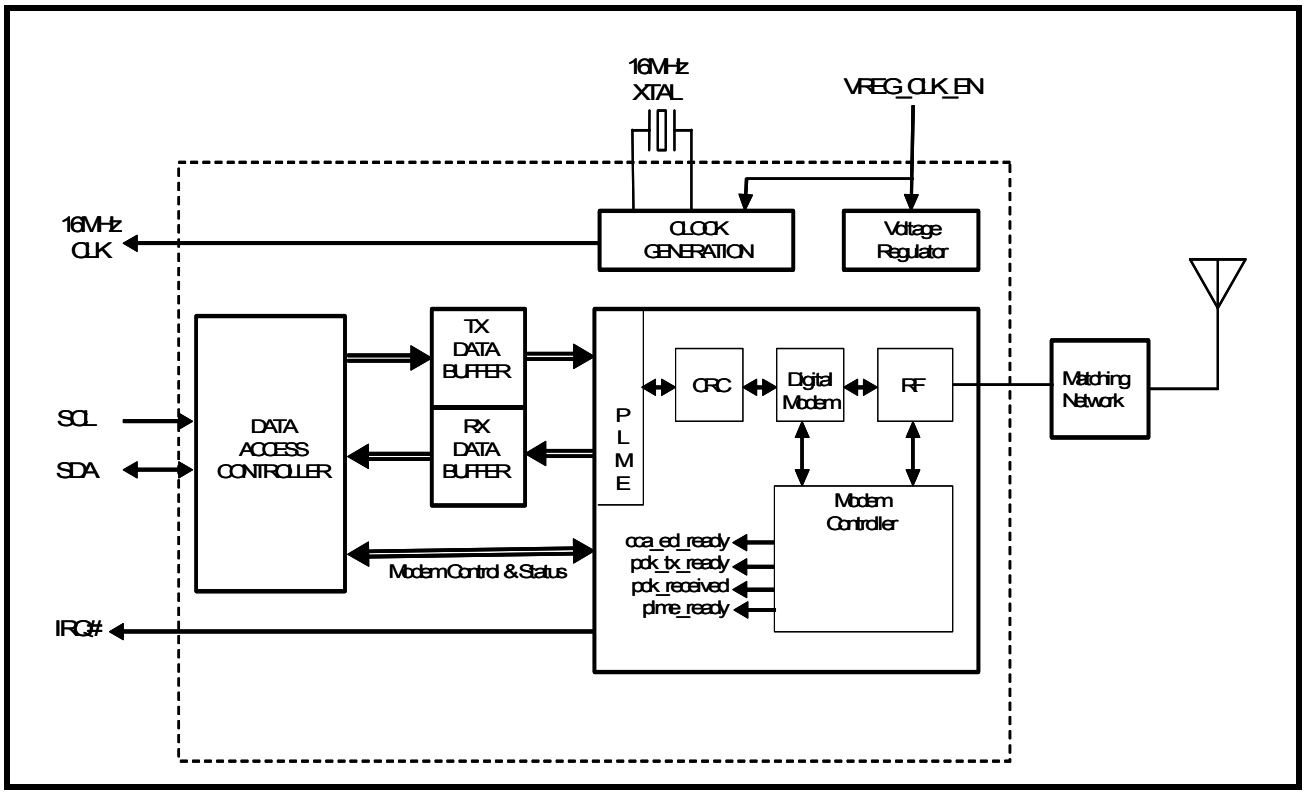


FIGURE 2. RF SYSTEM ARCHITECTURE

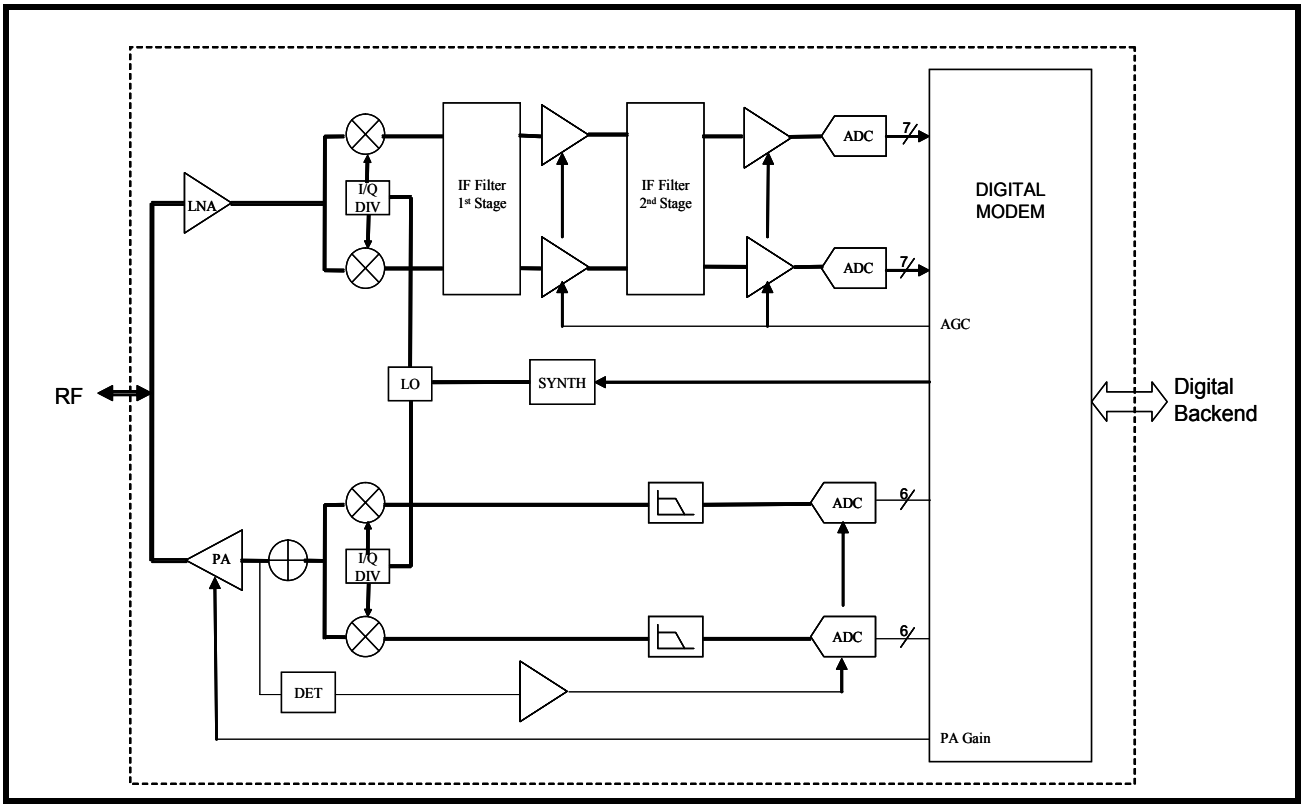
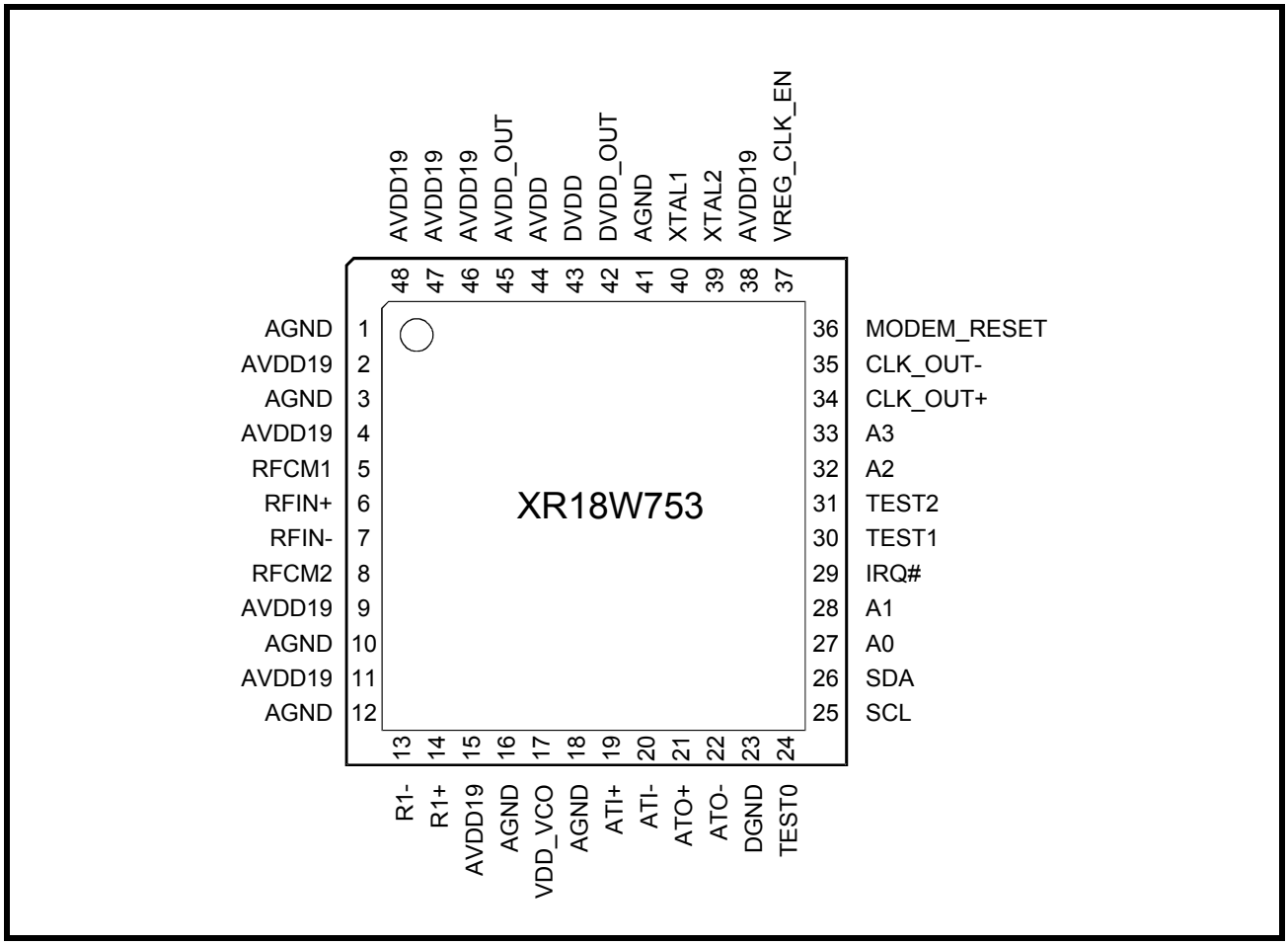


FIGURE 3. PIN DIAGRAM



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR18W753IL48	48-Lead QFN	-40°C to +85°C	Active

PIN DESCRIPTIONS

NAME	PIN	TYPE	DESCRIPTION
AGND	1	Ground	Analog ground for IF part of RX and BB part of TX
AVDD19	2	Power I	Analog VDD (1.9V ± 0.1V) for IF part of RX and BB part of TX.
AGND	3	Ground	Analog ground for RX frontend and PA
AVDD19	4	Power I	Analog VDD (1.9V ± 0.1V) for LNA and PA.
RFCM1	5	Analog O	Common Mode voltage output for matching network. Voltage output TX: 1.9V RX: ≈ 170mV
RFIN+ RFIN-	6 7	Analog I/O Analog I/O	Differential RF signals
RFCM2	8	Analog O	Common Mode voltage output for matching network. Voltage output TX: 1.9V RX: ≈ 170mV
AVDD19	9	Power I	Analog VDD (1.9V ± 0.1V) for LNA and PA.
AGND	10	Ground	Analog ground for RX frontend and PA
AVDD	11	Power I	Analog VDD (1.9V ± 0.1V) for LNA and PA.
AGND	12	Ground	Analog ground for IF part of RX and BB part of TX.
R1- R1+	13 14	Analog I/O	External resistor to fix PA power. 470 ohm resistor connected between R1- and R1+ is recommended.
AVDD19	15	Power I	Analog VDD (1.9V ± 0.1V) for synthesizer.
AGND	16	Ground	Analog ground for synthesizer.
VDD_VCO	17	Analog O	VDD of VCO. VDD = 1.9V ± 0.1V (for decoupling).
AGND	18	Ground	Analog ground for VCO.
ATI+	19	Analog I	Analog Test Input
ATI-	20	Analog I	Analog Test Input
ATO+	21	Analog O	Analog Test Output
ATO-	22	Analog O	Analog Test Output
DGND	23	Ground	Digital ground
TEST0	24	Digital I	Factory Test Mode. For normal operation, this pin should be connected to GND.
SCL	25	Digital OD	Open-drain I2C serial clock
SDA	26	Digital OD	Open-drain I2C serial data
A0	27	Digital I	I2C Address bit-0
A1	28	Digital I	I2C Address bit-1
IRQ#	29	Digital O	Interrupt output (active low, open-drain).
TEST1	30	Digital I	Factory Test Mode. For normal operation, this pin should be connected to GND.

NAME	PIN	TYPE	DESCRIPTION
TEST2	31	Digital I	Factory Test Mode. For normal operation, this pin should be connected to GND.
A2	32	Digital I	I2C Address bit-2
A3	33	Digital I	I2C Address bit-3. This address line should be connected to GND.
CLK_OUT+ CLK_OUT-	34 35	Digital O Digital O	16 MHz LVDS digital clock outputs. Connect pin 35 to ground for CMOS clock output.
MODEM_RESET	36	Digital I	Digital modem reset (active high, level sensitive).
VREG_CLK_EN	37	Digital I	Voltage Regulator and crystal oscillator enable (active high, level sensitive)
AVDD19	38	Power I	VDD (1.9V ± 0.1V) for crystal oscillator and clock divider.
XTAL1	39	Analog I	16MHz crystal input or external clock input. Based on typical PCB stray capacitance, a 27 pF capacitor to GND is recommended.
XTAL2	40	Analog I	Crystal output, 27 pF capacitor to GND is recommended. If an external clock is used at XTAL1, this input should be left unconnected.
AGND	41	Ground	Ground for crystal oscillator and buffers.
DVDD_OUT	42	Power O	Decoupling pin for digital VDD, 10 nF capacitor to GND recommended.
DVDD	43	Power I	Digital Power Supply, DVDD = 2.2 - 3.6V. DVDD and AVDD should use the same power supply. 100nF capacitor to GND recommended.
AVDD	44	Power I	Analog Power Supply, AVDD = 2.2 - 3.6V. DVDD and AVDD should use the same power supply. 100nF capacitor to GND recommended.
AVDD_OUT	45	Power O	1.9V stabilized analog VDD output. This output should be connected to all AVDD19 pins. 1uF ceramic capacitor to GND recommended.
AVDD19	46	Power I	Analog VDD (1.9V ± 0.1V) for ADC and DAC.
AVDD19	47	Power I	Analog VDD (1.9V ± 0.1V) for ADC.
AVDD19	48	Power I	Analog VDD (1.9V ± 0.1V) for IF strip, TX mixers and both I/Q dividers.
PADDLE	49	Ground	The center pad on the backside of the 48-QFN package is metallic and is not electrically connected to anything inside the device. It must be soldered on to the PCB and may be optionally connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

1.0 APPLICATION EXAMPLE

An example of how the XR18W753 can be used is shown in the figure below. In this example, the I^2C slave address of the XR18W753 is 0x60 (since all address lines are connected to GND).

FIGURE 4. APPLICATION DIAGRAM

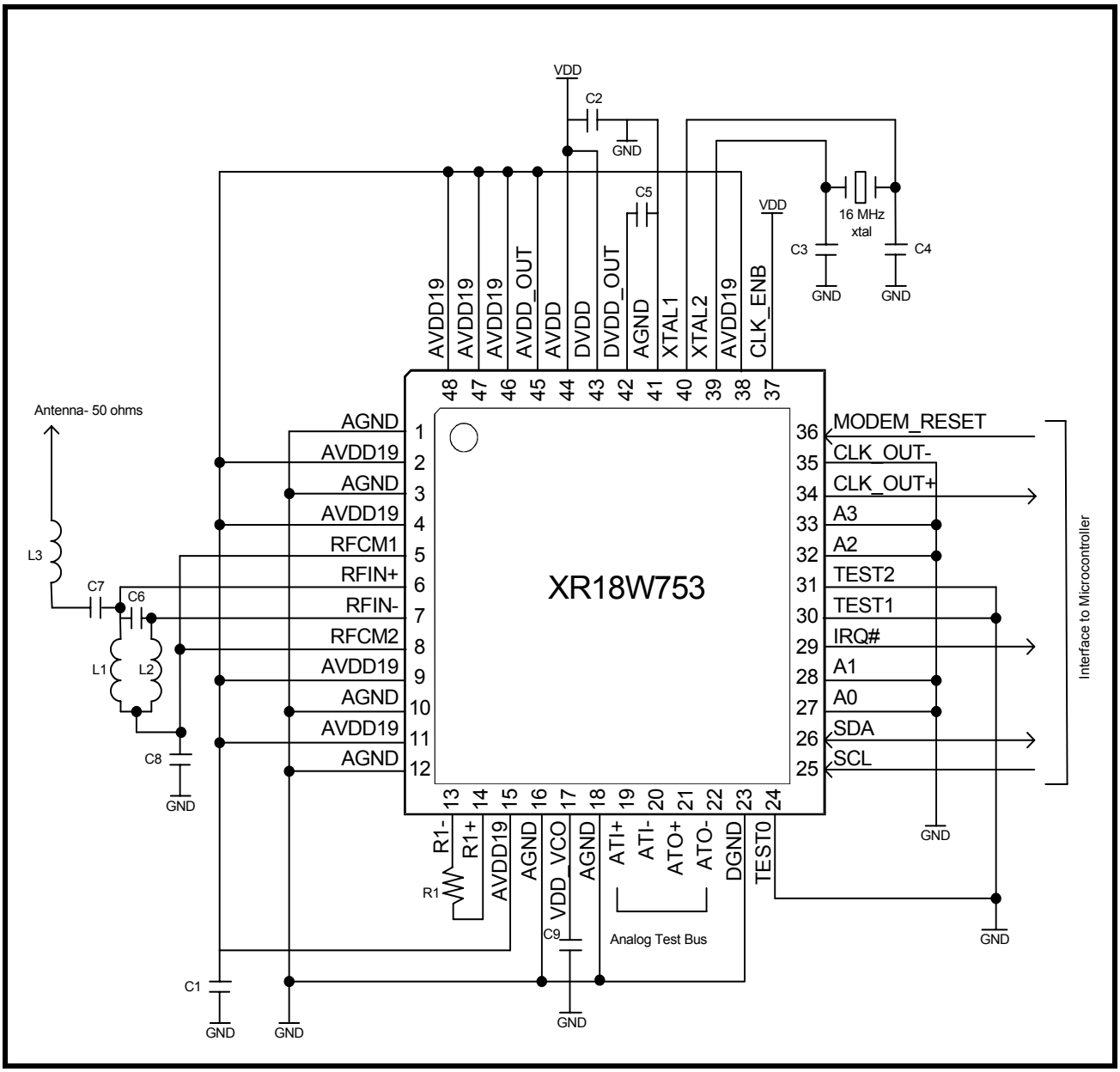


TABLE 1: VALUE OF EXTERNAL COMPONENTS

COMPONENT	VALUE[1]	NOTES
C1	1 uF	Ceramic capacitor
C2	100 nF	Ceramic capacitor
C3	27 pF	+/- 5%
C4	27 pF	+/- 5%
XTAL	16 MHz	16 MHz fundamental mode crystal 18 pF load capacitance +/-20ppm initial tolerance +/-20ppm variation over the temperature range
C5	10 nF	Ceramic capacitor
C6	2.2 pF	RF matching network capacitor
C7	8.2 pF	RF matching network capacitor
C8	100 pF	RF matching network capacitor
C9	100 pF	Ceramic capacitor
L1	4.3 nH	RF matching network inductor
L2	4.3 nH	RF matching network inductor
R1	470 ohms	External resistor to define the PA gain
L3	15 nH	RF matching network inductor

NOTE: *1. Values subject to change.*

2.0 PRODUCT DESCRIPTION

2.1 Radio Frequency Standards

The XR18W753 is designed to operate in licensed-free European 868 MHz SRD, North American / Australian 915 MHz ISM, and 950 - 956 MHz bands.

2.2 Transmitter Block

The transmitter block is a direct-up-conversion I/Q modulator consisting of D/A converters, interpolation filters, balanced I/Q mixers and a power amplifier.

2.3 Receiver Block

The receiver is a Low-IF digital receiver consisting of a low-noise amplifier (LNA), I/Q mixers, IF filters, variable gain amplifiers, and A/D converters.

2.4 Modem Block

The modem block is a Direct-Sequence-Spread-Spectrum (DSSS) O-QPSK digital modem with built-in automatic gain control (AGC), Physical Layer Management Entity (PLME), Frame Check Sum (FCS) computation, and Cyclical Redundancy Check (CRC) hardware.

2.5 Supporting Block

The supporting block in the XR18W753 includes voltage/current reference, supply voltage stabilizer, and crystal oscillator.

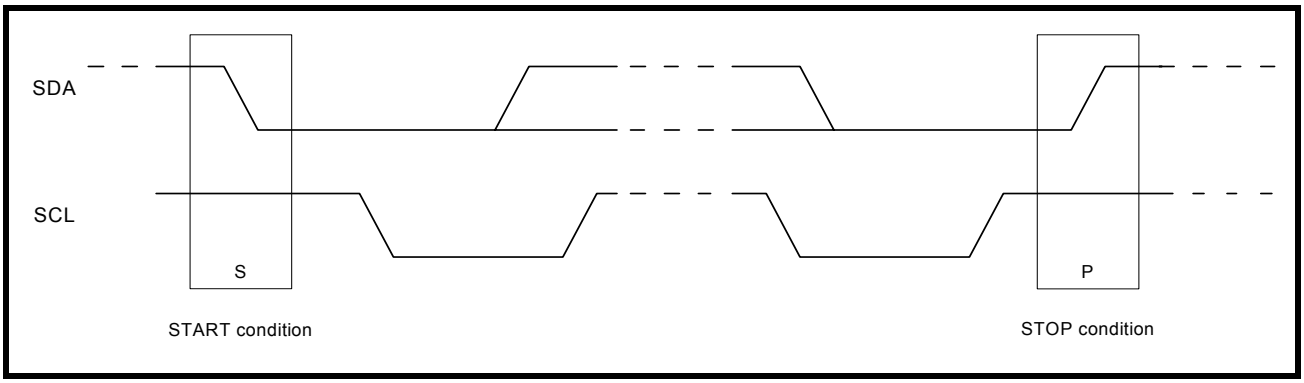
2.6 Baseband Microcontroller Interface

Interface to the XR18W753 can easily be made via the I^2C bus as in the XR18W750 baseband microcontroller. All internal registers and data buffers are accessible via this bus. A 16MHz CMOS clock is provided to the microcontroller, eliminating the cost of an extra clock or crystal.

2.6.1 I^2C-bus Interface

The I^2C-bus interface is compliant with the Standard-mode and Fast-mode I^2C-bus specifications. The I^2C-bus interface consists of two lines: serial data (SDA) and serial clock (SCL). In the Standard-mode, the serial clock and serial data can go up to 100 kbps and in the Fast-mode, the serial clock and serial data can go up to 400 kbps. The first byte sent by an I^2C-bus master contains a start bit (SDA transition from HIGH to LOW when SCL is HIGH), 7-bit slave address and whether it is a read or write transaction. The next byte is the sub-address that contains the address of the register to access. The XR18W751 responds to each write with an acknowledge (SDA driven LOW by XR18W751 for one clock cycle when SCL is HIGH). If the TX FIFO is full, the XR18W751 will respond with a negative acknowledge (SDA driven HIGH by XR18W751 for one clock cycle when SCL is HIGH) when the CPU tries to write to the TX FIFO. The last byte sent by an I^2C-bus master is a stop bit (SDA transition from LOW to HIGH when SCL is HIGH). For complete details, see the I^2C-bus specifications.

FIGURE 5. I^2C START AND STOP CONDITIONS



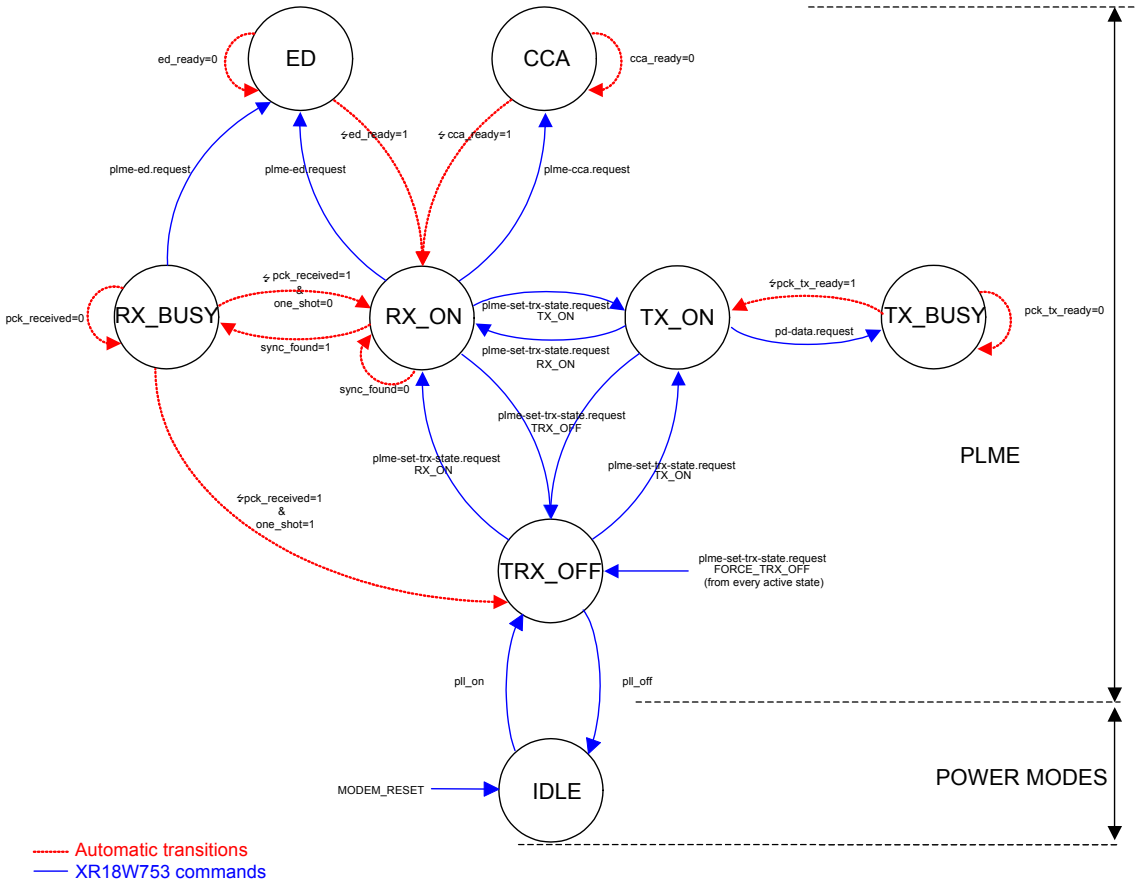
2.6.1.1 I²C-bus Addressing

The RF transceiver acts as an I²C slave. Four LSBs of I2C are mapped to external pins to support multiple chips in one application. There are eight possible slave addresses that can be selected for the XR18W753 using the A3, A2, A1 and A0 address lines. The table below shows the different addresses that can be selected. Note that A3 is always connected to GND.

A3	A2	A1	A0	I²C ADDRESS
0	0	0	0	0x60 (0110 000X)
0	0	0	1	0x62 (0110 001X)
0	0	1	0	0x64 (0110 010X)
0	0	1	1	0x66 (0110 011X)
0	1	0	0	0x68 (0110 100X)
0	1	0	1	0x6A (0110 101X)
0	1	1	0	0x6C (0110 110X)
0	1	1	1	0x6E (0110 111X)

The Physical Layer Management Entity (PLME) provides layer management service interfaces through which layer management functions may be invoked. The figure below shows the different modes of operation that can be invoked by the PLME.

FIGURE 6. MODES OF OPERATION



NOTE: Every XR18W753 command is acknowledged by the 'plme_ready' interrupt

The modes of operation can be invoked via the MODEM_REQUEST register and the status can be read from the MODEM_CONF0 and MODEM_CONF1 registers.

3.0 I2C MEMORY MAP

3.1 REGISTERS OVERVIEW

ADDRESS	REGISTER NAME	RESET VALUE	TYPE	COMMENTS
0x00	READ_SUBADDDRESS	0x00	R/W	
0x01	RX_FIFO	-	R	
0x02	TX_FIFO	0x00	W	
0x03	FIFO_CONTROL	0x00	R/W	
0x04	INT_MASKING	0x08	R/W	Interrupt masking
0x05	INT_STATUS	-	R	Interrupt status
0x06-0xF	Reserved	-	-	
0x10	MODEM_REQUEST	0x00	R/W	
0x11	MODEM_CONF_0	-	R	
0x12	MODEM_CONF_1	-	R	
0x13	ED_AV_TIME	0x00	R/W	
0x14	MODEM_ED	-	R	
0x15	MODEM_LQI	-	R	
0x16-0x1F	Reserved	-	-	
0x20	CHANNEL	0x01	R/W	Frequency channel selection
0x21	TX_POWER	0x00	R/W	Transmit output power
0x22 - 0x26	Reserved	-	-	
0x27	AGC_ACT_VALUE	-	R	
0x28	Reserved	-	-	
0x29	SLICER_LEVEL	-	R	Frequency Offset (2’s complement)
0x2A-0x2D	Reserved	-	-	
0x2E	ED_THRES	0x00	R/W	
0x2F - 0x30	RSSI_ACT_VALUE_0, 1	-	R	Two’s complement number
0x31-0x4F	Reserved	-	-	
0x50	TEST_0	-	R/W	For normal operation, initialize to 0xD1
0x51	TEST_1	-	R/W	For normal operation, initialize to 0x19
0x52	TEST_2	-	R/W	For normal operation, initialize to 0x82
0x53	TEST_3	-	R/W	For normal operation, initialize to 0x00
0x54 - 0x7D	Reserved	-	-	
0x7E	CHIP_ID	0xB1	R	
0x7F	REV_ID	0x03	R	

Reserved registers are for internal use only.

3.2 DETAILED REGISTERS DESCRIPTIONS

ADDRESS	REGISTER NAME	DESCRIPTION	TYPE
0x00	READ_SUBADDRESS	b[7:0] To ease reading via I2C, the data of READ_SUBADDRESS is a pointer to the first address in the I2C memory map. If the master wants to read the content of register e.g. 0x2E, the master first need to write 0x2E to READ_SUBADDRESS.	R/W
0x01	RX_FIFO	b[7:0] To retrieve data from the RX Data Buffer, the master must read from this register. All entries of the RX Data Buffer are mapped to this register, offering a FIFO mechanism.	R
0x02	TX_FIFO	b[7:0] To put data into the TX Data Buffer, the master must write to this register. All entries of the TX Data Buffer are mapped to this register, offering a FIFO mechanism.	W
0x03	FIFO_CONTROL	b[2:0] = 001 --> reset RX_FIFO read address b[2:0] = 010 --> reset RX_FIFO write address b[2:0] = 011 --> reset TX_FIFO read address b[2:0] = 100 --> reset TX_FIFO write address b[2:0] = 101 --> reset RX_FIFO read address b[2:0] = 110 --> reset RX_FIFO write address b[2:0] = 001 --> reset RX_FIFO read address b[2:0] = 111 --> reset all RX and TX FIFO addresses b[7:3] not used Via this register, the internal FIFO read and write pointers of the TX Data Buffer and the RX Data Buffer can be set to 0X00. The content of the Data Buffers is unaffected by resetting the pointers.	R/W
0x04	INT_MASKING	b[0] = 0 --> pck_tx_ready interrupt disabled b[0] = 1 --> pck_tx_ready interrupt enabled b[1] = 0 --> pck_received interrupt disabled b[1] = 1 --> pck_received interrupt enabled b[2] = 0 --> cca_ed_ready interrupt disabled b[2] = 1 --> cca_ed_ready interrupt enabled b[3] = 0 --> plme_ready interrupt disabled b[3] = 1 --> plme_ready interrupt enabled b[7:4] not used Via this register, the internal modem interrupts can be enabled or disabled. PLME_ready is enabled at start-up; after reset, a PLME_ready is generated.	R/W

3.2 DETAILED REGISTERS DESCRIPTIONS

ADDRESS	REGISTER NAME	DESCRIPTION	TYPE
0x05	INT_STATUS	b[0] = 0 --> indicates the pck_tx_ready interrupt occurred b[1] = 0 --> indicates the pck_received interrupt occurred b[2] = 0 --> indicates the cca_ed_ready interrupt occurred b[3] = 0 --> indicates the plme_ready interrupt occurred b[7:4] not used Via this register, the modem interrupt status can be read. Once read, the content of the register will automatically set to 0x00.	R
0x10	MODEM_REQUEST	b[4:0] = 00xxx --> no request (x indicates “don’t care”) b[4:0] = 01000 --> plme-set-trx-state = FORCE_TRX_OFF b[4:0] = 01010 --> plme-set-trx-state = RX_ON b[4:0] = 01011 --> plme-set-trx-state = TX_ON b[4:0] = 01100 --> pd-data.request (TX-data) b[4:0] = 01101 --> plme-ED.request b[4:0] = 01110 --> plme-CCA.request b[4:0] = 01111 --> not used b[4:0] = 10000 --> PLL off b[4:0] = 10001 --> PLL on b[6:5] = 00 --> not used b[6:5] = 01 --> CCA mode1 b[6:5] = 10 --> CCA mode2 b[6:5] = 11 --> CCA mode3 b[7] = 0 --> after full reception of a packet, the modem is accepting new incoming data (continuous packet reception) b[7] = 0 --> after full reception of a packet, the PLME goes to TRX_OFF state (one shot packet reception) This register is used for: 1. Sending PLME related requests to the modem. 2. Defining CCA mode for clear channel assessment . 3. Defining whether the modem should be sensitive for data after a full reception of a data packet.	R/W

3.2 DETAILED REGISTERS DESCRIPTIONS

ADDRESS	REGISTER NAME	DESCRIPTION	TYPE
0x11	MODEM_CONF_0	b[2:0] = 000 --> plme-set-trx-state = TRX_OFF b[2:0] = 001 --> plme-set-trx-state = SUCCESS b[2:0] = 010 --> plme-set-trx-state = RX_ON b[2:0] = 011 --> plme-set-trx-state = TX_ON b[2:0] = 100 --> plme-set-trx-state = BUSY_RX b[2:0] = 101 --> plme-set-trx-state = BUSY_TX b[2:0] = 110 --> not used b[2:0] = 111 --> not used b[4:3] = 00 --> plme-CCA = TRX_OFF b[4:3] = 01 --> plme-CCA = TX_ON b[4:3] = 10 --> plme-CCA = BUSY b[4:3] = 11 --> plme-CCA = IDLE b[6:5] = 00 --> plme-ED = TRX_OFF b[6:5] = 01 --> plme-ED = TX_ON b[6:5] = 10 --> plme-ED = SUCCESS b[6:5] = 11 --> not used b[7] not used This register is used for reading the confirmation of the PLME of the modem.	R
0x12	MODEM_CONF_1	[1:0] = 00 --> pd-data = TRX_OFF b[1:0] = 01 --> pd-data = RX_ON b[1:0] = 10 --> pd-data = SUCCESS b[1:0] = 11 --> not used b[2] = 0 --> no CRC error in received frame b[2] = 1 --> CRC error in received frame b[7:4] not used This register is used for reading the confirmation of the PLME of the modem and the result of the CRC computation of the received data packet.	R

3.2 DETAILED REGISTERS DESCRIPTIONS

ADDRESS	REGISTER NAME	DESCRIPTION	TYPE
0x13	ED_AV_TIME	Measurement time for ED Measurement b[3:0] = 0000 --> 8 symbols b[3:0] = 0001 --> 5.0 mSec b[3:0] = 0010 --> 5.5 mSec b[3:0] = 0011 --> 6.0 mSec b[3:0] = 0100 --> 6.5 mSec b[3:0] = 0101 --> 7.0 mSec b[3:0] = 0110 --> 7.5 mSec b[3:0] = 0111 --> 8.0 mSec b[3:0] = 1000 --> 8.5 mSec b[3:0] = 1001 --> 9.0 mSec b[3:0] = 1010 --> 9.5 mSec b[3:0] = 1011 --> 10.0 mSec b[3:0] = 11xx --> 10.0 mSec b[7:4] not used Via this register, the ED measurement time can be defined. In case value 0 is chosen, the measurement time is compliant to the definition of the IEEE802.15.4b standard. In the 902-928 MHz band, the measurement time equals 128us. For the 868 MHz band, this symbol time equals 320us.	R/W
0x14	MODEM_ED	LQI Value, updated as a result of successful ED measurement. The result of the ED measurement is available in this register. The value is normalized and on average will be independent from the ED measurement time (ED_AV_TIME). Note that the value of MODEM_ED also depends on the content of ED_THRESH (0x2E).	R
0x15	MODEM_LQI	LQI Value, updated after complete frame reception. During reception of a data packet, the correlation values of the symbol mapping is accumulated and divided by the number of symbols in the packets. The number is a normalized Link Quality Indication.	R
0x16-0x1F	Reserved	-	-

3.2 DETAILED REGISTERS DESCRIPTIONS

ADDRESS	REGISTER NAME	DESCRIPTION	TYPE
0x20	CHANNEL	b[4:0] = 00000 --> 868.3 MHz b[4:0] = 00001 --> 903 MHz b[4:0] = 00010 --> 904 MHz b[4:0] = 00011 --> 905 MHz b[4:0] = 00100 --> 906MHz b[4:0] = 00101 --> 907MHz b[4:0] = 00110 --> 908 MHz b[4:0] = 00111 --> 909 MHz b[4:0] = 01000 --> 910 MHz b[4:0] = 01001 --> 911 MHz b[4:0] = 01010 --> 912 MHz b[4:0] = 01011 --> 913 MHz b[4:0] = 01100 --> 914 MHz b[4:0] = 01101 --> 915 MHz b[4:0] = 01110 --> 916 MHz b[4:0] = 01111 --> 917 MHz b[4:0] = 10000 --> 918 MHz b[4:0] = 10001 --> 919 MHz b[4:0] = 10010 --> 920 MHz b[4:0] = 10011 --> 921 MHz b[4:0] = 10100 --> 922 MHz b[4:0] = 10101 --> 923 MHz b[4:0] = 10110 --> 924 MHz b[4:0] = 10111 --> 925 MHz b[4:0] = 11000 --> 926 MHz b[4:0] = 11001 --> 927 MHz b[4:0] = 11010 --> 951 MHz b[4:0] = 11011 --> 952 MHz b[4:0] = 11100 --> 953 MHz b[4:0] = 11101 --> 954 MHz b[4:0] = 11110 --> 955 MHz b[7:5] not used Via this register, the channel frequency can be selected.	R/W

3.2 DETAILED REGISTERS DESCRIPTIONS

ADDRESS	REGISTER NAME	DESCRIPTION	TYPE
0x21	TX_POWER	Transmit output power during normal operation. b[5:0] = 0xxxxx --> TX Power = 0 dBm b[5:0] = 111111 --> TX Power = 0 dBm b[5:0] = 111110--> TX Power = 0 dBm b[5:0] = 111101 --> TX Power = 0dBm b[5:0] = 111100 --> TX Power = -3 dBm b[5:0] = 111011--> TX Power = -3 dBm b[5:0] = 111010 --> TX Power = -3 dBm b[5:0] = 111001 --> TX Power = -6 dBm b[5:0] = 111000--> TX Power = -6 dBm b[5:0] = 110111 --> TX Power = -6 dBm b[5:0] = 110110 --> TX Power = -9 dBm b[5:0] = 110101--> TX Power = -9 dBm b[5:0] = 110110 --> TX Power = -9 dBm b[5:0] = 110011 --> TX Power = -12 dBm b[5:0] = 110010--> TX Power = -12 dBm b[5:0] = 110001 --> TX Power = -12 dBm b[5:0] = 110000 --> TX Power = -15 dBm b[5:0] = 101111--> TX Power = -15 dBm b[5:0] = 101110 --> TX Power = -15 dBm b[5:0] = 101101 --> TX Power = -18 dBm b[5:0] = 101100--> TX Power = -18 dBm b[5:0] = 101011 --> TX Power = -18 dBm b[5:0] = 101010 --> TX Power = -21 dBm b[5:0] = 101001--> TX Power = -21 dBm b[5:0] = 101000 --> TX Power = -21 dBm b[5:0] = 100xxx --> TX Power = -24 dBm b[7:6] not used Note: x indicates don’t care	R/W
0x22 - 0x26	Reserved	-	-

3.2 DETAILED REGISTERS DESCRIPTIONS

ADDRESS	REGISTER NAME	DESCRIPTION	TYPE
0x27	AGC_ACT_VALUE	AGC setting instantaneous value b[3:0] = 0000 --> IF-AGC set to 0dB b[3:0] = 0001 --> IF-AGC set to -6dB b[3:0] = 0010 --> IF-AGC set to -12dB b[3:0] = 0011 --> IF-AGC set to -18dB b[3:0] = 0100 --> IF-AGC set to -24dB b[3:0] = 0101 --> IF-AGC set to -30dB b[3:0] = 0110 --> IF-AGC set to -36dB b[3:0] = 0111 --> IF-AGC set to -42dB b[3:0] = 1000 --> IF-AGC set to -48dB b[3:0] = 1001 --> not used b[3:0] = 1010 --> not used b[3:0] = 1011 --> not used b[3:0] = 1100 --> not used b[3:0] = 1101 --> not used b[3:0] = 1110 --> not used b[3:0] = 1111 --> not used b[7:4] not used	R
0x28	Reserved	-	-
0x29	SLICER_LEVEL	Frequency offset in a link can be read out via this register. The value is interpreted as an 8-bit two's complement value (-128 to +127). The conversion from this value to frequency is given below. For 902 - 928 MHz application, the frequency offset is: f_{offset} = 1MHz x SLICER_LEVEL / 128 For 868 MHz application, the frequency offset is: f_{offset} = 400 kHz x SLICER_LEVEL / 128	R
0x2A-0x2D	Reserved	-	-
0x2E	ED_THRES	Energy detection threshold In IEE802.15.4 specification, it has been defined how the result of the ED measurement given in MODEM_ED (0x15) need to be reported. The value of ED_THRES is used to align the receiver with the IEE802.15.4 ED measurement specification.	R/W
0x2F - 0x30	RSSI_ACT_VALUE_0,1	Actual RSSI value_0, 1 The instantaneous level to the digital demodulator can be read via these two registers. The value is interpreted as a two's complement number. Together with the information of AGC_ACT_VALUE (0x27), the instantaneous RF level can be calculated.	R
0x31-0x4F	Reserved	-	-
0x50	TEST_0	This register is used for factory test modes. For normal operation, initialize this register to 0xD1.	R/W

3.2 DETAILED REGISTERS DESCRIPTIONS

ADDRESS	REGISTER NAME	DESCRIPTION	TYPE
0x51	TEST_1	This register is used for factory test modes. For normal operation, initialize this register to 0x19.	R/W
0x52	TEST_2	This register is used for factory test modes. For normal operation, initialize this register to 0x82.	R/W
0x53	TEST_3	This register is used for factory test modes. For normal operation, initialize this register to 0x00.	R/W
0x54 - 0x7D	Reserved	-	-
0x7E	CHIP_ID	Chip_ID used to categorize the XR18W753. The CHIP_ID is 0xB1.	R
0x7F	REV_ID	REV_ID is used to keep track of the hardware version of the XR18W753 chip.	R

ABSOLUTE MAXIMUM RATING

Supply Voltage, AVDD	+3.6	V
Supply Voltage, DVDD	+3.6	V
Supply Voltage, AVDD19	+2.0	V
Ambient Temperature	+85	^{o}C

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

Thermal Resistance (48-QFN)	theta-ja = 40^{o}C/W, theta-jc = 13^{o}C/W

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VDD IS 2.2V TO 3.6V

SYMBOL	PARAMETER	LIMITS 2.5V MIN	LIMITS 2.5V TYP	LIMITS 2.5V MAX	LIMITS 3.3V MIN	LIMITS 3.3V TYP	LIMITS 3.3V MAX	UNITS
V_{ILCK}	External Clock Input Low Level	-0.3		0.4	-0.3		0.6	V
V_{IHCK}	External Clock Input High Level	2.0		VDD	2.4		VDD	V
V_{IL}	Input Low Voltage	-0.3		0.5	-0.3		0.7	V
V_{IH}	Input High Voltage	1.8		5.5	2.0		5.5	V
V_{OL}	Output Low Voltage			 0.4			0.4	V V
V_{OH}	Output High Voltage	 1.8			2.0			V V
I_{IL}	Input Low Leakage Current			±10			±10	uA
I_{IH}	Input High Leakage Current			±10			±10	uA
C_{IN}	Input Pin Capacitance			5			5	pF
I_{DD}	Power Supply Current (VREG DISABLED) Power Supply Current (IDLE) Power Supply Current (RX_ON) Power Supply Current (TX_ON)		0.5 1.7 19 22			0.5 1.7 19 22		mA mA mA mA

AC ELECTRICAL CHARACTERISTICS - I2C-BUS TIMING SPECIFICATIONS

Unless otherwise noted: TA=-40^{o} to +85^{o}C, VDD=2.2 - 3.6V

SYMBOL	PARAMETER	STANDARD MODE I2C-BUS			FAST MODE I2C-BUS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{SCL}	Operating frequency			100			400	kHz
T_{BUF}	Bus free time between STOP and START	4.7			1.3			µs
$T_{HD;STA}$	START condition hold time	4.0			0.6			µs
$T_{SU;STA}$	START condition setup time	4.7			0.6			µs
$T_{HD;DAT}$	Data hold time	0			0			ns
$T_{VD;ACK}$	Data valid acknowledge			0.6			0.6	µs
$T_{VD;DAT}$	SCL LOW to data out valid			0.6			0.6	ns
$T_{SU;DAT}$	Data setup time	250			150			ns
T_{LOW}	Clock LOW period	4.7			1.3			µs
T_{HIGH}	Clock HIGH period	4.0			0.6			µs
T_F	Clock/data fall time			300			300	ns
T_R	Clock/data rise time			1000			300	ns
T_{SP}	Pulse width of spikes tolerance		0.5			0.5		µs
T_{D15}	SCL delay after reset	3			3			µs

FIGURE 7. SCL DELAY AFTER RESET

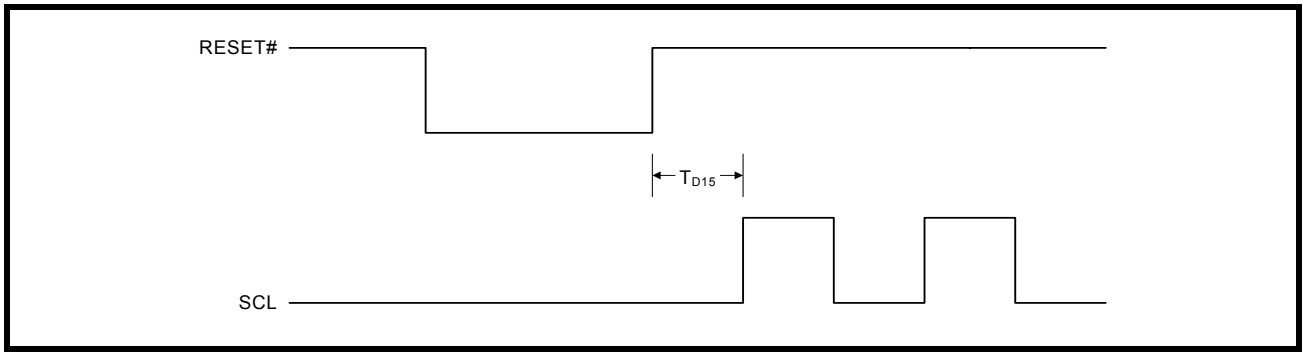
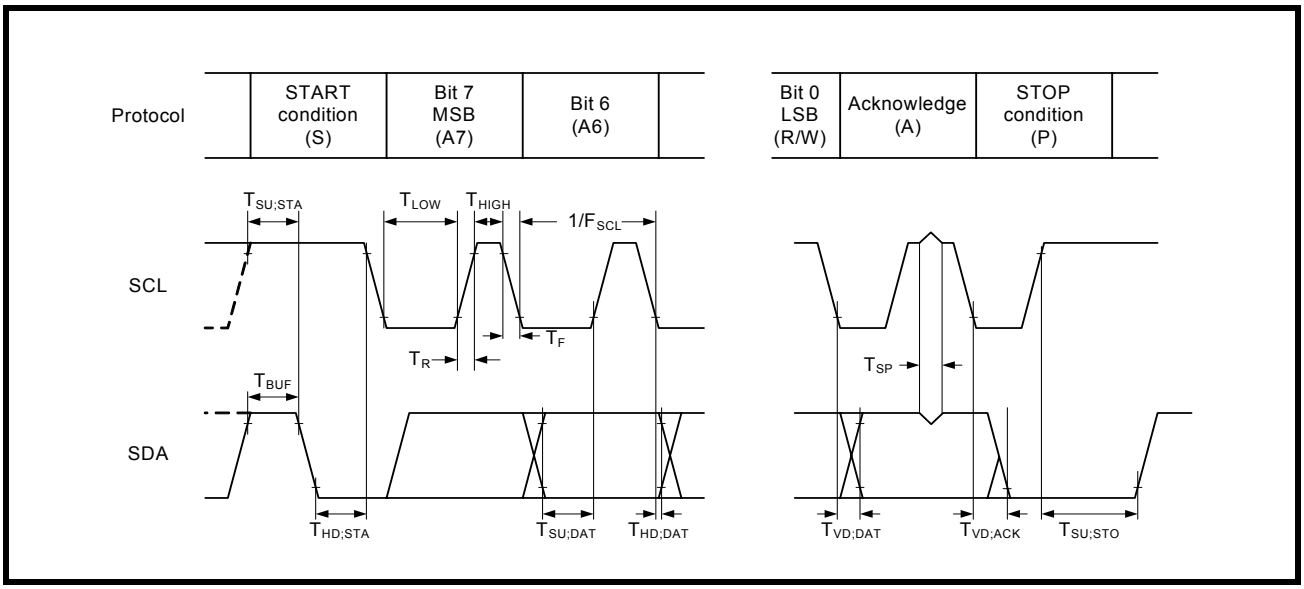


FIGURE 1. I²C-BUS TIMING DIAGRAM



REFERENCE OSCILLATOR SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Center Frequency		16		MHz
Frequency Tolerance			±40	ppm
External Crystal Load Capacitance		18		pF

OPERATING FREQUENCY

FREQUENCY BAND	FREQUENCY	UNIT
European SRD	868.3	MHz
North American / Australian ISM	903 - 927	MHz
950 MHZ	951 - 955	MHz

MODULATION

O-QPSK with half-sine wave pulse shaping	Equivalent to MSK (FM with m=0.5)

DATA RATES

FREQUENCY BAND	SYMBOL RATE	BIT RATE	CHIP RATE	-3dB BANDWIDTH	NOTE
European SRD	25 Ksps	100 Kbps	400 Kcps	200 KHz	16-ary symbols 16 chips per symbol 4 bits per symbol 2 symbols per byte
North American / Australian ISM	62.5 Ksps	250 Kbps	1 Mcps	500 KHz	
950 MHZ	62.5 Ksps	250 Kbps	1 Mcps	500 KHz	

PACKET STRUCTURE

Europe SRD Band		
Preamble (all zero-symbols)	4	Bytes
Start Frame Delimiter (SFD = 0xA7)	1	Bytes
Frame Length (PHR)	1	Bytes
Payload Data	0 - 127	Bytes
Frame Check Sum (FCS)	2	Bytes
North American / Australian ISM Band		
Preamble (all zero-symbols)	10	Bytes
Start Frame Delimiter (SFD = 0xA7)	1	Bytes
Frame Length (PHR)	1	Bytes
Payload Data	0 - 127	Bytes
Frame Check Sum (FCS)	2	Bytes
950 MHZ Band		
Preamble (all zero-symbols)	10	Bytes
Start Frame Delimiter (SFD = 0xA7)	1	Bytes
Frame Length (PHR)	1	Bytes
Payload Data	0 - 127	Bytes
Frame Check Sum (FCS)	2	Bytes

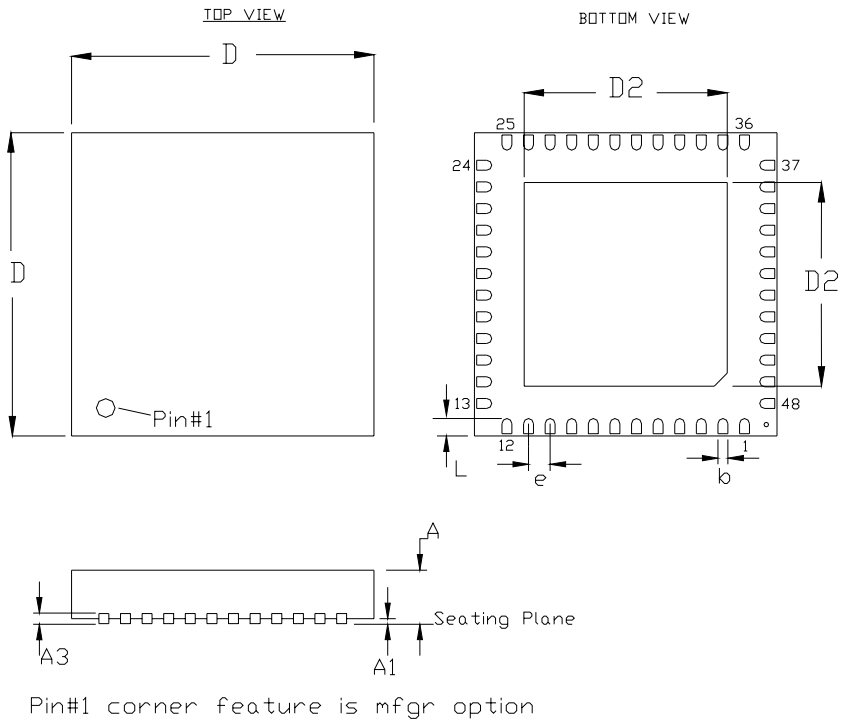
TRANSMITTER

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
TX Output Power		0 -3 -6 -9 -12 -15 -18 -21 -24		dBm	
TX Power Control		3		dB	
Antenna Impedance		50		Ω	with external matching network
Error Vector Magnitude		5		%	
Spurious Emission (wideband) 30MHz - 1GHz 1GHz - 12.75GHz 1.8GHz - 1.9GHz 5.15GHz - 5.3GHz		 -86 -80 -97 -97		dBm/Hz	EN300 328 4.3.4.2

RECEIVER

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Sensitivity @100 Kbps		-94		dBm	PER = 1%, Payload = 20 bytes
Sensitivity 250 Kbps		-91		dBm	PER = 1%, Payload = 20 bytes
Noise Figure		12		dB	
Antenna Impedance		50		Ω	with external matching network
Blocking / Desensitization 1MHz 2MHz 5MHz 10MHz		 -52 -47 -32 -22		dBm	EN 300 220 CW. at -82 dBm sensitivity level
Largest signal		10		dBm	
IP3		-20		dBm	
RSSI Accuracy		±6		dB	

PACKAGE DIMENSIONS (48 PIN QFN - 7 X 7 X 0.9 mm)



Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A3	0.006	0.010	0.15	0.25
D	0.270	0.281	6.85	7.15
D2	0.201	0.209	5.10	5.30
b	0.007	0.012	0.18	0.30
e	0.0197 BSC		0.50 BSC	
L	0.012	0.020	0.30	0.50

REVISION HISTORY

DATE	REVISION	DESCRIPTION
February 2007	P1.0.0	Preliminary Datasheet.
September 2007	P1.0.1	Updated to new datasheet template.
March 2008	1.0.0	Final Datasheet

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 2008 EXAR Corporation

Datasheet March 2008.

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.