Dual Channel High Efficiency and High Accuracy Average Current Control LED Backlight Buck Controller

General Description

The RT6010 is a dual channel high accuracy average current control LED backlight buck controller for 2 LED strings w/ o LED binning. Dual MOSFET drivers are specifically designed to drive two power N-MOSFETs in an asynchronous buck converter topology. The controller provides variable LED current control by adjusting the CS resistor value for digital and linear dimming. The controller operates with T1/T2 Average Current Control (T^2C) topology to provide high accuracy ±3%. The controller also provides high efficiency (higher than 95%) under proper setting without LED binning. The controller provides V_{IN} from 8V to 450V. It is preferred to operate the controller under a current ripple of < 30% average current and about 85% duty to optimize the performance.

The RT6010 can be easily connected in series by master/ slave synchronization for multiple channel, even for more than 6-CH. The controller provides SPD (Smart Phase Shift Dimming) that is easily implemented to synchronize master and slave ICs. The controller provides both analog and PWM dimming.

The RT6010 automatically detects LED bar open, LED bar short to V_{IN}, and LED bar short to GND to prevent VOUT from over/under voltage damages. The controller also outputs fault signal with programmable delay to previous power stage, such as ACDC controller.

Ordering Information

RT6010□□

- Package Type
  S :SOP-16
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

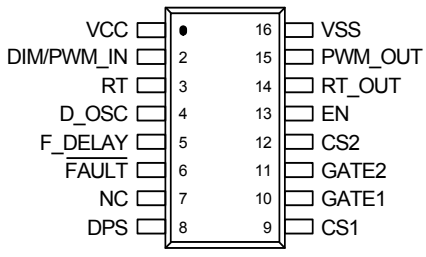
- **Fast Average Current Control T^2C (T1/T2 Average Current Control)**
- **Dual MOSFET Drives for Asynchronous Buck Topology**
- **Provide High Efficiency > 95% and High Accuracy ±3% Channel to Channel Variation**
- **Provide LED w/o Binning**
- **Programmable PWM Constant Off Time**
- **Support both PWM and Analog Dimming**
- **PWM Dimming Duty Down to 1%**
- **OVP for Bar Short with V_{IN}**
- **UVP for Bar Open/Short to GND with programmable Fault Delay**
- **Support SPD (Smart Phase Shift Dimming) for Multiple Channel Dimming Solution**
- **V_{IN} POR Detection with EN Pin to Prevent Malfunction**
- **SOP-16 Package**
- **RoHS Compliant and Halogen Free**

Applications

- LCD TV, MNT Display Backlight
- DC/DC or ACDC LED Driver Application
- General Purpose Constant Current Source
- LED Signage and Display
- Architectural and Decorative LED Lighting
- LED Street Lighting

Pin Configurations

(TOP VIEW)



SOP-16

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Marking Information

RT6010
GSYMDNN
●

RT6010GS : Product Number

YMDNN : Date Code

Typical Application Circuit

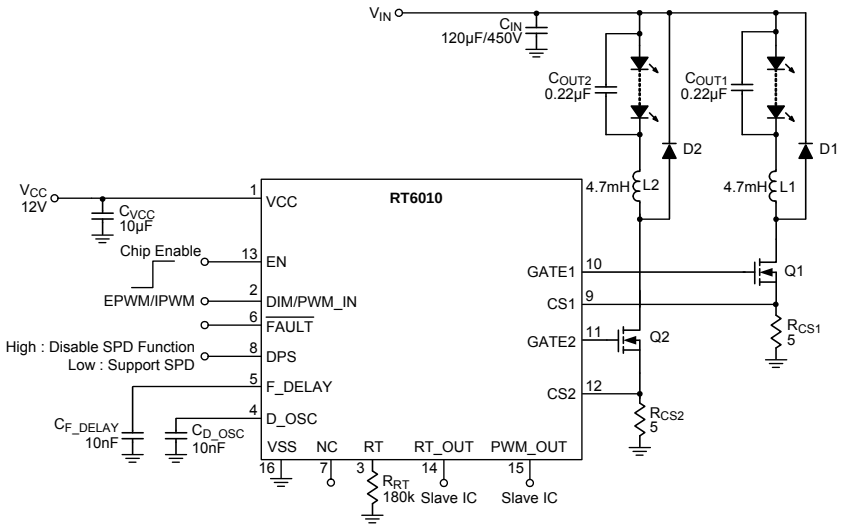


Figure 1

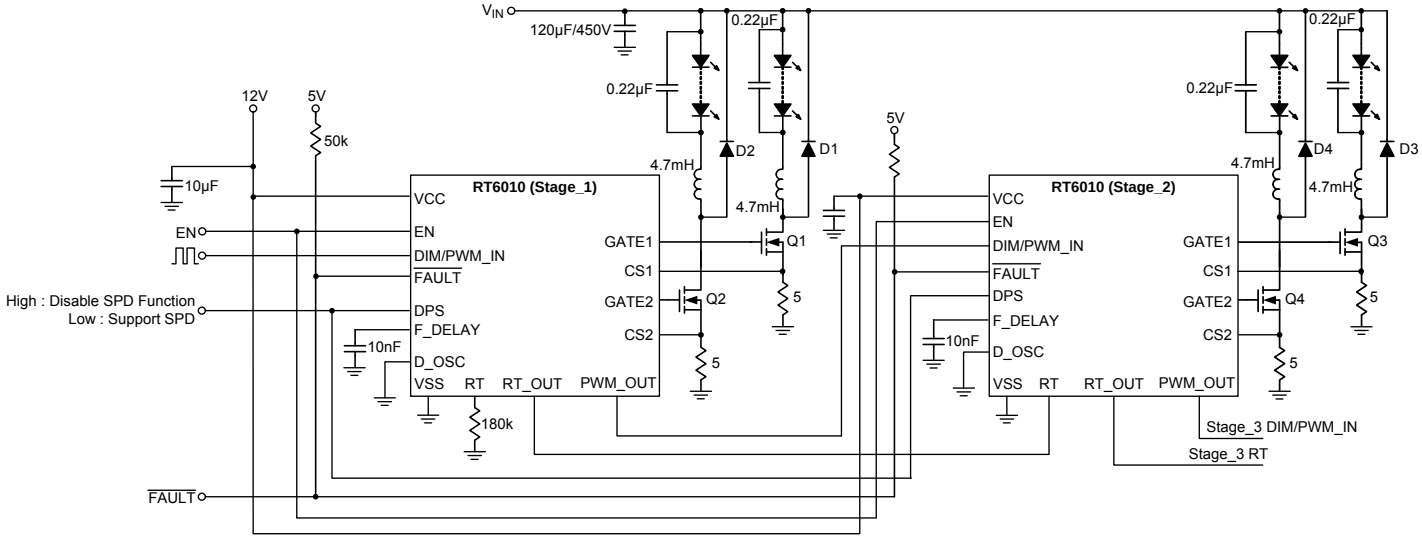


Figure 2. Synchronization for Multiple Channel_Digital

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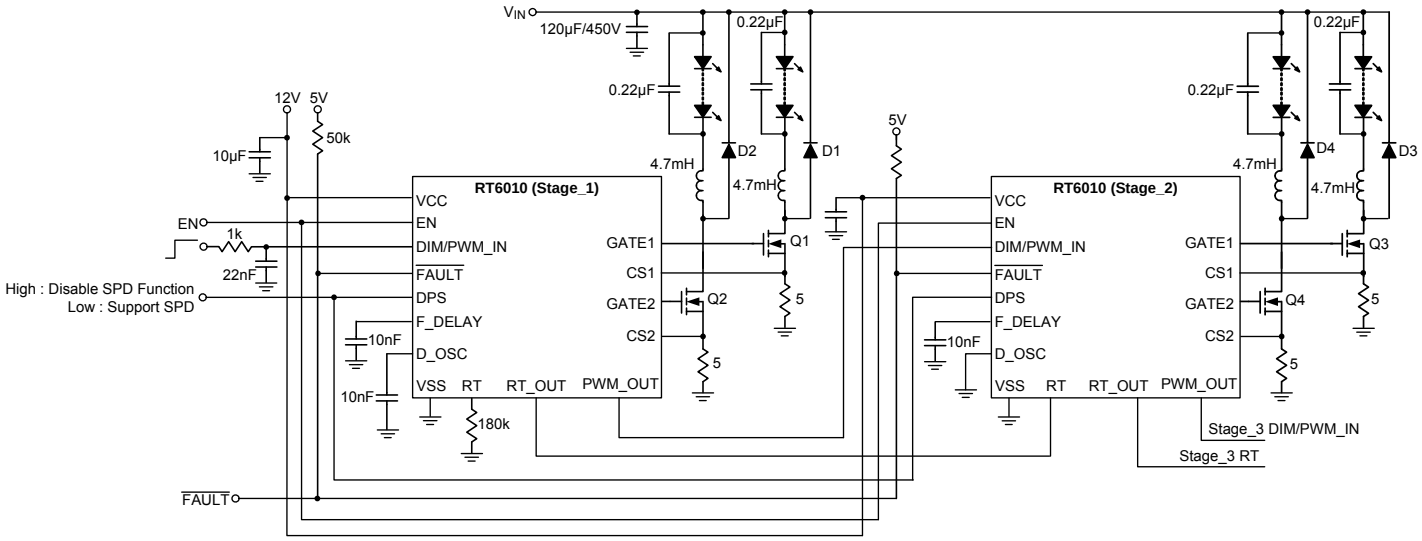


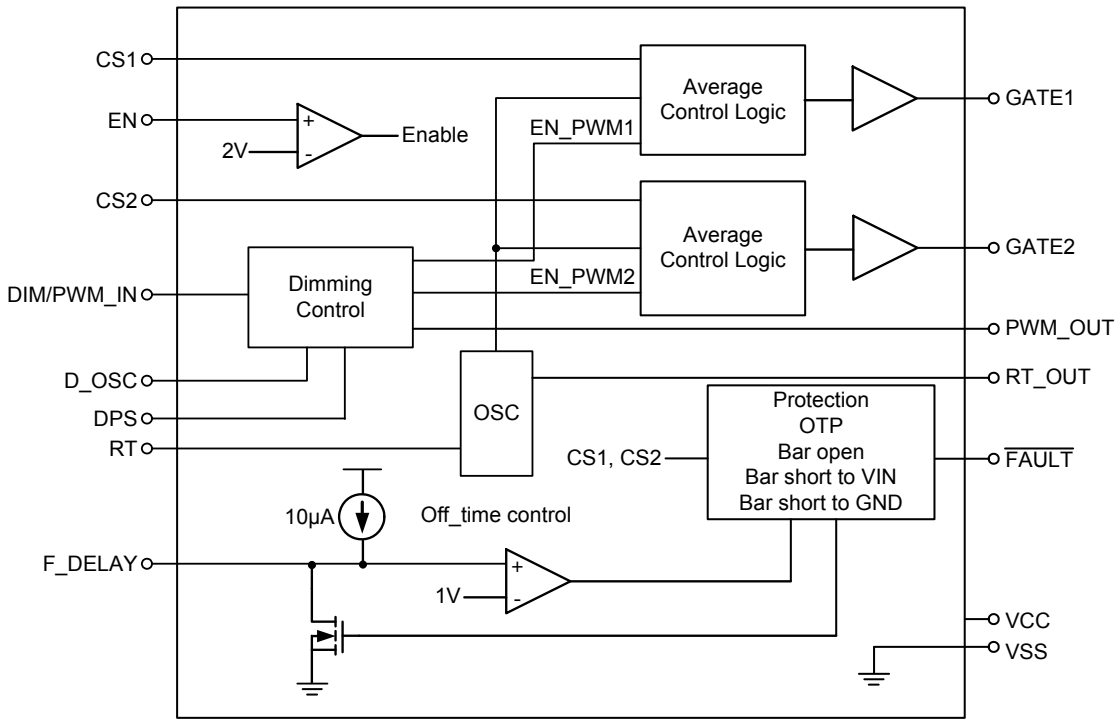
Figure 3. Synchronization for Multiple Channel_Analog

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VCC	Power Supply for PWM Controller.
2	DIM/PWM_IN	Dimming PWM Pulse Input or Analog Voltage Input.
3	RT	Constant off time setting by connecting proper resistor to VSS.
4	D_OSC	For analog dimming, D_OSC should be connected to a capacitor to generate dimming triangle oscillator that is compared with DIM/PWM_IN DC voltage level to generate PWM dimming pulse. For digital dimming, D_OSC should be connected to VSS.
5	F_DELAY	Define $\overline{\text{FAULT}}$ pin output delay by connecting to a proper capacitor to prevent false trigger for UVP and OTP.
6	$\overline{\text{FAULT}}$	Open drain output fault including UVP, OVP, and OTP (Active Low).
7	NC	No Internal Connection.
8	DPS	Smart Phase Shift Dimming Disable Pin. Pull DPS high to disable function.
9	CS1	Channel 1 Current Sense Input.
10	GATE1	Channel 1 Current Gate Driver Output.
11	GATE2	Channel 2 Current Gate Driver Output.
12	CS2	Channel 2 Current Sense Input.
13	EN	Chip Enable (Active High). Enable PWM system, prefer connect to V_{IN} resistive voltage divider to guarantee V_{IN} power ready to prevent from PWM malfunction.
14	RT_OUT	Output for the next RT6010 RT.
15	PWM_OUT	SPD (Smart Phase Shift Dimming) output for slave to synchronize dimming phase shift.
16	VSS	Ground.

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Function Block Diagram



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Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- –0.3V to 15V
- D_OSC, PWM_OUT ---------- –0.3V to 7V
- Others Pins ---------- –0.3V to 15V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-16 ---------- 1.176W
- Package Thermal Resistance (Note 2)
  SOP-16, θ_{JA} ---------- 85°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Control Input Voltage, V_{CC} ---------- 12V ±10%
- Supply Input Voltage, V_{IN} ---------- 8V to 450V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input							
Supply Current		I_{VCC}	V_{BOOT} = 12V, V_{DIM/PWM_IN} = 5V, V_{CSx} = 0.3V	--	4	--	mA
Shutdown Current		I_{SHDN}	Without HV LDO → lower shut down current 1mA	--	--	1	mA
UVLO Threshold		V_{UVLO}		7	8	9	V
UVLO Hysteresis		ΔV_{UVLO}		--	1	--	V
DIM/PWN_IN Threshold Voltage	Logic-High	V_{IH}		2	--	--	V
	Logic-Low	V_{IL}		--	--	0.6	
PWM_OUT Threshold Voltage	Logic-High	V_{OH}		2.4	--	--	V
	Logic-Low	V_{OL}		--	--	0.4	
EN Threshold				--	2	--	V
EN Hysteresis				--	0.2	--	V
PWM Controller							
CS V_{REF}				--	500	--	mV
On-Time		t_{ON}	Recommend	2	8	20	μs
Constant Off-Time		t_{OFF}	Set up by RT(set 66.6kΩ)	0.8	1	1.2	μs
Duty			Recommend customer application duty	40	85	90	%

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Frequency		Defined by t_{OFF}	50	100	300	kHz
Channel-to-Channel Accuracy			--	1.6	--	%
Protection						
OVP		LED string short	--	1	--	V
UVP		LED string no connection	--	100	--	mV
F_DELAY Detect Voltage		Bar open, Bar short to GND, Bar short to V_{IN} & OTP	0.9	1	1.1	V
F_DELAY Current Source			--	10	--	μA
$\overline{FAULT}$ Open Drain Ability			--	--	100	Ω
UVP/OVP Blanking Time			--	500	--	ns
UVP Delay Time		To gate off	--	250	--	ns
OTP			--	160	--	°C
OTP Hysteresis			--	20	--	°C
Dimming						
PWM Dimming Frequency			100	--	600	Hz
Min Dimming Pulse			5	--	--	μs
Forced Dimming Delay Time (High)		Force dimming to H when DIM/PWM_IN goes H for too long	--	25	--	ms
D_OSC Input High-Level	V_{IH}	When operating at analog dimming, we recommend DIM below 2.4V	--	2.5	--	V
D_OSC Input Low-Level	V_{IL}	When operating at analog dimming, we recommend DIM above 1.1V	--	1	--	V
D_OSC Sourcing Current			--	10	--	μA
D_OSC Sinking Current			--	10	--	μA
Driver Capability						
Gate Driver Source		V_{CC} = 12V, V_{GATEX} = 9V	--	80	--	mA
Gate Driver Sink		V_{CC} = 12V, V_{GATEX} = 3V	--	200	--	mA

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

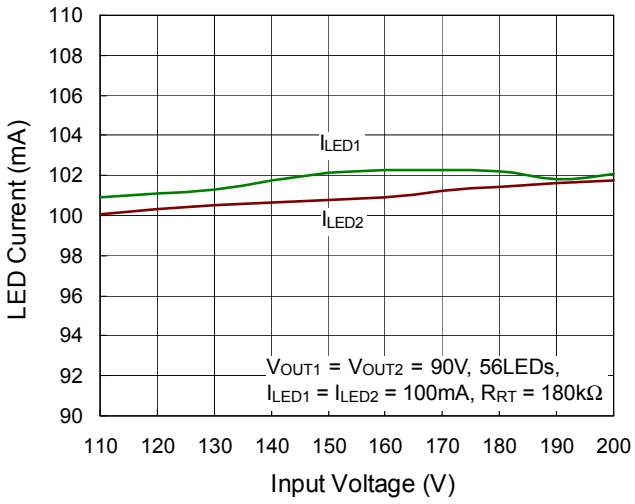
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

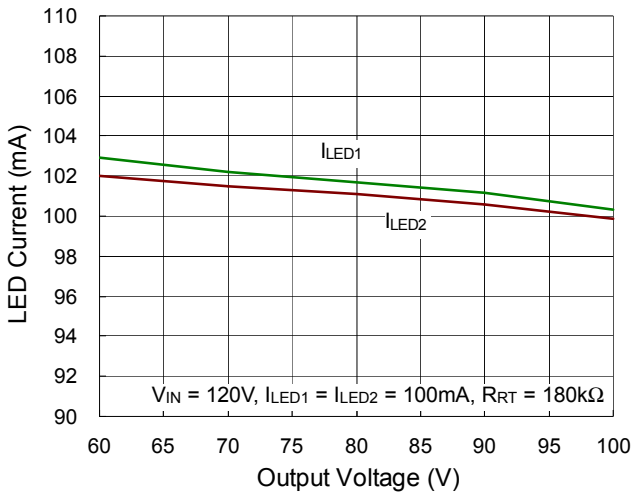
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Typical Operating Characteristics

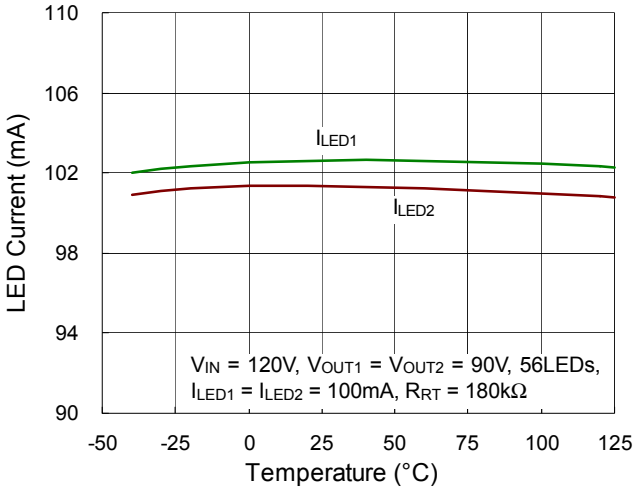
LED Current vs. Input Voltage



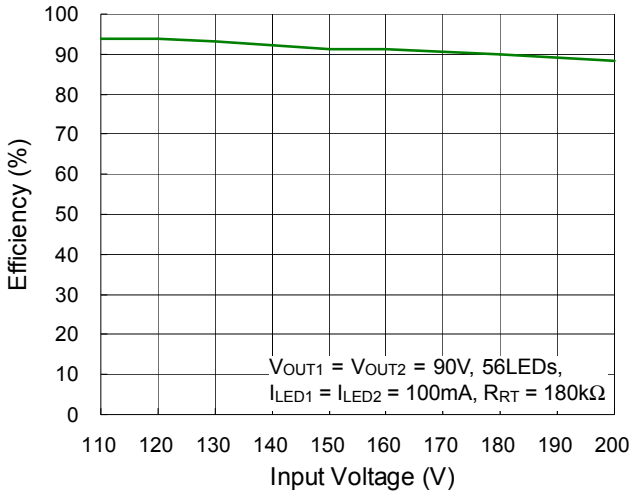
LED Current vs. Output Voltage



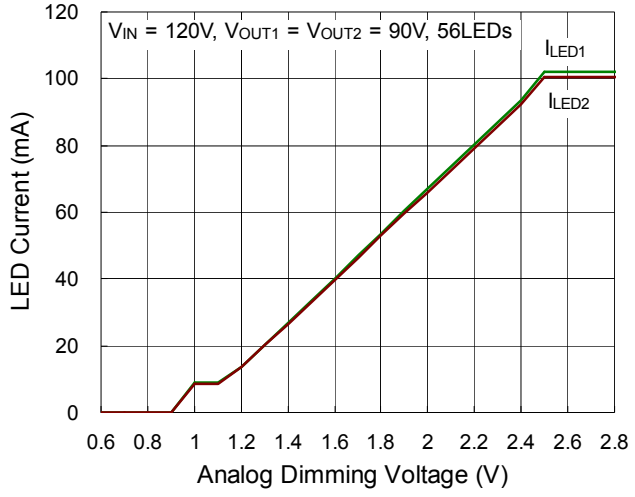
LED Current vs. Temperature



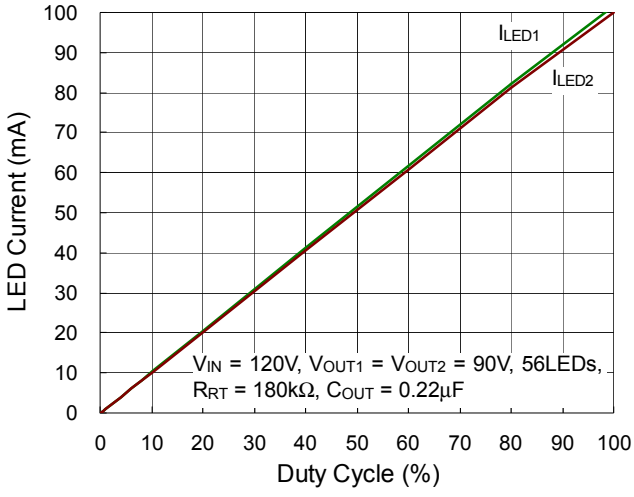
Efficiency vs. Input Voltage



LED Current vs. Analog Dimming Voltage

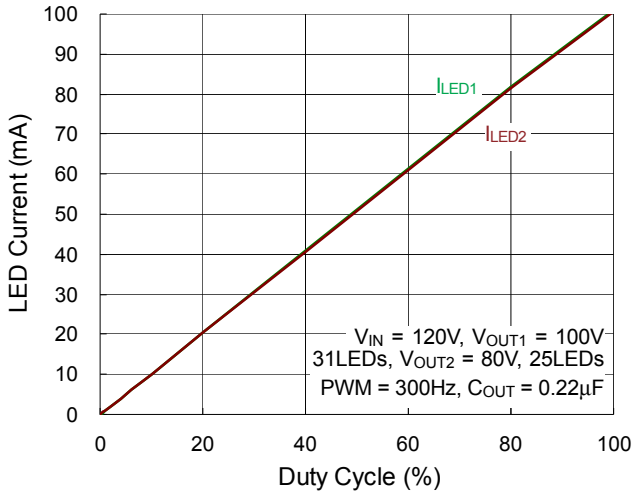


LED Current vs. PWM Duty Cycle

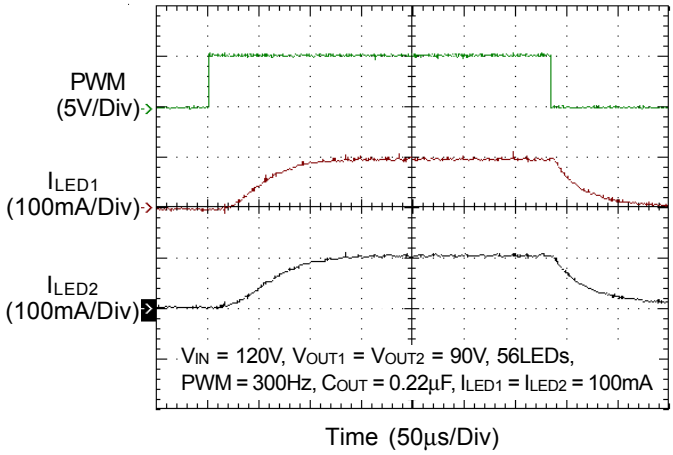


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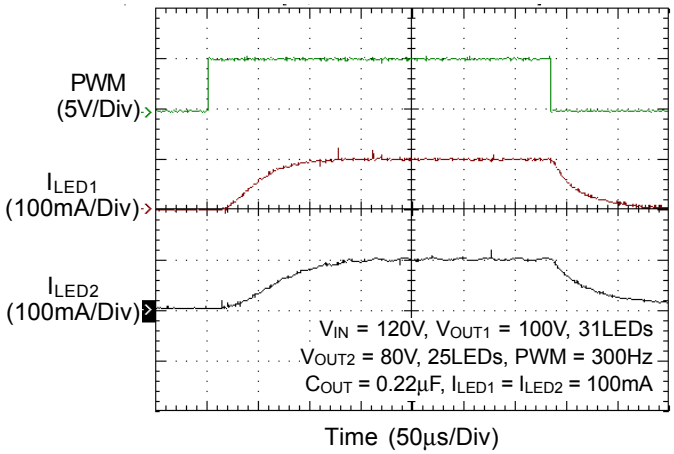
LED Current vs. PWM Duty Cycle



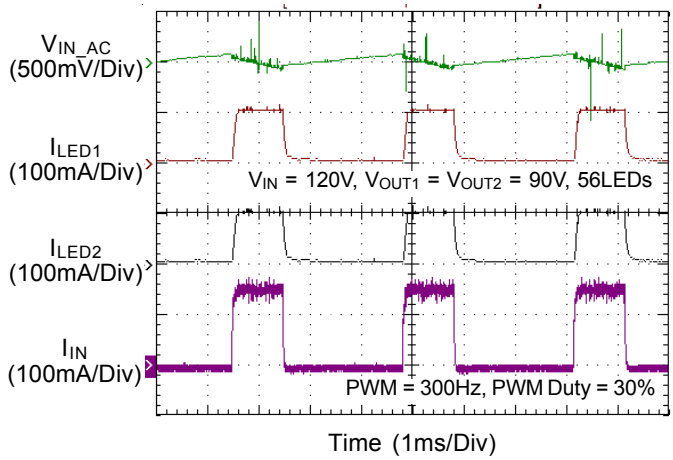
PWM Dimming Response



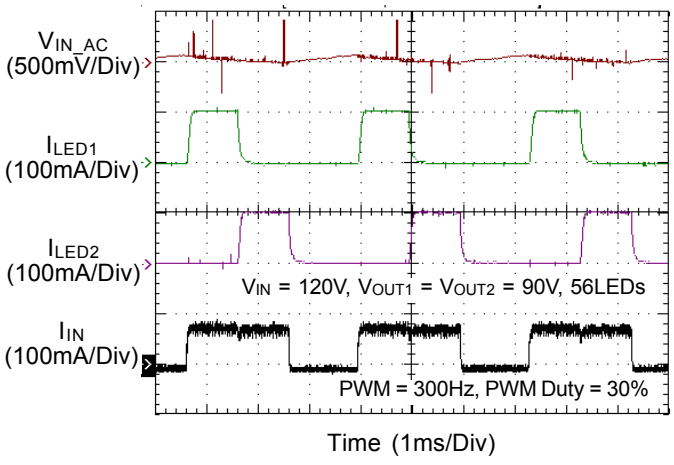
PWM Dimming Response



Non-SPD Function



SPD Function



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Application Information

The RT6010 is a dual channel, high accuracy current control LED backlight buck controller. The controller is capable of providing efficiency higher than 95% for LED backlight use.

Current Setting

Current flow through the inductor during charging period is detected by a sensing resistor, R_{CS}. The RT6010 provides average current mode by dynamically adjusting V_{REF}. The LED average current can be set as :

$$I_{OUT} = \frac{500mV}{R_{CS}}$$

Constant Off-Time Setting

The RT6010 is a constant off-time control IC. The off-time can be set via the external RT pin resistance, R_{RT}. The switching frequency is usually designed to be between 50kHz to 300kHz, so the constant off-time must also meet the following condition :

$$50k \leq \frac{V_{IN} - V_{LED}}{t_{OFF} \times V_{IN}} \leq 300k$$

$$t_{OFF} = 15p \times R_{RT}$$

where t_{OFF} is the constant off-time

Smart Phase Shift Dimming

The RT6010 provides dimming function selection via the DPS pin. If the pin is connected to VCC, the two dimming signals will be in sync for those two channels. On the other hand, if the pin is connected to GND, the two dimming signals will be separated. See Figure below.

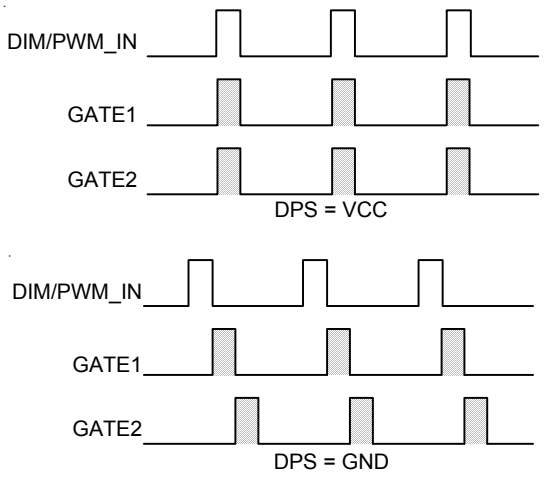


Figure 4. Smart Phase Shift Dimming Via the DPS Pin

Analog Dimming Frequency Setting

The RT6010 not only provides digital dimming, but also analog dimming as well. The analog dimming frequency is set via the D_OSC pin. Note that the minimum dimming duty is 6.667%. The dimming frequency is set according to the following equation :

$$f_{PWM} = 10\mu A / (C_{D_OSC} \times 3V)$$

where C_{D_OSC} is the capacitor connected from the D_OSC pin to GND.

Protection Functions

The RT6010 provides various protection features to prevent damage to the IC during abnormal situations. The features include over voltage protection, under voltage protection, and over temperature protection. The protection flow chart is shown below.

FLT Blanking Delay

An FLT blanking delay function is available for setting the fault delay time to prevent false triggers for UVP and OTP. The delay time is set via the external capacitor connected from the F_DELAY pin to ground. The blanking delay time can be set according to below equation :

$$t = C_{F_DELAY} \times \frac{1V}{10\mu A}$$

where C_{F_DELAY} is the capacitor connected from the F_DELAY pin to GND. After V_{F_DELAY} > 1V, a fault signal will be sent to the $\overline{FAULT}$ pin.

Over Voltage Protection

The RT6010 provides Over Voltage Protection (OVP) when the LED cathode becomes shorted to VIN. The OVP threshold voltage of the CSx pin is approximately 1V. If OVP is triggered during gate-on period, the controller will turn off the MOSFET for 400μs. If OVP occurs consecutively for more than 14 times, the RT6010 will send a fault signal to the FAULT.

Under Voltage Protection

For situations where the LED cathode becomes open or shorted to GND, the RT6010 provides Under Voltage Protection (UVP). The threshold voltage of UVP is approximately 0.1V. If UVP occurs during gate-on period, the RT6010 will send a fault signal to the $\overline{FAULT}$ pin after the fault delay time.

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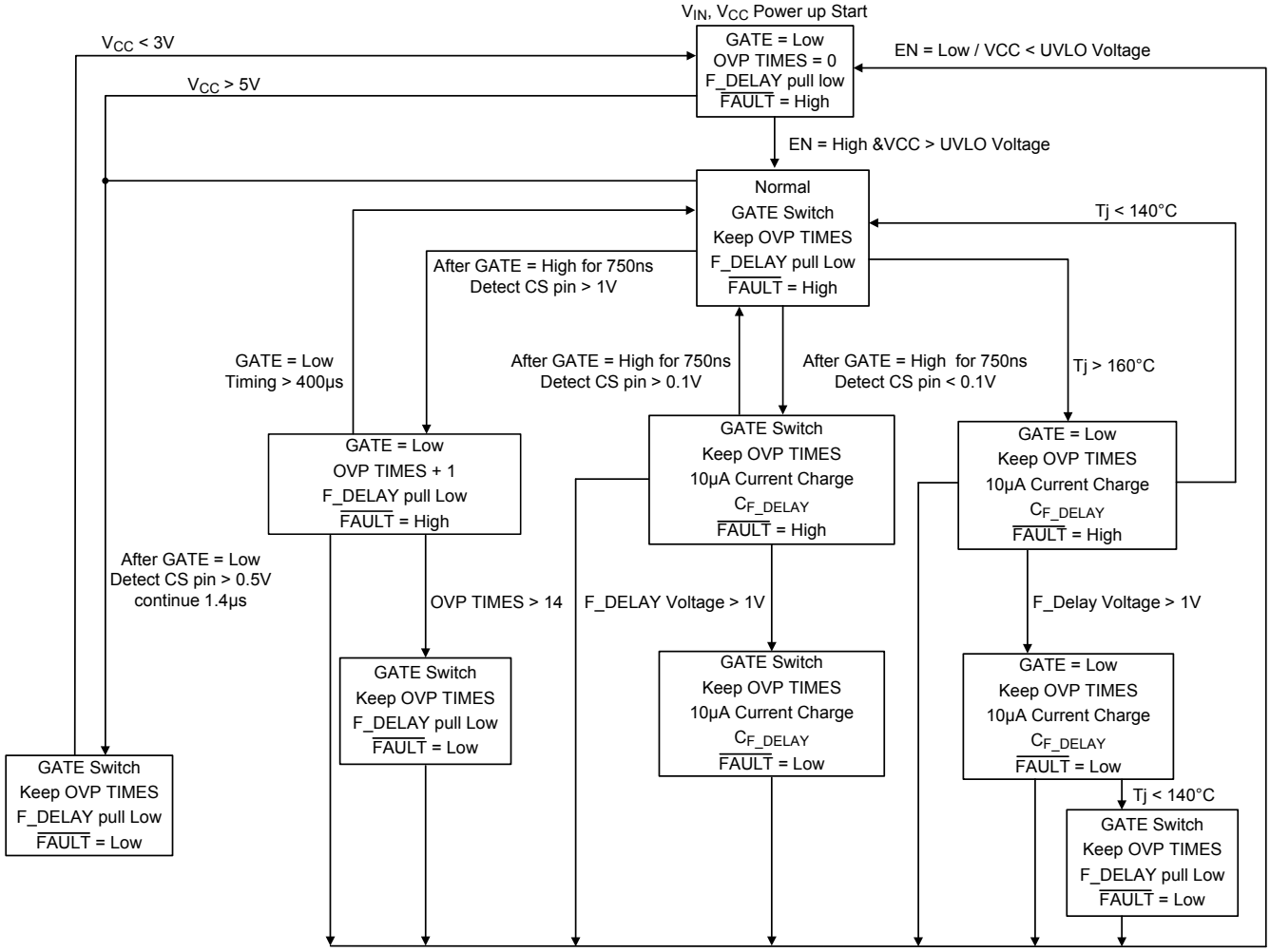


Figure 5. Protection Flow Chart for the RT6010

Over Temperature Protection

To prevent excessive power dissipation from damaging the device, the RT6010 includes an over temperature protection feature. When the temperature rises above OTP temperature, a fault signal will be sent to disable the channel after the fault delay time. After the die temperature falls below OTP hysteresis temperature, the channel will be enabled again.

Inductor Selection

The inductor current ripple is usually designed below 30% of its average current. Hence, the recommended inductor value can be calculated as :

$$L > \frac{V_{LED}}{0.3 \times I_{OUT}} \times t_{OFF}$$

where V_{LED} is the LED series voltage drop, t_{OFF} is the PWM off-time, and I_{OUT} is the LED average current.

MOSFET Selection

For operating at high input or output voltages, the power N-MOSFET switch is typically chosen according to the drain voltage, V_{DS}, rating and low gate charge. Consideration of switch on-resistance, $R_{DS(ON)}$, is usually secondary because switching losses dominate power loss. The gate driving voltage follows the V_{CC} voltage range, which is 12V for normal operation. The N-MOSFET must meet this specification.

Capacitor Selection

Selecting a suitable capacitor can reduce LED current ripple and increase LED life-time. Moreover, if the capacitor has good current sense linearity, it will also ensure that the current matching is accurate. Note that having too large of a capacitance will cause the LED current to respond slowly. The typical value of the capacitor is 0.22µF.

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Diode Selection

Ultra-fast diodes are chosen for their low forward voltage drop and fast switching speed. When selecting ultra-fast diodes, important parameters such as power dissipation, reverse voltage rating, and pulsating peak current should all be taken into consideration. A suitable ultra-fast diode's reverse voltage rating must be greater than the input voltage and its average current rating must exceed the LED average current.

Power On

For power on sequence, it is recommended to connect EN to a resistive voltage divider placed between V_{IN} and GND to prevent UVP malfunction, as shown below.

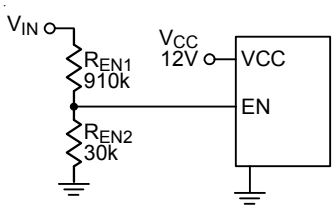


Figure 6. Circuit for Proper Power On Via EN Pin

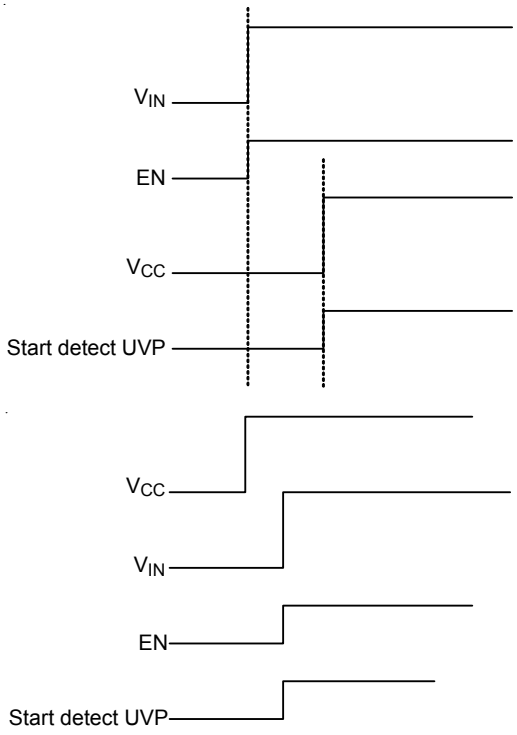


Figure 7. (a) Proper Start Up with R_{EN1}, R_{EN2} Resistors

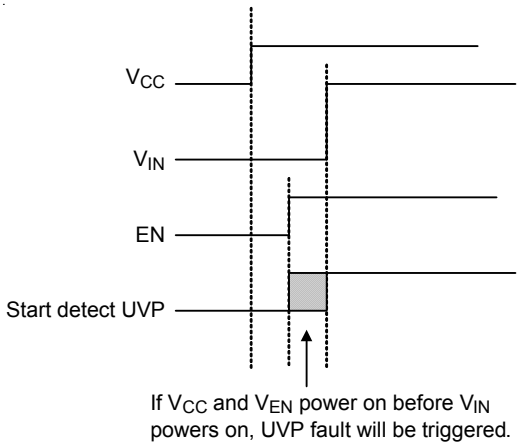


Figure 7. (b) UVP Malfunction without R_{EN1}, R_{EN2} Resistors

Figure 7. Timing Diagram for Power On Sequence

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-16 package, the thermal resistance, θ_{JA}, is 85°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)} = (125°C - 25°C) / (85°C/W) = 1.176W$ for SOP-16 package

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The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

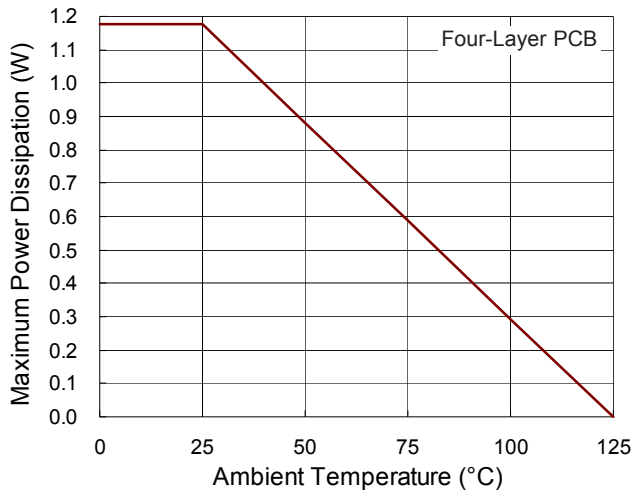


Figure 8. Derating Curve of Maximum Power Dissipation

Layout Considerations

PCB layout plays an important role for the RT6010. Careful layout can decrease switching noise for stable operation and improve performance. For best performance of the RT6010, the following layout guidelines should be strictly followed.

- Current sense feedback resistors, D_OSC capacitor, F_DELAY capacitor, RT resistor and capacitors for VIN and VCC should be placed as close to the controller as possible.
- Keep the power loops as short as possible to prevent voltage spikes caused by current transition from one device to another at high speed as a result of parasitic components on the circuit board. Therefore, all current switching loops should be kept as short as possible with wide traces to minimize the parasitic components.
- Minimize the trace length between the MOSFET and the controller. Since the drivers are integrated in the controller, the driving path should be short and wide to reduce the parasitic inductance and resistance.
- The CS1 and CS2 current sense feedback trace should be kept away from the switching node. Keep the feedback trace close to the CS1 and CS2 pins. Allow large area for VIN inductor trace, FET trace, R_{CS1} and R_{CS2} trace, and GND pad.

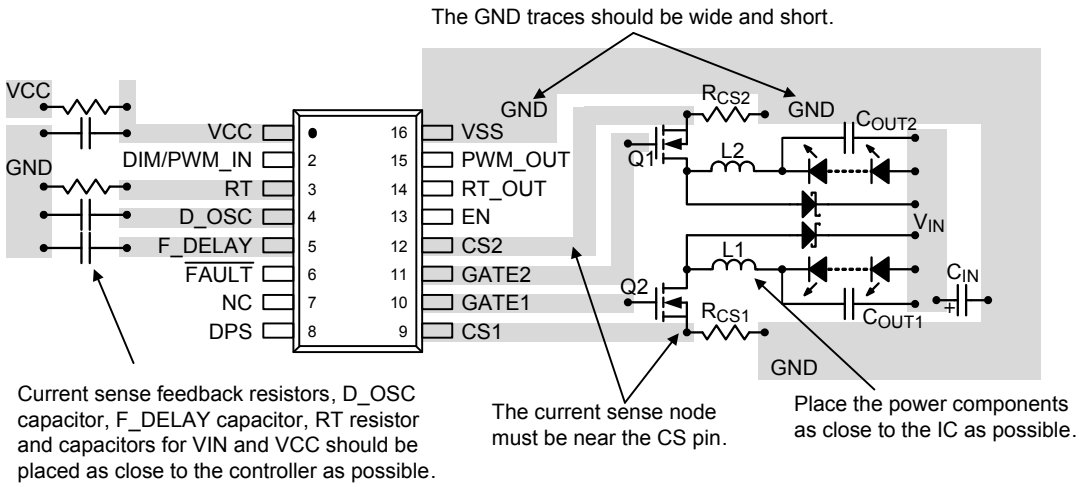
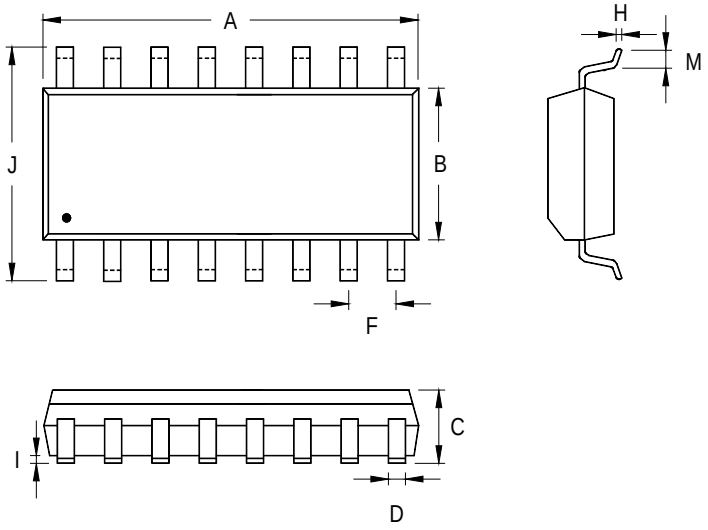


Figure 9. PCB Layout Guide

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Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	9.804	10.008	0.386	0.394
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

16-Lead SOP Plastic Package

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