

Philips Components

Document No.	853-0659
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10130

Latch

Dual D-Type Latch

FEATURES

- Typical propagation delay: 2.5ns
- Typical supply current ($-I_{EE}$): 30mA

DESCRIPTION

The 10130 is a clocked Dual D-Type Latch. Each element can be clocked separately by holding the common clock in the Low-State and using the clock enable inputs for the clocking function. The outputs are latched when the level of the clock is High. All unused inputs must be tied to V_{IL} or V_{EE} .

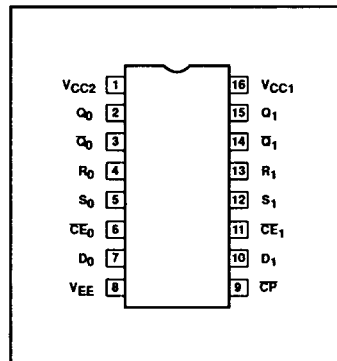
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic DIP	10130N
16-Pin Ceramic DIP	10130F

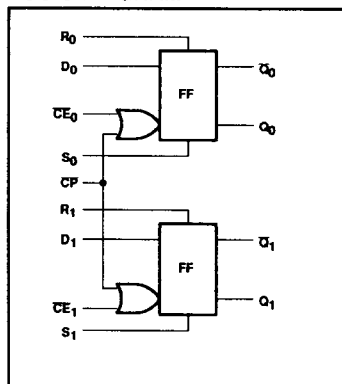
PIN DESCRIPTION

PINS	DESCRIPTION
D_0, D_1	Data Inputs
CP	Clock Input
CE_0, CE_1	Clock Enable Inputs
S_0, S_1	Set Inputs
R_0, R_1	Reset Inputs
$Q_0, Q_1, \bar{Q}_0, \bar{Q}_1$	Data Outputs

PIN CONFIGURATION



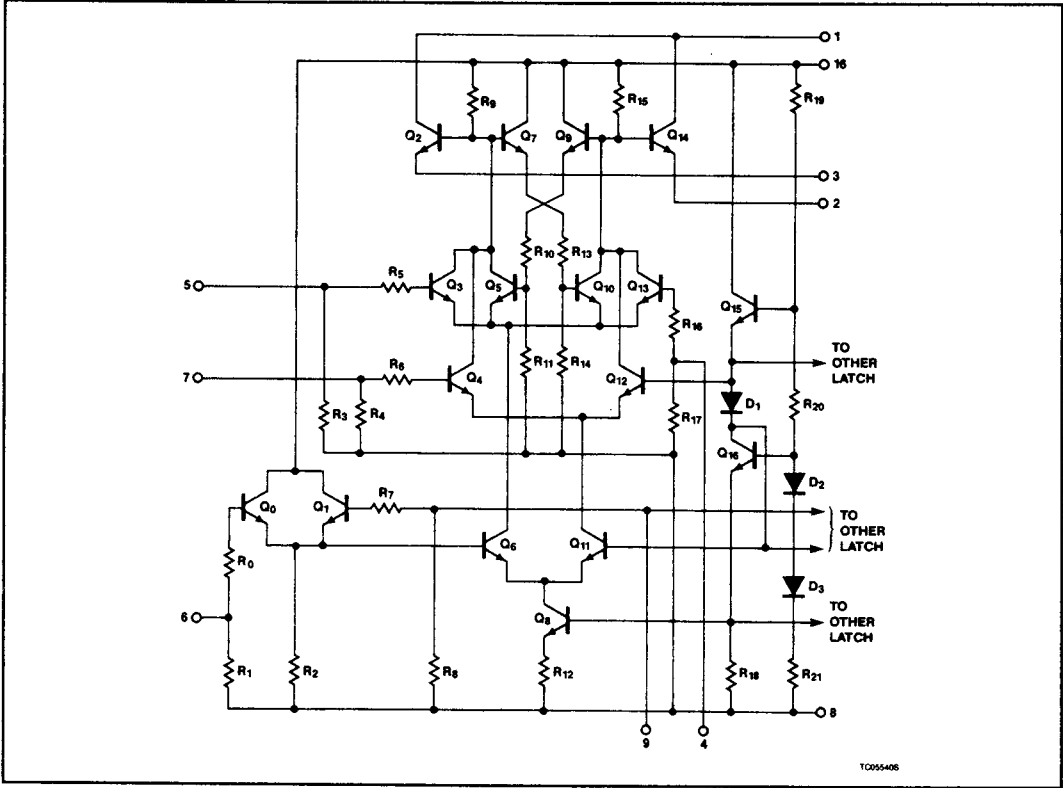
LOGIC DIAGRAM



Latch

10130

SIMPLIFIED SCHEMATIC



FUNCTION TABLES

SYNCHRONOUS OPERATION

INPUTS			OUTPUTS
D _n	CP	C _E	Q _{n+1} *
L	L	L	L
L	L	H	Q _n
L	H	L	Q _n
L	H	H	Q _n
H	L	L	H
H	L	H	Q _n
H	H	L	Q _n
H	H	H	Q _n

* R and S = Low

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS
R	S	Q ₁
L	L	Q
L	H	H
H	L	L
H	H	N

CP or C_E = High
H = High voltage level
L = Low voltage level
N = Not allowed

Latch**10130****ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER		LIMITS	UNIT
V _{EE}	Supply voltage		-8.0 to 0	V
V _{IN}	Input voltage (V _{IN} should never be more negative than V _{EE})		0 to V _{EE}	V
I _O	Output source current (continuous)		-50	mA
T _S	Storage temperature range		-55 to +150	°C
T _J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			-5.2		V
V_{IH}	High level input voltage	$T_A = -30^\circ\text{C}$			-890	mV
		$T_A = +25^\circ\text{C}$			-810	mV
		$T_A = +85^\circ\text{C}$			-700	mV
V_{IHT}	High level input threshold voltage	$T_A = -30^\circ\text{C}$	-1205			mV
		$T_A = +25^\circ\text{C}$	-1105			mV
		$T_A = +85^\circ\text{C}$	-1035			mV
V_{ILT}	Low level input threshold voltage	$T_A = -30^\circ\text{C}$			-1500	mV
		$T_A = +25^\circ\text{C}$			-1475	mV
		$T_A = +85^\circ\text{C}$			-1440	mV
V_{IL}	Low level input voltage	$T_A = -30^\circ\text{C}$	-1890			mV
		$T_A = +25^\circ\text{C}$	-1850			mV
		$T_A = +85^\circ\text{C}$	-1825			mV
T_A	Operating ambient temperature range		-30	+25	+85	°C

NOTE:

When operating at other than the specified V_{EE} voltage (-5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

Latch

10130

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30^\circ\text{C}$ to $+85^\circ\text{C}$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified^{1,3}

SYMBOL	PARAMETER	TEST CONDITIONS ²		LIMITS			UNIT
				MIN.	TYP.	MAX.	
V_{OH}	High level output voltage	$T_A = -30^\circ\text{C}$	For Q_n output, apply V_{IHMAX} to each D_n input, one at a time, with V_{ILMIN} applied to all other inputs.	-1060		-890	mV
		$T_A = +25^\circ\text{C}$		-960		-810	mV
		$T_A = +85^\circ\text{C}$	For $\overline{Q}_n$ output, apply V_{ILMIN} to all inputs.	-890		-700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30^\circ\text{C}$	For Q_n output, apply V_{HT} to each D_n input, one at a time with V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ output, apply V_{ILT} to each D_n input, one at a time, with V_{ILMIN} applied to all other inputs.	-1080			mV
		$T_A = +25^\circ\text{C}$		-980			mV
		$T_A = +85^\circ\text{C}$		-910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30^\circ\text{C}$	For Q_n output, apply V_{ILT} to each D_n input, one at a time with V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ output, apply V_{IHT} to each D_n input, one at a time, with V_{ILMIN} applied to all other inputs.			-1655	mV
		$T_A = +25^\circ\text{C}$				-1630	mV
		$T_A = +85^\circ\text{C}$				-1595	mV
V_{OL}	Low level output voltage	$T_A = -30^\circ\text{C}$	For Q_n output, apply V_{ILMIN} to all inputs. For $\overline{Q}_n$ output, apply V_{IHMAX} to each D_n input, one at a time, with V_{ILMIN} applied to all other inputs.	-1890		-1675	mV
		$T_A = +25^\circ\text{C}$		-1850		-1650	mV
		$T_A = +85^\circ\text{C}$		-1825		-1615	mV
I_{IH}	High level input current	CE_0 , CE_1 inputs	$T_A = -30^\circ\text{C}$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.		360	μA
			$T_A = +25^\circ\text{C}$			220	μA
			$T_A = +85^\circ\text{C}$			220	μA
		$\overline{CP}$ input	$T_A = -30^\circ\text{C}$	Apply V_{IHMAX} to $\overline{CP}$ input with V_{ILMIN} applied to all other inputs.		425	μA
			$T_A = +25^\circ\text{C}$			265	μA
			$T_A = +85^\circ\text{C}$			265	μA
		D_n inputs	$T_A = -30^\circ\text{C}$	Apply V_{IHMAX} to each D_n input under test, one at a time with V_{ILMIN} applied to all other inputs.		455	μA
			$T_A = +25^\circ\text{C}$			285	μA
			$T_A = +85^\circ\text{C}$			285	μA
		R_n inputs	$T_A = -30^\circ\text{C}$	Apply V_{IHMAX} to S_n and CP inputs and R_n input under test, one at a time with V_{ILMIN} applied to all other inputs.		455	μA
			$T_A = +25^\circ\text{C}$			285	μA
			$T_A = +85^\circ\text{C}$			285	μA
		S_n inputs	$T_A = -30^\circ\text{C}$	Apply V_{IHMAX} to R_n and CP inputs and S_n input under test, one at a time with V_{ILMIN} applied to all other inputs.		455	μA
			$T_A = +25^\circ\text{C}$			285	μA
			$T_A = +85^\circ\text{C}$			285	μA
I_{IL}	Low level input current	$T_A = -30^\circ\text{C}$	Apply V_{ILMIN} to each input under test, one at a time, with V_{IHMAX} applied to all other inputs.	0.5			μA
		$T_A = +25^\circ\text{C}$		0.5			μA
		$T_A = +85^\circ\text{C}$		0.3			μA
$-I_{EE}$	V_{EE} supply current	$T_A = -30^\circ\text{C}$				38	mA
		$T_A = +25^\circ\text{C}$			30	35	mA
		$T_A = +85^\circ\text{C}$				38	mA

Latch

10130

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS ²	LIMITS			UNIT
			MIN.	TYP.	MAX.	
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25^\circ\text{C}$		0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation			0.230		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.140		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2\text{V} \pm 0.010\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS								UNIT
			T _A = −30°C		T _A = +25°C			T _A = +85°C			
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
t _{PLH} t _{PHL}	Propagation delay D _n to Q _n , Q̄ _n	Waveform 1	1.00 1.00	3.60 3.60	1.00 1.00	2.50 2.50	3.50 3.50	1.00 1.00	3.80 3.80	ns ns	
t _{PLH} t _{PHL}	Propagation delay R _n to Q _n , Q̄ _n		1.00 1.00	3.60 3.60	1.00 1.00	2.70 2.70	3.50 3.50	1.00 1.00	3.90 3.90	ns ns	
t _{PLH} t _{PHL}	Propagation delay S _n to Q _n , Q̄ _n		1.00 1.00	3.60 3.60	1.00 1.00	2.70 2.70	3.50 3.50	1.00 1.00	3.90 3.90	ns ns	
t _{PLH} t _{PHL}	Propagation delay CP, CE _n to Q _n , Q̄ _n		1.00 1.00	4.30 4.30	1.00 1.00		4.00 4.00	1.00 1.00	4.10 4.10	ns ns	
t _s	Setup time D _n to CP, CE _n	Waveform 2	2.50		2.50			2.50		ns	
t _h	Hold time D _n to CP, CE _n		1.50		1.50			1.50		ns	
t _{TLH} t _{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	3.60 3.60	1.10 1.10	2.70 2.70	3.50 3.50	1.10 1.10	3.80 3.80	ns ns	

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

Latch

10130

AC WAVEFORMS

