ML620Q53x/54x/Q55x (x:6,8) Preliminary

Ultra Low Power 16-bit Microcontroller

GENERAL DESCRIPTION

This LSI family is a high-performance 16-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I2C bus interface (master), supply voltage level detect circuit, RC oscillation type A/D converter, and successive approximation type A/D converter are incorporated around 16-bit CPU nX-U16/100.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. The rich peripheral circuits such as I/O port, Serial interface and Timers are installed. So this LSI family is most suitable for consumer and industry devices that are required for multi-actuation system. And, this LSI has a data flash-memory fill area by software which can be written in.
The on-chip debug function that is installed enables program debugging and programming.

FEATURES

- CPU
  - 16-bit RISC CPU (CPU name: nX-U16/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit operation, bit logic operations, jump, conditional jump, call return stack operation, arithmetic shift, and so on.
  - On-Chip debugs function
  - Minimum instruction execution time
    30.5 µs (@ 32.768 kHz system clock)
    62.5 ns (@16 MHz system clock)

- Built-in coprocessor for multiplication, division, and multiply-accumulate operations
  - Signed or unsigned operation setting
  - Multiplication: 16 bit x 16 bit (operation time 4 cycles)
  - Division: 32 bit / 16 bit (operation time 8 cycles)
  - Division: 32 bit / 32 bit (operation time 16 cycles)
  - Multiply-accumulate (non-saturating): 16 bit x 16 bit + 32bit (operation time 4 cycles)
  - Multiply-accumulate (saturating): 16 bit x 16 bit + 32 bit (operation time 4 cycles)

- Internal memory
  - Supports ISP function (re-writing the program memory area by software)
  - Number of segments

Product name	Flash memory		SRAM	STATUS
	Program area*	Data area		
ML620Q558	256KB (128K × 16bit)	2KB (1K × 16bit)	20KB (10K × 16bit)	Under developing
ML620Q556	128KB (64K × 16bit)	2KB (1K × 16bit)	10KB (5K × 16bit)	Under planning
ML620Q548	256KB (128K × 16bit)	2KB (1K × 16bit)	20KB (10K × 16bit)	Under planning
ML620Q546	128KB (64K × 16bit)	2KB (1K × 16bit)	10KB (5K × 16bit)	Under developing
ML620Q538	256KB (128K × 16bit)	2KB (1K × 16bit)	20KB (10K × 16bit)	Under planning
ML620Q536	128KB (64K × 16bit)	2KB (1K × 16bit)	10KB (5K × 16bit)	Under planning

*: including 1KB of unusable test area

- Interrupt controller (INTC)
  - 1 non-makeable interrupt sources (Internal source: WDT)
  - 52 makeable interrupt sources (Internal sources: 44, External sources: 8)
  - External interrupts and comparator allow edge selection and sampling selection
  - Priority level (4-level) can be set for each interrupt

- Time base counter (TBC)
  - Low-speed time base counter ×2 channels (1 channel is for Real time clock)
  - Generate 32kHz~1Hz signal by dividing Low-speed clock(32.768kHz)
  - Interruption generates function, Frequency correct function.

- Timers (TMR)
  - 8 bits × 12 channels
    (Timer0-B: Available 16-bit x 6 configuration by using Timer0-1 or Timer2-3, Timer4-5, Timer6-7, Timer8-9, TimerA-B)
  - Selection of one shot timer mode is available.
  - External clock can be selected as timer clock.

- Function Timers (FTM)
  - 16-bit × 8 channels
  - 4 operation mode
    [Timer mode] function as 16-bit timer
    [Capture mode] available input signal pulse width and period measurement.
    [PWM1 mode] available 2-duty PWM output by 1 channel
    [PWM2 mode] available 1 pair (positive phase/negative phase) PWM output
  - Output logic switch function (positive logic/negative logic)
  - Interrupt generate (period/duty/capture/accord with setting)
  - Sequential/One shot mode
  - Available dead time setting
  - An event trigger (external pin input interrupt or timer interrupt request) can control start/stop/clear of the timer
  - Available external input emergency stop and emergency stop interrupt

- 3-phase motor PWM
  - Asynchronous PWM (Triangle wave modulation 3-phase PWM) x 1 channel (PWM: 6 output)
  - Available dead time setting

- Watchdog timer (WDT)
  - Non-makeable interrupts and resets (generate interrupt at 1st overflow, generate reset at 2nd overflow)
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s when LSCLK = 32.768 kHz)
  - Watchdog timer status flag :（active/inactive） Watchdog timer active detection function(display active status)

- Real time clock (RTC)
  - 1 channel (Calendar (up to 99 years), Alarm, Time adjustment, 1Hz clock output)
  - Automatic leap year correction
  - Regular interrupts (0.5s, 1s, 1 minute,)
  - Alarm interrupt × 2 channels (day of the week, hour, minute; month, day hour, minute)

- Synchronous serial port (SSIOF)
  - with 4-byte transmits and receives FIFOs (SSIOF) : 2 channels
  - Master/Slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit lengths are selectable
  - Phase/Polarity of clock is selectable
  - Supports slave-select signal

- UART/UART-F
  - without FIFOs (UART) : 1ch
  - with 4-bytes transmits and receives FIFOs (UARTF) : 4ch
  - Full duplex buffer system
  - Communication speed: Settable within the range of 2400bps to 115200bps.
  - Programmable interface (data length, parity, stop bits selectable)
  - bit length, parity/no parity, odd/even parity, 1/2 stop bit selectable
  - positive logic/negative logic selectable
  - LIN bus correspondence is possible by software
  - build-in baud rate generator

- I^2C bus interface (I^2C)
  – Master function × 2 channel
  – Fast mode (400 kbps), standard mode (100 kbps)

- General-purpose ports (PORT)
  – Input port × 2, Input/output port × 88 channels (including secondary or tertiary or fourthly or fifthly functions) on ML620Q556/558.
  – Input port × 2, Input/output port × 68 channels (including secondary or tertiary or fourthly or fifthly functions) on ML620Q546/548.
  – Input port × 2, Input/output port × 50 channels (including secondary or tertiary or fourthly or fifthly functions) on ML620Q536/538.

- Melody driver (MELODY)
  – Tempo: 15 types
  – Scale: 29 types (Melody sound frequency: 508 Hz to 10.922 kHz)
  – Tone length: 63 types
  – Buzzer output mode (4 output modes, 8 buzzer frequencies, 7duty levels at 4.096kHz /15 duty levels at other buzzer frequencies)

- RC oscillation type A/D converter (RC-ADC)
  – Time division × 2 channels
  – 24-bit counter

- Successive approximation type A/D converter (SA-ADC)
  – Input × 20 channels on ML620Q558/556/548/546、Input × 16 channels on ML620Q538/536
  – Conversion time : 1.25us
  – 10-bit A/D converter
  – Starting by trigger of Timer/FTM function

- Analog Comparator (CMP)
  – Input x 2 channel
  – Operation voltage range: VDD = 1.8V ~ 5.5V
  – Common mode input voltage : 0.2V to V_{DD}－0.2V
  – Input offset voltage : 30mV(max)
  – Interrupt allow edge selection and sampling are selectable

- Voltage Level Supervisor (VLS)
  – Threshold voltages: selectable from 16 levels
  – interrupt or reset generate are selectable

- Low Level Detector(LLD)
  – Judgment Voltage: 1.8V±0.2V
  – Available low level detecction reset generation.

- Reset
  – Reset by the RESET_N pin
  – Reset by power-on detection
  – Reset by overflow of watchdog timer (WDT)
  – Reset by Voltage Level Supervisor(VLS)
  – Reset by Low Level Detector(LLD)

- Clock
  – Low-speed clock: (This LSI cannot guarantee the operation without low-speed clock)
    Crystal oscillation (32.768 kHz)
    External clock input (30kHz to 36kHz)
    Built-in RC oscillation (32.768kHz)
    Detects the stop of the crystal oscillation and automatically change to built-in RC oscillation
  – High-speed clock:
    Crystal/Ceramic oscillation (16MHz)

External clock input (300 kHz to 16 MHz)
Built-in RC oscillation (16MHz)

- Flash programming
  - Supports remap function（Software remap, Hardware remap）
  - In self programming (ISP)

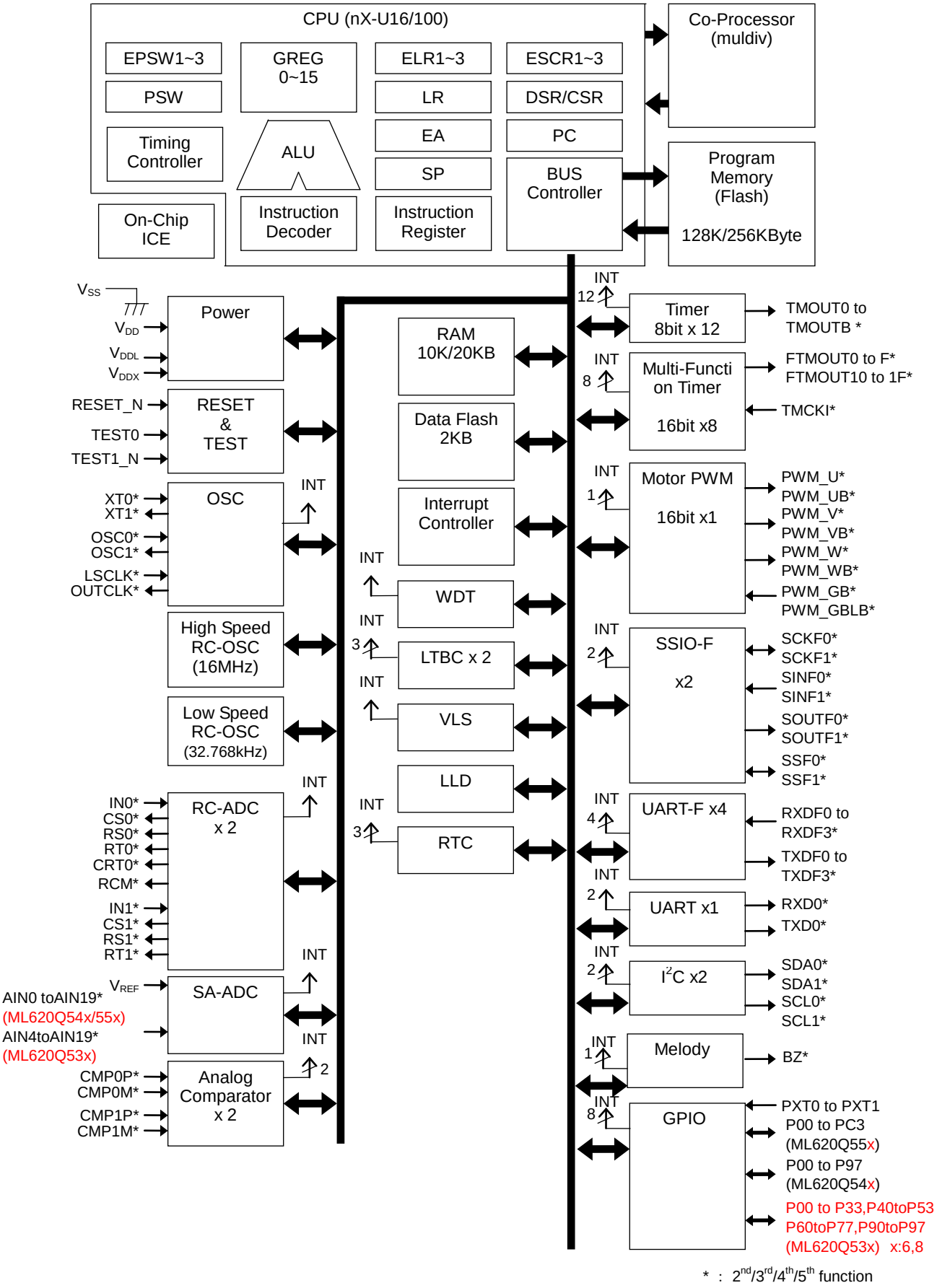
- Power management
  - HALT mode: Instruction execution by CPU is suspended. All peripheral circuits keep operating states.
  - HALT-H mode: Instruction execution by CPU is suspended. Stop of high-speed oscillation automatically. All peripheral circuits keep operating states.
  - DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits (Timer, LTBC) keep operating states.
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8,1/16,1/32 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - 64-pin plastic TQFP （ML620Q536/Q538） Tray
  - 80-pin plastic TQFP （ML620Q546/Q548） Tray
  - 100-pin plastic TQFP （ML620Q556/Q558） Tray

- Guaranteed operating range
  - Operating temperature (ambient) : –40°C to +95°C
  - Operating voltage: V_{DD} = 1.8V to 5.5V

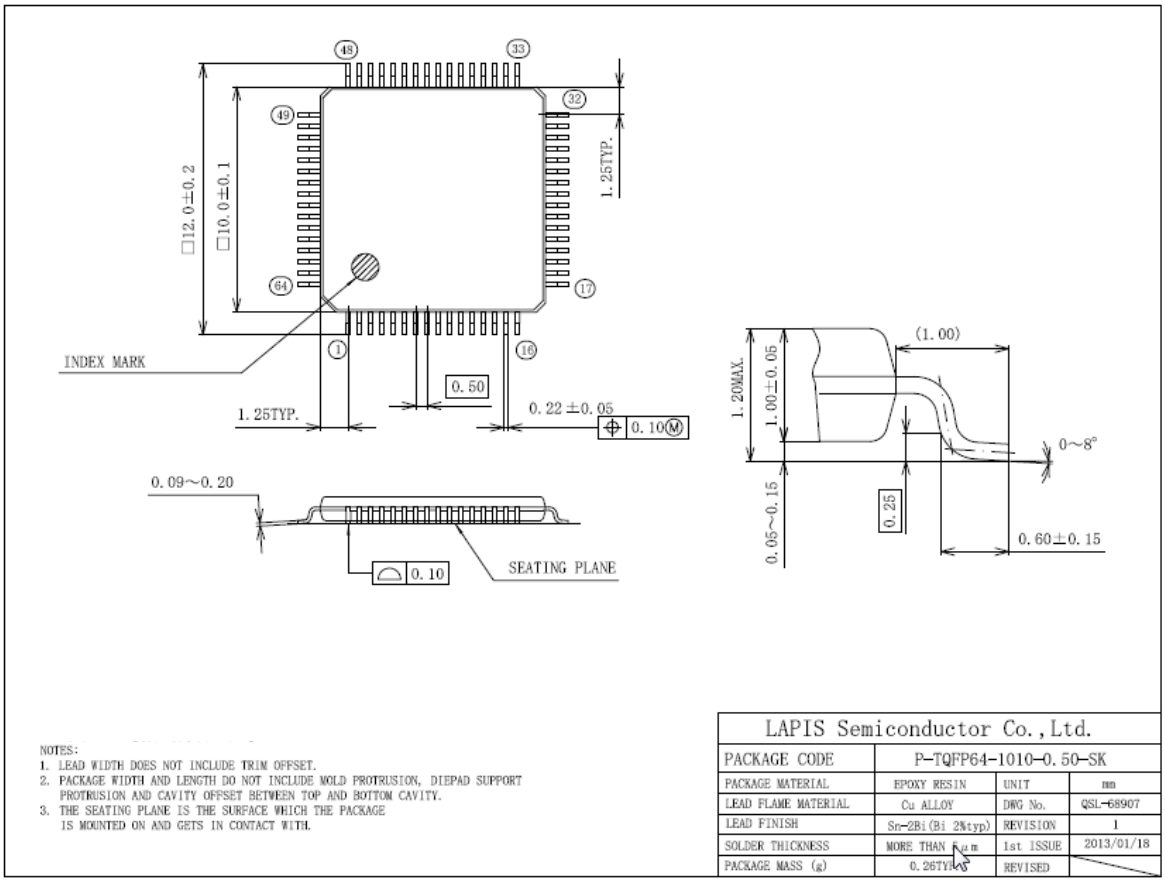
BLOCK DIAGRAM

ML620Q536/538/546/548/556/558/ Block Diagram



PACKAGE DIMENSIONS

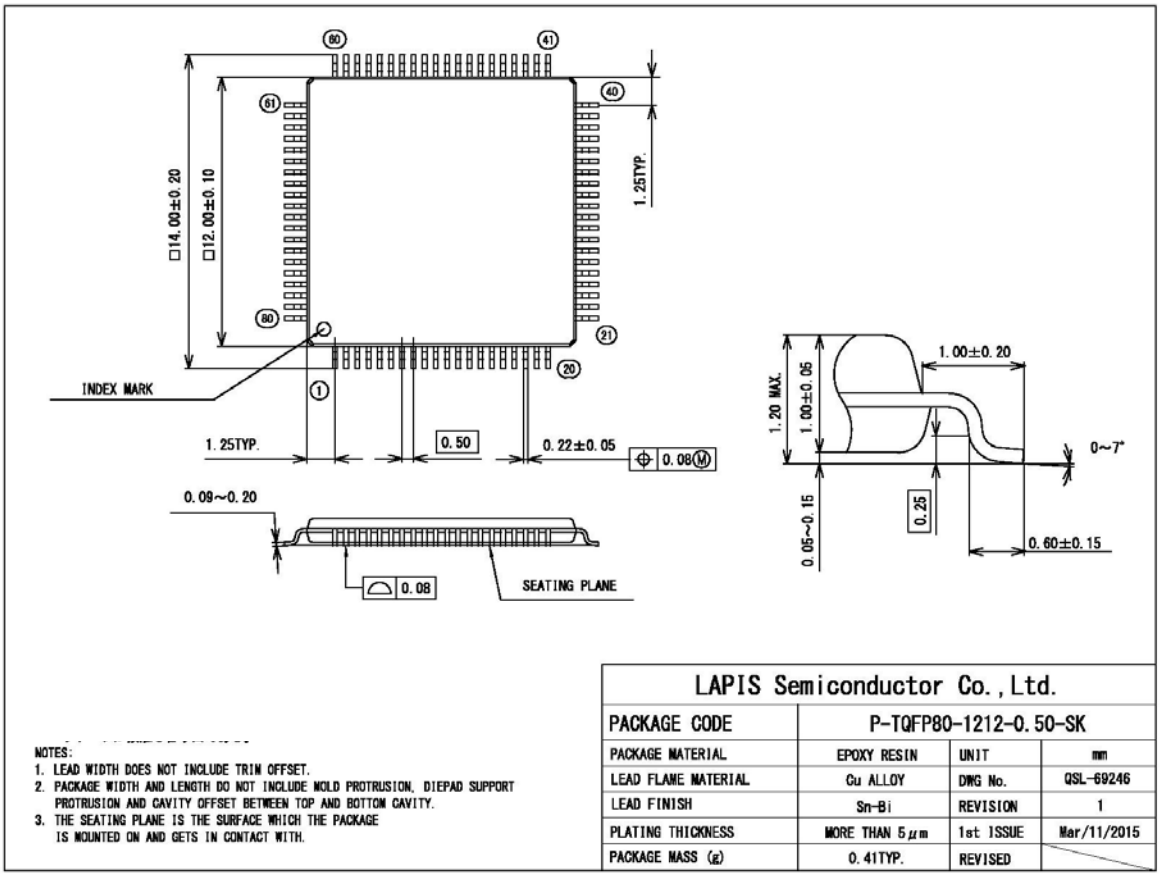
ML620Q536/538 Package Dimensions



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TQFP64-1010-0.50-SK		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FRAME MATERIAL	Cu ALLOY	DWG No.	QSL-68907
LEAD FINISH	Sn-2Bi(Bi 2%typ)	REVISION	1
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	2013/01/18
PACKAGE MASS (g)	0.26TYP.	REVISED	

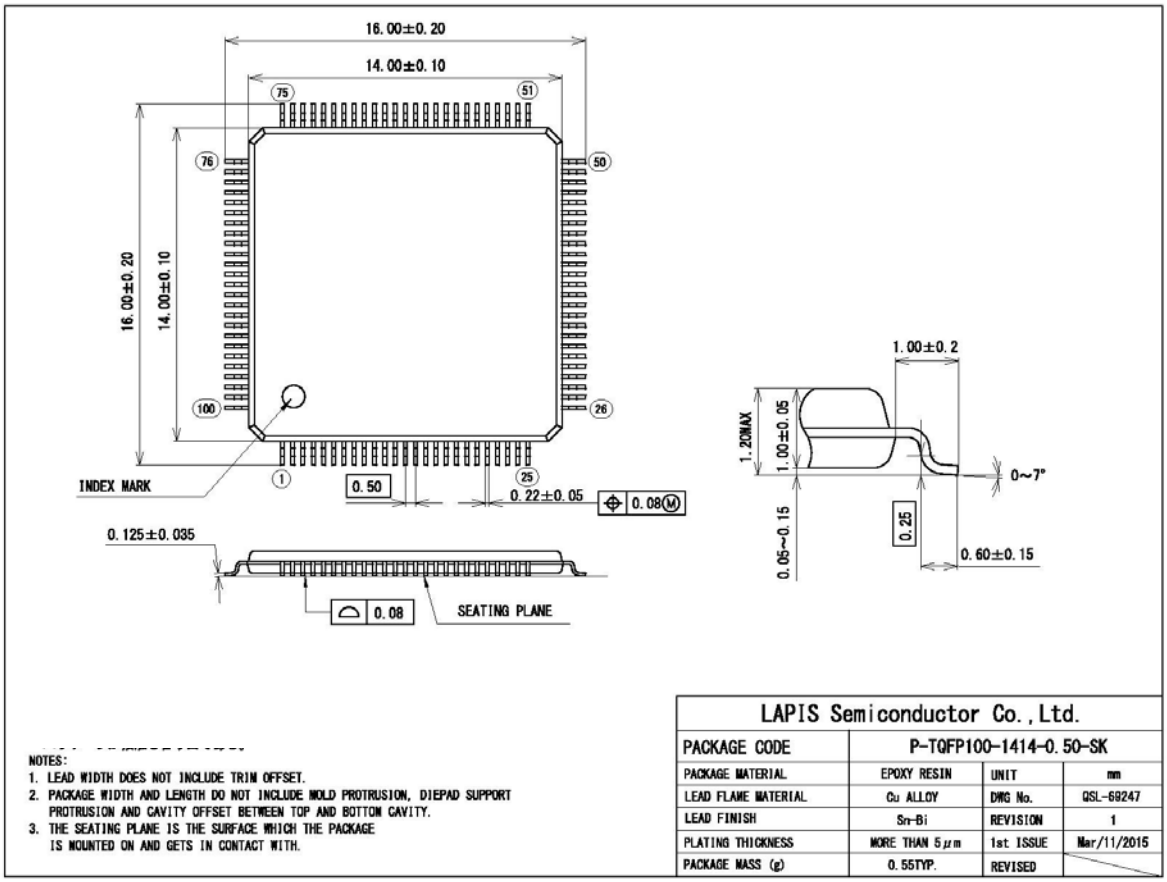
ML620Q546/548 Package Dimensions



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TQFP80-1212-0.50-SK		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FRAME MATERIAL	Cu ALLOY	DWG No.	QSL-69246
LEAD FINISH	Sn-Bi	REVISION	1
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Mar/11/2015
PACKAGE MASS (g)	0.41TYP.	REVISED	

ML620Q556/558 Package Dimensions



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Previous Edition	
PEDL620Q546_558-01	Dec.1.2013	—	—	1st release edition
PEDL620Q546_558-02	Apr.24.2014	1to4	1to4	Modification of Features
		5	5	Modification of block diagram
PEDL620Q546_558-03	Jun.14.2014	2	2	Modification of resolution of SA-ADC.
		3	3	Modification of number of general I/O ports.
		4	4	Modification of function of block control
		5	5	Modification of block diagram
PEDL620Q546_558-04	Nov.20.2014	3	3	Modification of number of general I/O ports.
		4	4	Modification of block diagram
PEDL620Q546_558-05	Apr.30.2015	1 to 8	1 to8	Modification of general description. Added package dimensions.
PEDL620Q53x_54x_55x-06	Jly.30.2015	1 to 8	1 to8	Added ML620Q536/538/548/556 Information.

Notes

1) The information contained herein is subject to change without notice.

2) Although LAPIS Semiconductor is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. LAPIS Semiconductor shall have no responsibility for any damages arising out of the use of our Products beyond the rating specified by LAPIS Semiconductor.

3) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

4) The technical information specified herein is intended only to show the typical functions of the Products and examples of application circuits for the Products. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Semiconductor or any third party with respect to the information contained in this document; therefore LAPIS Semiconductor shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.

5) The Products are intended for use in general electronic equipment (i.e. AV/OA devices, communication, consumer systems, gaming/entertainment sets) as well as the applications indicated in this document.

6) The Products specified in this document are not designed to be radiation tolerant.

7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a LAPIS Semiconductor representative: transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

8) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.

9) LAPIS Semiconductor shall have no responsibility for any damages or injury arising from non-compliance with the recommended usage conditions and specifications contained herein.

10) LAPIS Semiconductor has used reasonable care to ensure the accuracy of the information contained in this document. However, LAPIS Semiconductor does not warrant that such information is error-free and LAPIS Semiconductor shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

11) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. For more details, including RoHS compatibility, please contact a ROHM sales office. LAPIS Semiconductor shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

12) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

13) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Semiconductor.

Copyright 2014-2015 LAPIS Semiconductor Co., Ltd.

LAPIS Semiconductor Co.,Ltd.

2-4-8 Shinyokohama, Kouhoku-ku,
Yokohama 222-8575, Japan
http://www.lapis-semi.com/en/