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FAIRCHILD SEMICONDUCTOR®

November 2013

FAN6757— mWSaver® PWM Controller

Features

- Single-Ended Topologies, such as Flyback and Forward Converters
- mWSaver® Technology
  - Achieves Low No-Load Power Consumption: <50 mW at 230 V_{AC} (EMI Filter Loss Included)
  - Eliminates X Capacitor Discharge Resistor Loss with AX-CAP® Technology
  - Linearly Decreases Switching Frequency to 23 kHz
  - Burst Mode Operation at Light-Load Condition
  - 500 V High-Voltage JFET Startup Circuit to Eliminate Startup Resistor Loss
- Highly Integrated with Rich Features
  - Proprietary Frequency Hopping to Reduce EMI
  - High-Voltage Sampling to Detect Input Voltage
  - Peak-Current-Mode Control with Slope Compensation
  - Cycle-by-Cycle Current Limiting with Line Compensation
  - Leading-Edge Blanking (LEB)
  - Built-In 7 ms Soft-Start
- Advanced Protections
  - Brown-In/Brownout Recovery
  - Internal Overload / Open-Loop Protection (OLP)
  - V_{DD} Under-Voltage Lockout (UVLO)
  - V_{DD} Over-Voltage Protection (V_{DD} OVP)
  - Over-Temperature Protection (OTP)
  - Current-Sense Short-Circuit Protection (SSCP)

Description

The FAN6757 is a next-generation Green Mode PWM controller with innovative mWSaver® technology, which dramatically reduces standby and no-load power consumption, enabling conformance to worldwide Standby Mode efficiency guidelines.

An innovative AX-CAP® method minimizes losses in the EMI filter stage by eliminating X-cap discharge resistors while meeting IEC61010-1 safety requirements.

Protections ensure safe operation of the power system in various abnormal conditions. A proprietary frequency-hopping function decreases EMI emission. Built-in synchronized slope compensation allows more stable Peak-Current-Mode control over a wide range of input voltage and load conditions. The proprietary internal line compensation ensures constant output power limit over the entire universal line voltage range.

Requiring a minimum number of external components, FAN6757 provides a basic platform that is well suited for cost-effective flyback converter designs that require extremely low standby power consumption.

Applications

Flyback power supplies that demand extremely low standby power consumption, such as:

- Adapters for Notebooks, Printers, Game Consoles
- Open-Frame SMPS for LCD TV, LCD Monitors, Printers

Ordering Information

Part Number	Protections(1)				Operating Temperature Range	Package	Packing Method
	OLP	OVP	OTP	SSCP			
FAN6757MRMX	A/R	L	L	A/R	-40 to +105°C	8-Pin, Small-Outline Package (SOP)	Tape & Reel

Note:

1. A/R = Auto Recovery Mode protection, L = Latch Mode protection.

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Application Diagram

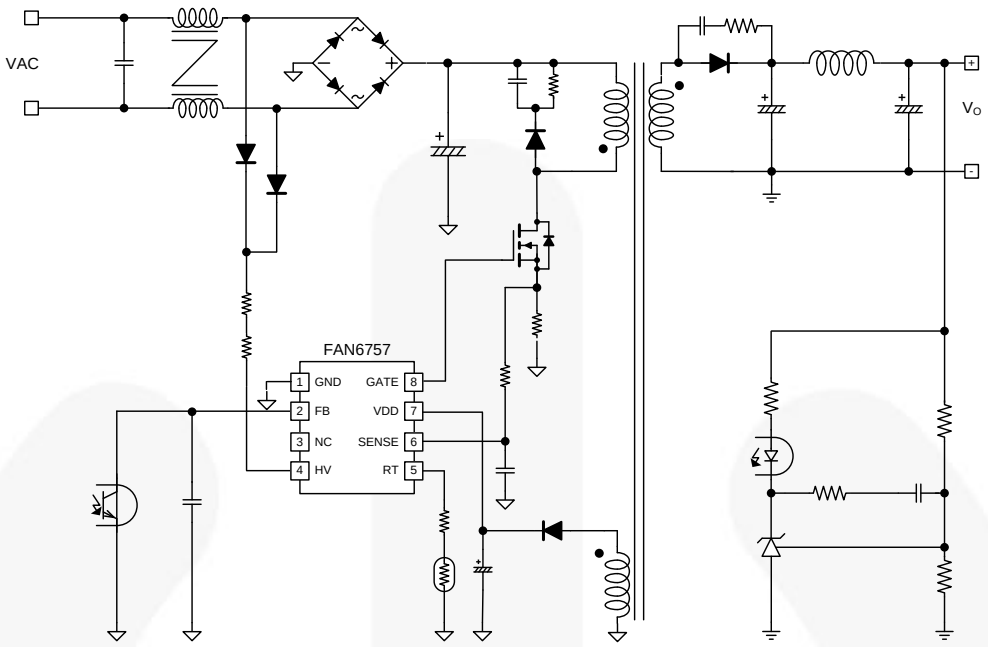


Figure 1. Typical Application

Internal Block Diagram

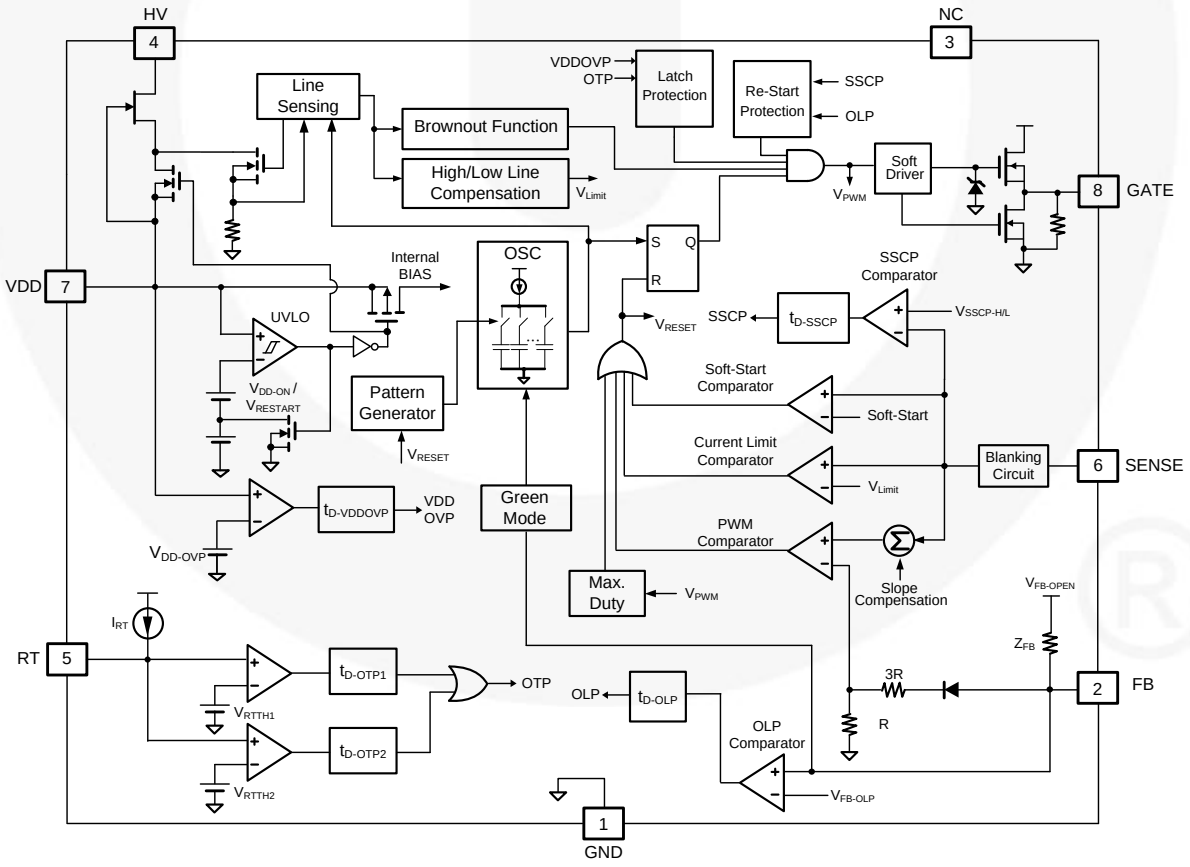
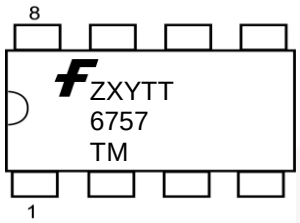


Figure 2. Functional Block Diagram

Marking Information



Z - Plant Code
X - 1-Digit Year Code
Y - 1-Digit Week Code
TT - 2-Digit Die Run Code
T - Package Type (M=SOP)
M - Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

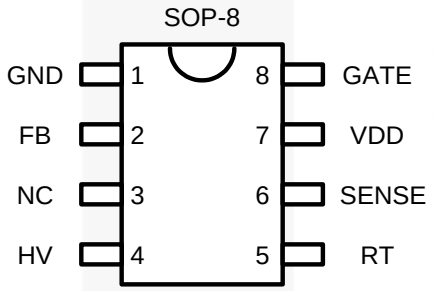


Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. This pin is used for the ground potential of all the pins. A 0.1 µF decoupling capacitor placed between VDD and GND is recommended.
2	FB	**Feedback**. The output voltage feedback information from the external compensation circuit is fed into this pin. The PWM duty cycle is determined from this pin and the current-sense signal from Pin 6. The FAN6757 performs open-loop protection: if the FB voltage is higher than a threshold voltage (around 4.6 V) for more than 57.5 ms, the controller latches off the PWM.
3	NC	No connection
4	HV	**High-Voltage Startup**. This pin is connected to the line input or bulk capacitor, via 200 kΩ resistors, to achieve brownout and high/low line compensation. If the voltage of the HV pin is lower than the brownout voltage (AC line peak voltage less than 100 V) and lasts for 65 ms, PWM output turns off. High/low line compensation dominates the OCP level and cycle-by-cycle current limit, to solve the unequal OCP level and power-limit problems under universal input.
5	RT	**Over-Temperature Protection**. An external NTC thermistor is connected from this pin to the GND pin. The impedance of the NTC thermistor decreases at high temperatures. Once the voltage of the RT pin drops below the threshold voltage, the controller latches off the PWM. If the RT pin is not connected to an NTC resistor for over-temperature protection, it is recommended to place one 100 kΩ resistor to ground to prevent from noise interference. This pin is limited by an internal clamping circuit.
6	SENSE	**Current Sense**. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting.
7	VDD	**Power Supply**. The internal protection circuit disables PWM output as long as V_{DD} exceeds the OVP trigger point.
8	GATE	**Gate Drive Output**. The totem-pole output driver for the power MOSFET. It is internally clamped below 14.5 V.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
V_{VDD}	DC Supply Voltage[1,2]			30	V
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V
V_{SENSE}	SENSE Pin Input Voltage		-0.3	7.0	V
V_{RT}	RT Pin Input Voltage		-0.3	7.0	V
V_{HV}	HV Pin Input Voltage			500	V
P_D	Power Dissipation (T_A＜50°C)			400	mW
Θ_{JA}	Thermal Resistance (Junction-to-Air)			150	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Human Body Model, JEDEC:JESD22-A114	All Pins except HV Pin[3]		6.5	kV
	Charged Device Model, JEDEC:JESD22-C101	All Pins except HV Pin[3]		2.0	

Notes:
1. All voltage values, except differential voltages, are given with respect to the network ground terminal.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. ESD level on the HV pin is CDM=1 kV and HBM=1 kV.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. We does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{HV}	Resistance on HV Pin	150	200	250	kΩ

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Electrical Characteristics

V_{DD}=15 V and T_J=T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD} Section						
V_{DD-ON}	Threshold Voltage to Startup	V_{DD} Rising	16	17	18	V
V_{UVLO}	Threshold Voltage to Stop Switching in Normal Mode	V_{DD} Falling	5.5	6.5	7.5	V
$V_{RESTART}$	Threshold Voltage to enable HV Startup to Charge V_{DD} in Normal Mode	V_{DD} Falling		4.7		V
V_{DD-OFF}	Threshold Voltage to Stop Operating in Protection Mode	V_{DD} Falling	10	11	12	V
V_{DD-OLP}	Threshold Voltage to Enable HV Startup to Charge V_{DD} in Protection Mode	V_{DD} Falling	6	7	8	V
V_{DD-LH}	Threshold Voltage to Release Latch Mode	V_{DD} Falling	3.5	4.0	4.5	V
V_{DD-AC}	Minimum Voltage of VDD Pin for Enabling Brown-in to Avoid Startup Fail		V_{UVLO} +2.5	V_{UVLO} +3.0	V_{UVLO} +3.5	V
I_{DD-ST}	Startup Current	V_{DD}=V_{DD-ON} – 0.16 V			30	µA
I_{DD-OP1}	Supply Current in PWM Operation	V_{DD}=15 V, V_{FB}=3 V, Gate Open			1.8	mA
I_{DD-OP2}	Supply Current when PWM Stops	V_{DD}=15 V, V_{FB} <1.4 V, Gate Off			800	µA
I_{DD-OLP}	Internal Sink Current when V_{DD-OLP}<V_{DD}<V_{DD-OFF} in Protection Mode	V_{DD} = V_{DD-OLP} + 0.1 V	90	140	190	µA
I_{LH}	Internal Sink Current when V_{DD}<V_{DD-OLP} in Latch-Protection Mode	V_{DD} = 5 V	30			µA
V_{DD-OVP}	Threshold Voltage for V_{DD} Over-Voltage Protection		23.5	24.5	25.5	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time		110	205	300	µs
HV Section						
I_{HV}	Inherent Current Limit of HV Pin	V_{AC}=90 V (V_{DC}=120 V), V_{DD}=0 V	1.50	3.25	5.00	mA
V_{AC-OFF}	Threshold Voltage for Brownout	DC Source Series, R=200 kΩ to HV Pin	90	100	110	V
V_{AC-ON}	Threshold Voltage for Brown-In	DC Source Series, R=200 kΩ to HV Pin	100	110	120	V
$\triangle V_{AC}$	V_{AC-ON} – V_{AC-OFF}	DC Source Series, R=200 kΩ to HV Pin	8	12	16	V
$t_{D-AC-OFF}$	Debounce Time for Brownout		40	65	90	ms
t_{S-WORK}	Work Period of HV-Sampling Circuit in Standby Mode	V_{FB}<V_{FB-ZDC}	95	140	185	ms
t_{S-REST}	Rest Period of HV-Sampling Circuit in Standby Mode	V_{FB}<V_{FB-ZDC}	180	260	320	ms
V_{HV-DIS}	HV Discharge Threshold	R_{HV}=200 kΩ to HV Pin	V_{DC} ×0.45	V_{DC} ×0.51	V_{DC} ×0.56	V
$t_{D-HV-DIS}$	Debounce Time for HV Discharge		75	115	155	ms
t_{HV-DIS}	HV Discharge Time		360	510	660	ms

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Electrical Characteristics

V_{DD}=15 V and T_J=T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Oscillator Section						
f_{OSC}	Frequency in Normal Mode	Center Frequency	62	65	68	kHz
		Hopping Range (V_{FB}>V_{FB-N})	±3.55	±4.25	±4.95	
t_{HOP}	Hopping Period	V_{FB}>V_{FB-G}	5.12	6.40	7.68	ms
f_{OSC-G}	Green-Mode Frequency	Center Frequency	20	23	26	kHz
		Hopping Range (Increase V_{FB} from V_{FB-G} Until Hopping Starts)	±1.25	±1.50	±1.75	
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11 V to 22 V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-40 to 105°C			5	%
Feedback Input Section						
A_V	Input Voltage to Current-Sense Attenuation		1/4.50	1/3.75	1/3.00	V/V
Z_{FB}	Pull High Impedance at Normal Mode		17	19	21	kΩ
$V_{FB-OPEN}$	Output High Voltage	FB Pin Open	5.2	5.4	5.6	V
V_{FB-OLP}	FB Open-Loop Trigger Level		4.3	4.6	4.9	V
t_{D-OLP}	Delay of FB Pin Open-Loop Protection		45.0	57.5	70.0	ms
V_{FB-N}	Green-Mode Entry FB Voltage		2.6	2.8	3.0	V
V_{FB-G}	Green-Mode Ending FB Voltage		2.1	2.3	2.5	V
$V_{FB-ZDCR}$	FB Threshold Voltage for Zero-Duty Recovery at Normal Mode		1.9	2.1	2.3	V
V_{FB-ZDC}	FB Threshold Voltage for Zero-Duty at Normal Mode		1.8	2.0	2.2	V
Current-Sense Section						
t_{PD}	Delay to Output			100	250	ns
t_{LEB}	Leading-Edge Blanking Time		200	265	330	ns
$V_{LIMIT-L}$	Current Limit at Low Line (V_{AC-RMS}=86 V)	V_{DC}=122 V, Series R=200 kΩ to HV	0.43	0.46	0.49	V
$V_{LIMIT-H}$	Current Limit at High Line (V_{AC-RMS}=259 V)	V_{DC}=366 V, Series R=200 kΩ to HV	0.36	0.39	0.42	V
V_{SSCP-L}	Threshold Voltage for SENSE Short-Circuit Protection	V_{DC}=122 V, Series R=200 kΩ to HV	30	50	70	mV
V_{SSCP-H}	Threshold Voltage for SENSE Short-Circuit Protection	V_{DC}=366 V, Series R=200 kΩ to HV	80	100	120	mV
$t_{ON-SSCP}$	On Time for $V_{SSCP-(L/H)}$ Checking	V_{SENSE}<$V_{SSCP-(L/H)}$	4.00	4.55	5.10	µs
t_{D-SSCP}	Debounce Time for SENSE Short-Circuit Protection	V_{SENSE}<$V_{SSCP-(L/H)}$	110	170	230	µs
t_{SS}	Soft-Startup Time	Startup Time	5	7	9	ms

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Electrical Characteristics

V_{DD}=15 V and T_J=T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
GATE Section						
DCY_{MAX}	Maximum Duty Cycle		75.0	82.5	90.0	%
V_{GATE-L}	Gate Low Voltage	V_{DD}=15 V, I_O=50 mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=12 V, I_O=50 mA	8			V
t_r	Gate Rising Time (10~90%)	V_{DD}=15 V, C_L=1 nF	85	110	135	ns
t_f	Gate Falling Time (10~90%)	V_{DD}=15 V, C_L=1 nF	30	40	50	ns
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22 V	11.0	14.5	18.0	V
RT Section						
I_{RT}	Output Current of RT Pin			100		µA
V_{RTTH1}	Threshold Voltage, Latch Protection (Generally Used for External OTP Triggering)	V_{RTTH2} < V_{RT} < V_{RTTH1}, After 14.5 ms Latch Off	1.000	1.035	1.070	V
V_{RTTH2}	Second Latch Protection Threshold Voltage	V_{RTTH2} < 0.7 V, After 185 µs Latch Off	0.65	0.70	0.75	V
R_{OTP}	Value of V_{RTTH1}/I_{RT}		9.66	10.50	11.34	kΩ
t_{D-OTP1}	Debounce Time, First Latch Protection Triggering	V_{RTTH2} < V_{RT} < V_{RTTH1}	11.0	14.5	18.0	ms
t_{D-OTP2}	Debounce Time, Second Latch Protection Triggering	V_{RT}< V_{RTTH2}	110	185	260	µs
Over-Temperature Protection Section (OTP)						
T_{OTP}	Protection Junction Temperature			+135		°C
$T_{RESTART}$	Restart Junction Temperature			T_{OTP}-25		°C

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Typical Characteristics

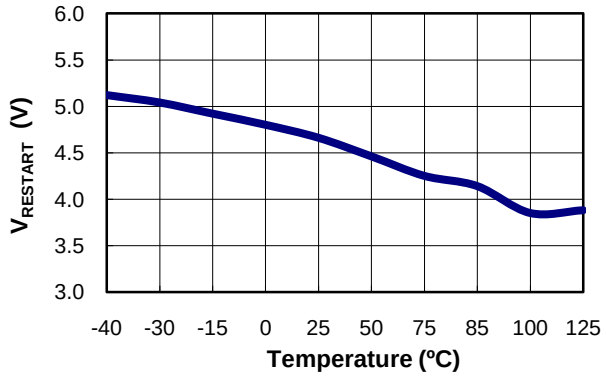


Figure 5. $V_{RESTART}$ vs. Temperature

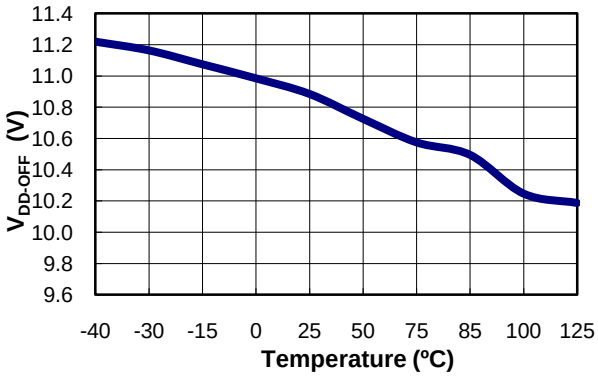


Figure 6. V_{DD-OFF} vs. Temperature

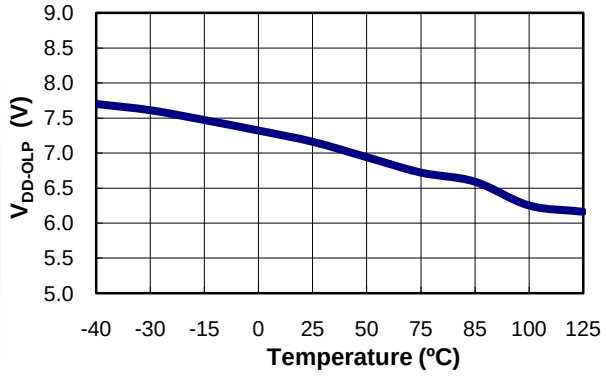


Figure 7. V_{DD-OLP} vs. Temperature

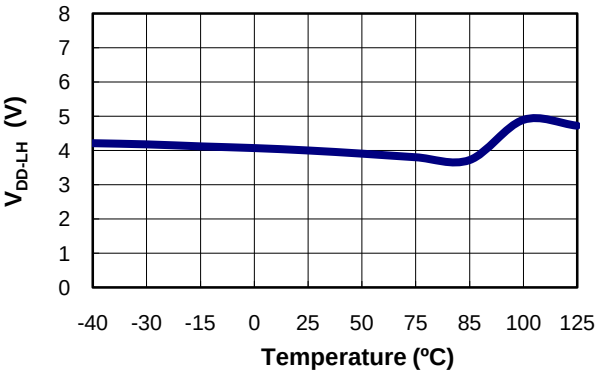


Figure 8. V_{DD-LH} vs. Temperature

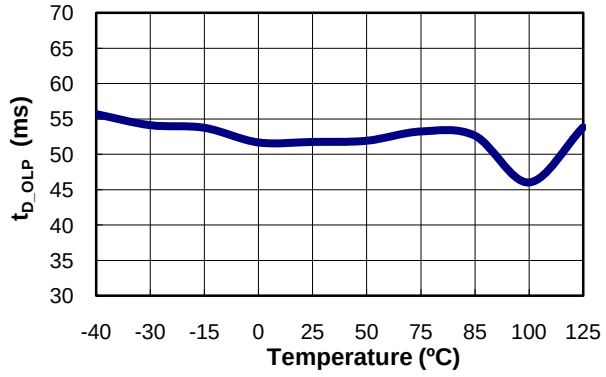


Figure 9. T_{D-OLP} vs. Temperature

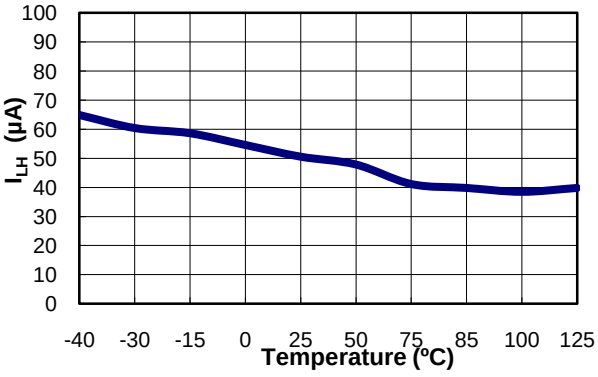


Figure 10. I_{LH} vs. Temperature

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Typical Characteristics

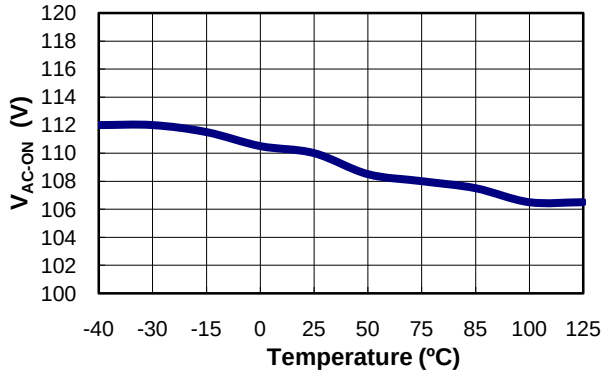


Figure 11. V_{AC-ON} vs. Temperature

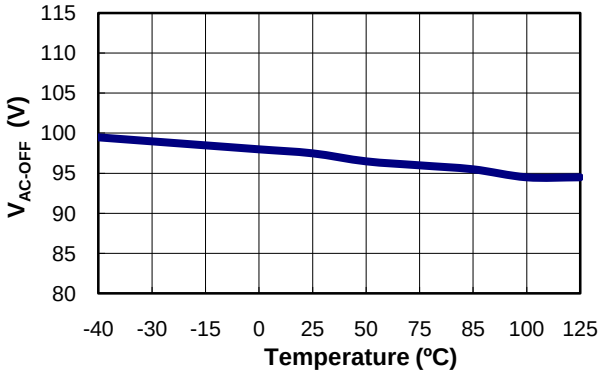


Figure 12. V_{AC-OFF} vs. Temperature

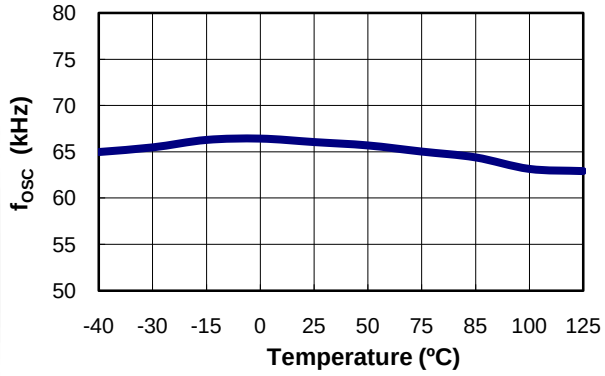


Figure 13. f_{OSC} vs. Temperature

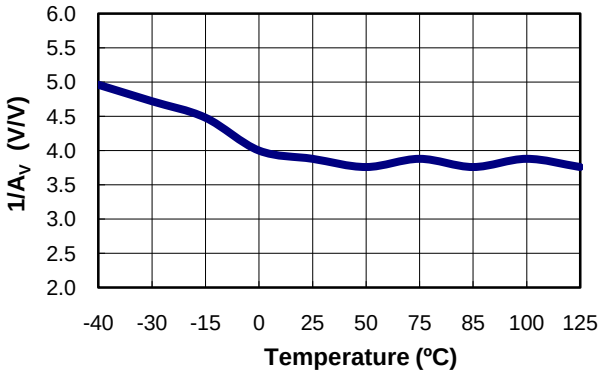


Figure 14. $1/A_V$ vs. Temperature

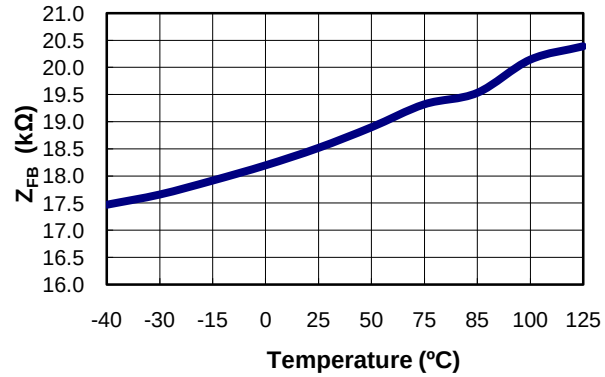


Figure 15. Z_{FB} vs. Temperature

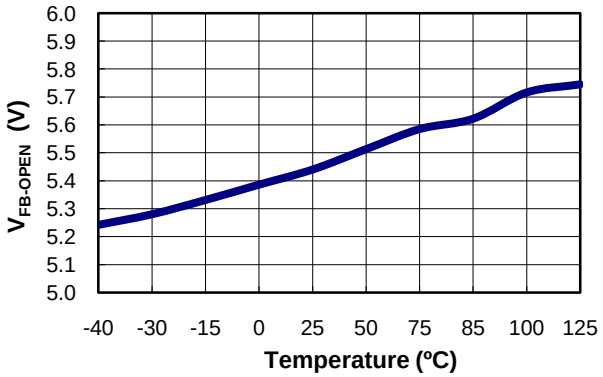


Figure 16. $V_{FB-OPEN}$ vs. Temperature

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Typical Characteristics

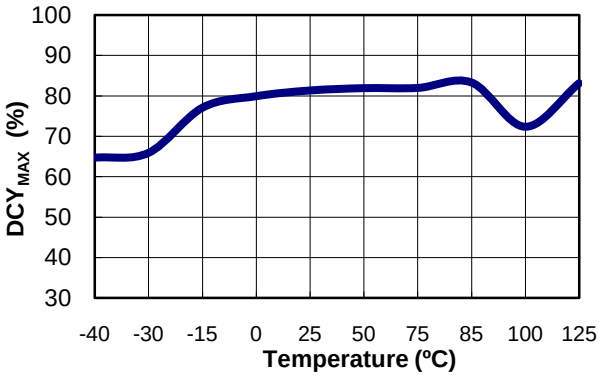


Figure 17. DCY_{MAX} vs. Temperature

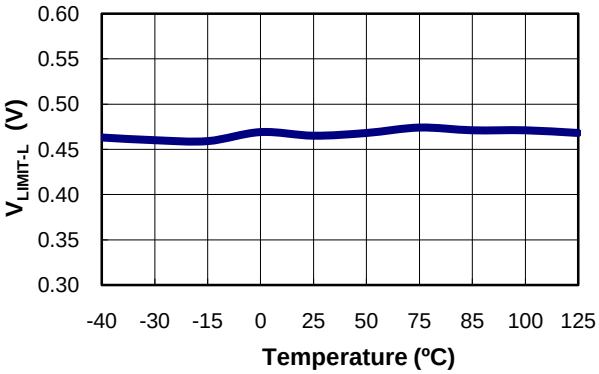


Figure 18. $V_{LIMIT-L}$ vs. Temperature

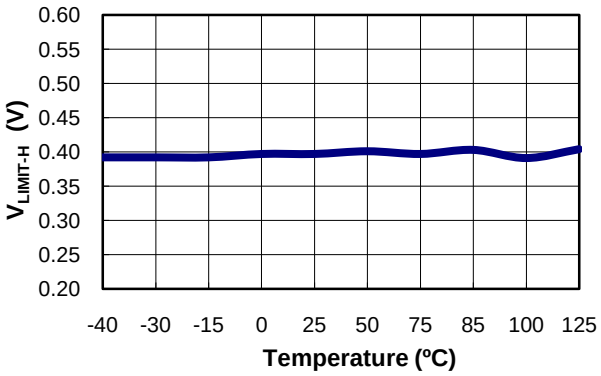


Figure 19. $V_{LIMIT-H}$ vs. Temperature

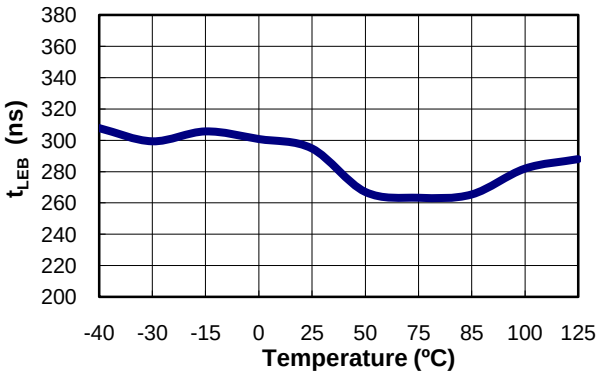


Figure 20. t_{LEB} vs. Temperature

Functional Description

Current Mode Control

FAN6757 employs peak current-mode control, as shown in Figure 21. An opto-coupler (such as the H11A817A) and a shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. The built-in slope compensation stabilizes the current loop and prevents sub-harmonic oscillation.

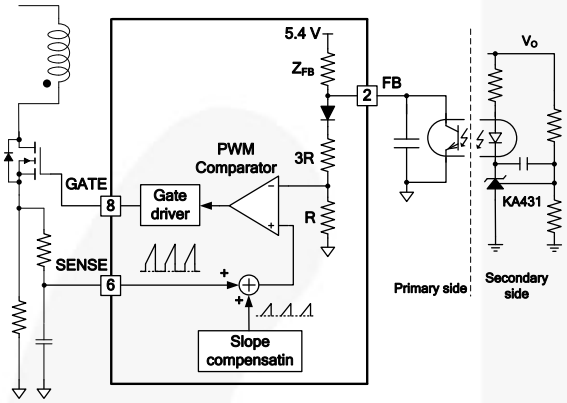


Figure 21. Current Mode Control Circuit Diagram

Green-Mode Operation

The FAN6757 modulates the PWM frequency as a function of the FB voltage to improve the medium- and light-load efficiency, as shown in Figure 22. Since the output power is proportional to the FB voltage in current-mode control, the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is fixed at 65 kHz. Once V_{FB} decreases below V_{FB-N} (2.8 V), the PWM frequency starts linearly decreasing from 65 kHz to 23 kHz to reduce switching losses. As V_{FB} drops to V_{FB-G} (2.3 V), where switching frequency is decreased to 23 kHz, the switching frequency is fixed to avoid acoustic noise.

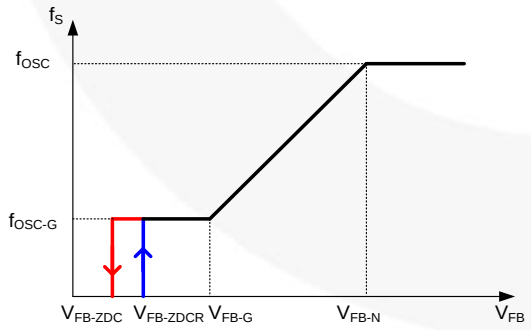


Figure 22. V_{FB} vs. PWM Frequency

When V_{FB} falls below V_{FB-ZDC} (2.0 V) as load decreases further, the FAN6757 enters Burst Mode operation, where PWM switching is disabled. Then the output voltage starts to drop, causing the feedback voltage to rise. Once V_{FB} rises above $V_{FB-ZDCR}$ (2.1 V), switching resumes. Burst Mode alternately enables and disables switching, reducing switching loss for lower power consumption, as shown in Figure 23.

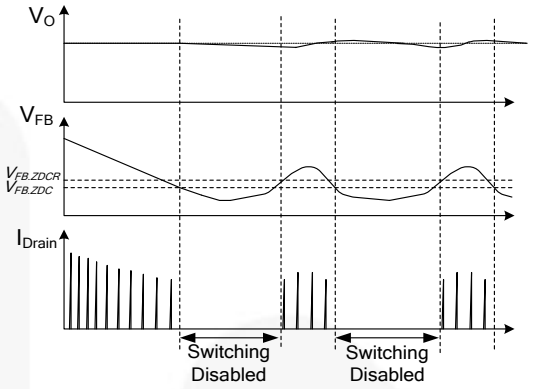


Figure 23. Burst Switching in Green Mode

Operating Current

In normal conditions, operating current is less than 1.8 mA (I_{DD-OP1}). When V_{FB}<1.4 V, operating current is further reduced below 800 µA (I_{DD-OP2}) by disabling several blocks of the FAN6757. The low operating current improves light-load efficiency and reduces the requirement of V_{DD} hold-up capacitance.

High-Voltage Startup and Line Sensing

The HV pin is typically connected to the AC line input through two external diodes and one resistor (R_{HV}), as shown in Figure 24. When the AC line voltage is applied, the V_{DD} hold-up capacitor is charged by the line voltage through the diodes and resistor. After V_{DD} reaches the turn-on threshold voltage (V_{DD-ON}), the startup circuit charging V_{DD} capacitor is switched off and V_{DD} is supplied by the auxiliary winding of the transformer. Once the FAN6757 starts up, it continues operation until V_{DD} drops below 6.5 V (V_{UVLO}). The IC startup time with a given AC line input voltage is:

$$t_{STARTUP} = R_{HV} \cdot C_{DD} \cdot \ln \frac{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi}}{V_{AC-IN} \cdot \frac{2\sqrt{2}}{\pi} - V_{DD-ON}} \quad (1)$$

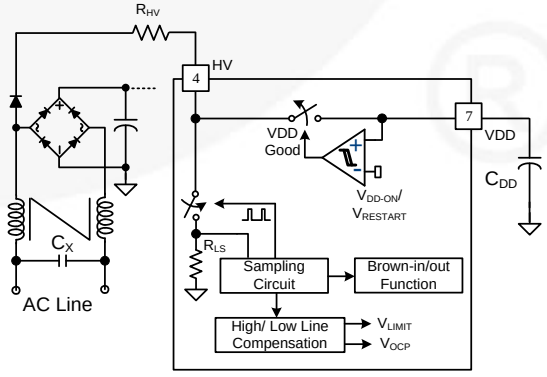


Figure 24. Startup Circuit

The HV pin detects the AC line voltage using a switched voltage divider consisting of an external resistor (R_{HV}) and an internal resistor (R_{LS}), as shown in Figure 24. The internal line-sensing circuit detects line voltage using a sampling circuit and a peak-detection circuit. Since the voltage divider causes power consumption when it is switched on, the switching is driven by a signal with a very narrow pulse width to minimize power loss. The sampling frequency is also adaptively changed according to the load condition to minimize power consumption in light-load condition.

Based on the detected line voltage, brown-in and brownout thresholds are determined as:

$$V_{BROWN\text{-}IN}\ (\text{RMS}) = \frac{R_{HV}}{200\text{k}} \cdot \frac{V_{AC\text{-}ON}}{\sqrt{2}} \quad (2)$$

$$V_{BROWN\text{-}OUT}\ (\text{RMS}) = \frac{R_{HV}}{200\text{k}} \cdot \frac{V_{AC\text{-}OFF}}{\sqrt{2}} \quad (3)$$

Since the internal resistor (R_{LS}=1.62 kΩ) of the voltage divider is much smaller than R_{HV}, the thresholds are given as a function of R_{HV}.

Note that V_{DD} must be larger than $V_{DD\text{-}AC}$ to start up, even though sensed line voltage satisfies Equation 2.

AX-CAP® Discharge

The EMI filter in the front end of the Switched-Mode Power Supply (SMPS) typically includes a capacitor across the AC line connector. Most of the safety regulations, such as UL 1950 and IEC61010-1, require the capacitor be discharged to a safe level within a given time when AC plug is removed from its receptacle. Typically, discharge resistors across the capacitor are used to ensure the capacitor is discharged naturally, which introduces power loss as long as it is connected to the receptacle.

The innovative AX-CAP® technology intelligently discharges the filter capacitor only when the power supply is unplugged from the power outlet. Since the AX-CAP® discharge circuit is disabled in normal operation, the power loss in the EMI filter can be virtually removed.

The discharge of the capacitor is achieved through the HV pin. Once AC outlet detaching is detected, the FAN6757 discharges the capacitor across the AC line connector by the external resistor on the HV pin.

High/Low Line Compensation for Constant Power Limit

FAN6757 has pulse-by-pulse current limit, as shown in Figure 25, to limit the maximum input power with a given input voltage. If the output consumes beyond this maximum power, the output voltage drops triggering the overload protection.

As shown in Figure 25, the high/low line compensation block adjusts the current-limit level, V_{LIMIT}, based on the line voltage. Figure 26 shows how the pulse-by-pulse current-limit level changes with the line voltage for different R_{HV} resistors. To maintain the constant output power limit regardless of line voltage, the cycle-by-cycle current-limit level, V_{LIMIT}, decreases as line voltage increases. The current-limit level is also proportional to the R_{HV} resistor value and the power-limit level can be tuned using the R_{HV} resistor.

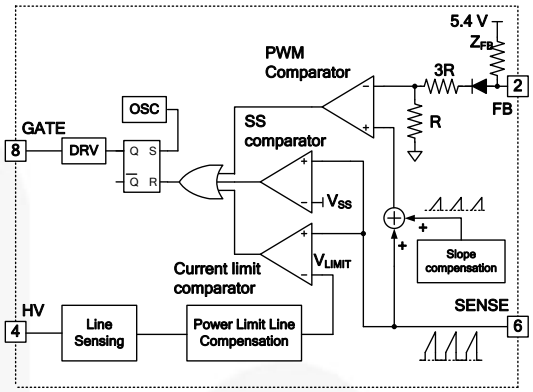


Figure 25. Pulse-by-pulse Current Limit Circuit

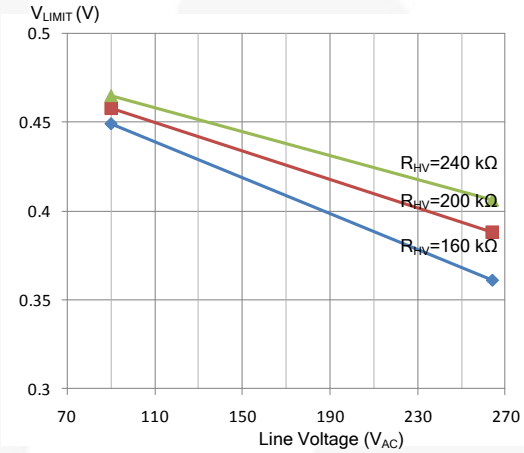


Figure 26. Current Limit vs. Line Voltage

Under-Voltage Lockout (UVLO)

As shown in Figure 27, as long as protection is not triggered, the turn-off threshold of V_{DD} is fixed internally at V_{UVLO} (6.5 V). When Protection Mode is triggered, the V_{DD} level to terminate PWM gate switching is changed to $V_{DD\text{-}OFF}$ (11 V), as shown in Figure 28. When V_{DD} drops below $V_{DD\text{-}OFF}$, switching is terminated and the operating current from VDD is reduced to $I_{DD\text{-}OLP}$ to slow down the discharge of VDD until V_{DD} reaches $V_{DD\text{-}OLP}$. This delays re-startup after shutdown by protection to minimize the input power and voltage/current stress of switching devices during fault condition.

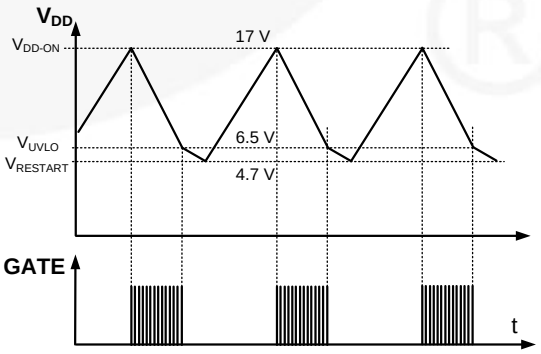


Figure 27. V_{DD} UVLO at Normal Mode

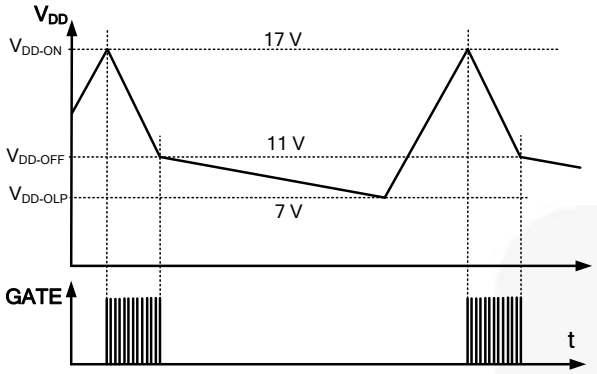


Figure 28. V_{DD} UVLO at Protection Mode

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time, t_{LEB}, is introduced. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Gate Output / Soft Driving

The BiCMOS output stage has a fast totem-pole gate driver. The output driver is clamped by an internal 14.5 V Zener diode to protect power MOSFET gate from over voltage. A soft driving is implemented to minimize electromagnetic interference (EMI) by reducing the switching noise.

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents IC damage from over-voltage exceeding the IC voltage rating. When the V_{DD} voltage exceeds 24.5 V, the protection is triggered. This protection is typically caused by open circuit of the secondary-side feedback network.

Soft-Start

An internal soft-start circuit progressively increases the pulse-by-pulse current-limit level of the MOSFET for 7 ms during startup to establish the correct working conditions for the transformers and capacitors.

Over-Temperature Protection (OTP)

The RT pin provides adjustable Over-Temperature Protection (OTP) and an external latch triggering function. For OTP applications, an NTC thermistor, R_{NTC}, usually in series with a resistor R_A, is connected between the RT pin and ground. The internal current source, I_{RT}, (100 µA) introduces voltage on RT as:

$$V_{RT} = I_{RT} \cdot (R_{NTC} + R_A) \quad (4)$$

At high ambient temperature, R_{NTC} decreases reducing V_{RT}. When V_{RT} is lower than V_{RTTH1} (1.035 V) for longer than t_{D-OTP1} (14.5 ms), the protection is triggered and the FAN6757 enters latch mode protection.

The OTP can be also trigged by pulling down the RT pin voltage using an opto-coupler or transistor. Once V_{RT} is less than V_{RTTH2} (0.7 V) for longer than t_{D-OTP2} (185 µs), the protection is triggered and latch mode protection begins.

When OTP is not used, it is recommended to place a 10 kΩ resistor between this pin and ground to prevent noise interference.

Sense-Pin Short-Circuit Protection

FAN6757 provides safety protection for Limited Power Source (LPS) test. When the current-sense resistor is short circuited by a soldering defect during production, the current-sensing information is not properly obtained, which results in unstable operation of the power supply.

To protect the power supply against a short circuit across the current-sense resistor, the FAN6757 shuts down when the current-sense voltage is very low, even with a relatively large duty cycle. As shown in Figure 29, the current-sense voltage is sampled $t_{ON-SSCP}$ (4.55 µs) after the gate turn-on. If the sampled voltage (V_{S-CS}) is lower than V_{SSCP} for 11 consecutive switching cycles (170 µs), the FAN6757 shuts down immediately. V_{SSCP} varies linearly with the line voltage. At 122 V DC input, it is typically 50 mV (V_{SSCP-L}); while at 366 V DC, it is typically100 mV (V_{SSCP-H}).

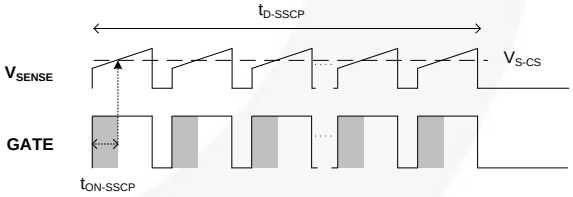


Figure 29. Timing Diagram of SSCP

Typical Application Circuit

Application	PWM Controller	Input Voltage Range	Output
65 W Notebook Adapter	FAN6757MRMX	85 V_{AC} ~ 265 V_{AC}	19 V, 3.42 A

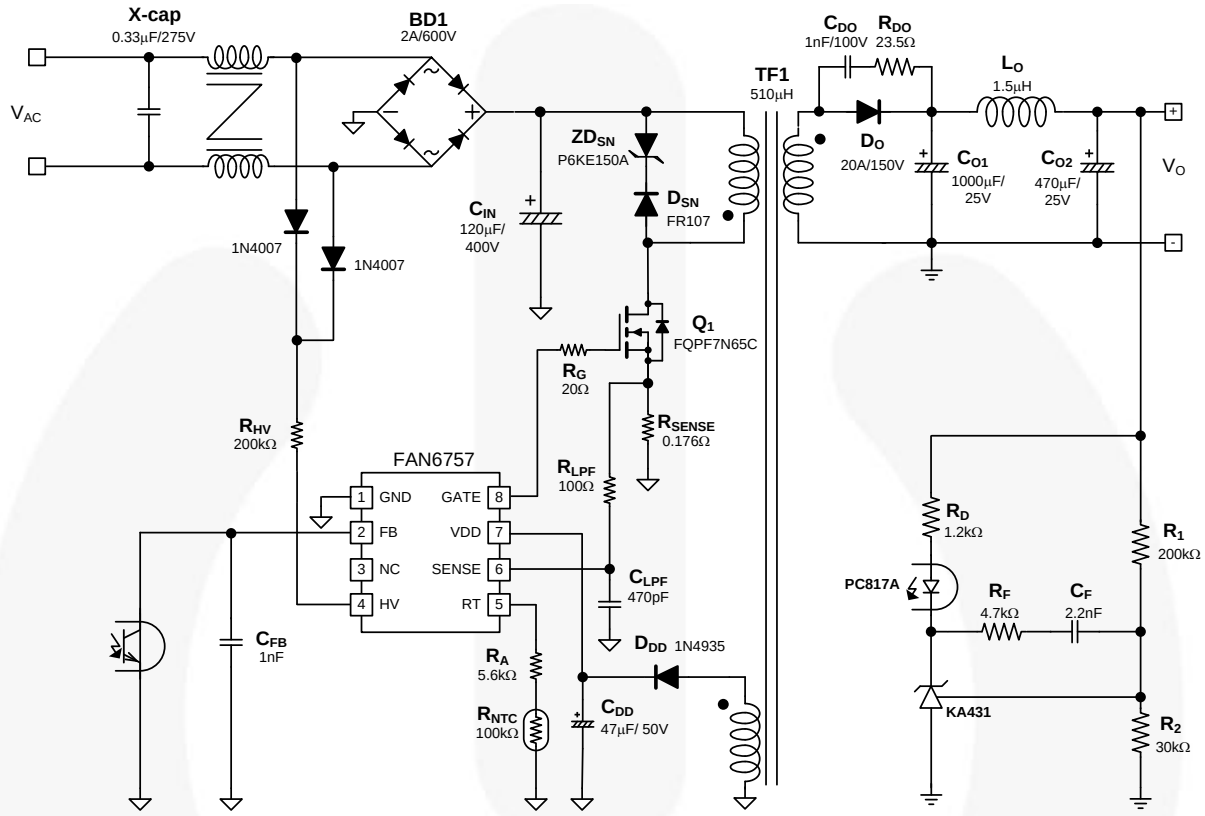


Figure 30. Schematic of Typical Application Circuit

Transformer Schematic Diagram

- Core: Ferrite Core RM-10
- Bobbin: RM-10

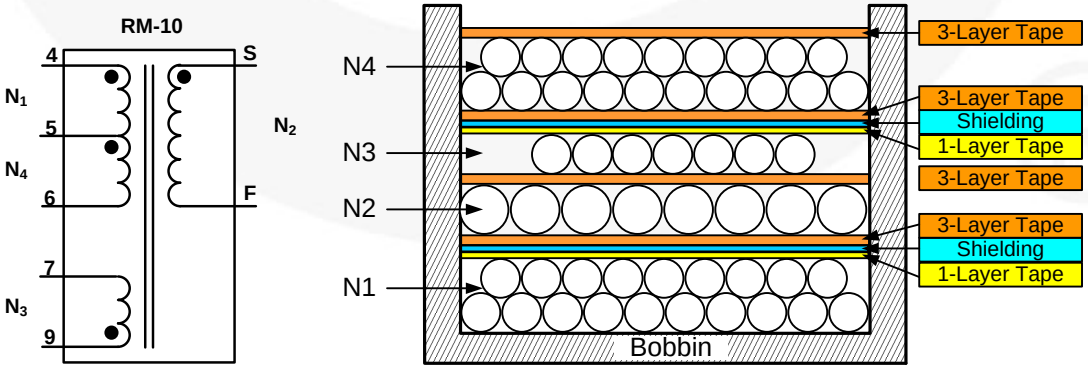


Figure 31. Transformer Specification

Winding Specification

	Pin (Start → Finish)	Wire	Turns	Winding Method	Remark
N1	4 → 5	0.5φ×1	19	Solenoid Winding	Enameled Copper Wire
Insulation: Polyester Tape, t = 0.025 mm, 1 Layer					
Shielding: Adhesive Tape of Copper Foil, t = 0.025×7 mm, 1.2 Layers, Open Loop, Connected to Pin 4					
Insulation: Polyester Tape t = 0.025 mm, 3 Layers					
N2	S → F	0.9φ×1	8	Solenoid Winding	Triple Insulated Wire
Insulation: Polyester Tape, t = 0.025mm, 3 Layers					
N3	9 → 7	0.4φ×1	7	Solenoid Winding	Enameled Copper Wire
Insulation: Polyester Tape, t = 0.025 mm, 1 Layer					
Shielding: Adhesive Tape of Copper Foil, t = 0.025×7 mm, 1.2 Layers, Open Loop, Connected to Pin 4					
Insulation: Polyester Tape t = 0.025 mm, 3 Layers					
N4	5 → 6	0.5φ×1	19	Solenoid Winding	Enameled Copper Wire
Insulation: Polyester Tape t = 0.025 mm, 3 Layers					

Electrical Characteristics

	Pin	Specification	Remark
Primary-Side Inductance	4 − 6	510 μH ±5%	1 kHz, 1 V
Primary-Side Effective Leakage Inductance	4 − 6	20 μH Maximum	Short All Other Pins

Typical Performance

Table 1. Power Consumption

Input Voltage	Output Power	Actual Output Power	Input Power	Specification
230 V_{AC}	No Load	0 W	0.045 W	Input Power < 0.05 W
	0.25 W	0.255 W	0.360 W	Input Power < 0.5 W
	0.5 W	0.521 W	0.711 W	Input Power < 1 W

Table 2. Efficiency

Output Power	16.25 W	32.5 W	48.75 W	65 W	Average
115 V 60 Hz	87.84%	87.42%	86.92%	86.23%	87.10%
230 V 50 Hz	87.88%	87.95%	87.82%	87.69%	87.83%

Physical Dimensions

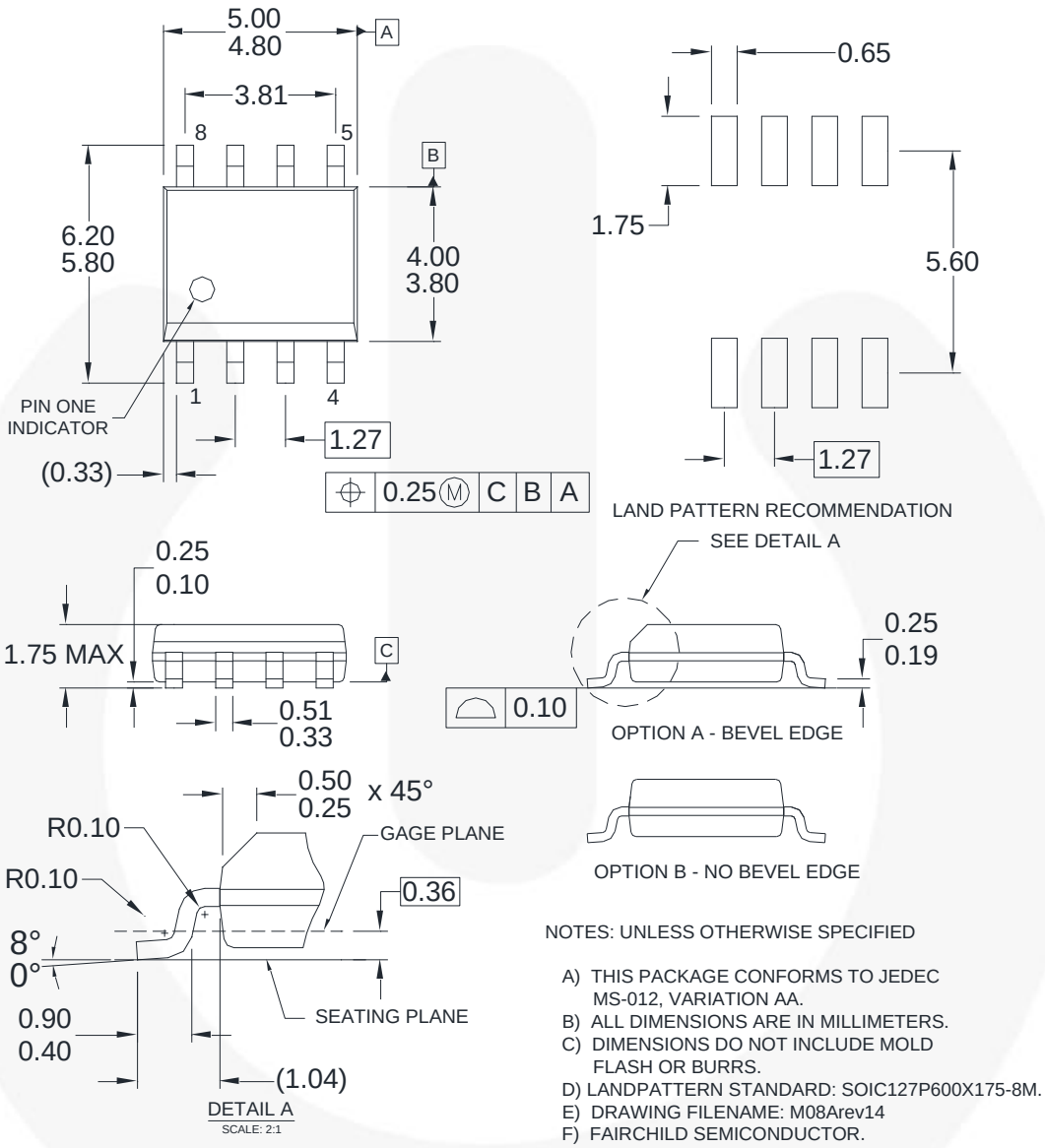


Figure 32. 8-Pin, SOP-8 Package

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