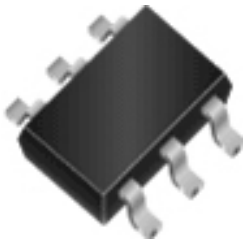
ESD5485E

4-Lines, Uni-directional, Low Capacitance Transient Voltage Suppressors

http//:www.sh-willsemi.com



SOT-23-6L

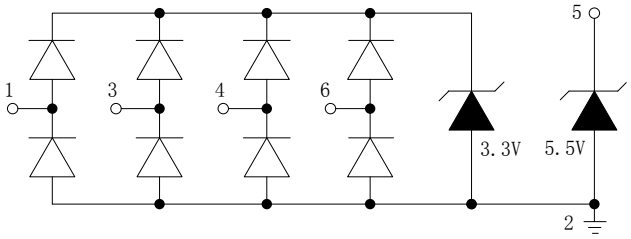
Descriptions

The ESD5485E is a low capacitance TVS (Transient Voltage Suppressor) array designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD (Electrostatic Discharge).

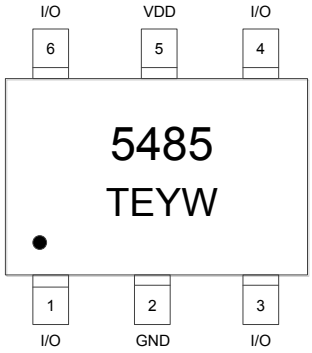
The ESD5485E incorporates four pairs of low capacitance steering diodes plus a TVS diode.

The ESD5485E may be used to provide ESD protection up to ±30kV (contact discharge) according to IEC61000-4-2, and withstand peak pulse current up to 40A (5/50ns) according to IEC61000-4-4, 10A (8/20μs) according to IEC61000-4-5.

The ESD5485E is available in SOT-23-6L package. Standard products are Pb-free and Halogen-free.



Circuit diagram



5485 = Device code
TE =Special code
YW = Date code

Marking & Pin configuration (Top View)

Features

- Reverse stand-off voltage: 3.3V max(Any I/O pin)
- 5.5V max(VDD pin)
- Transient protection for each line according to
  IEC61000-4-2 (ESD): ±30kV (contact discharge)
  IEC61000-4-4 (EFT): 40A (5/50ns)
  IEC61000-4-5 (surge): 10A (8/20μs)
- Low capacitance: $C_{I/O - GND}$ = 1.45pF typ.
- Low leakage current: I_R <10nA typ.
- Low clamping voltage: $V_{CL, I/O - GND}$ = 5.3V @ I_{PP} = 16A (TLP)
- Solid-state silicon technology

Applications

- USB 2.0
- Video Graphics Cards
- DVI
- Notebooks

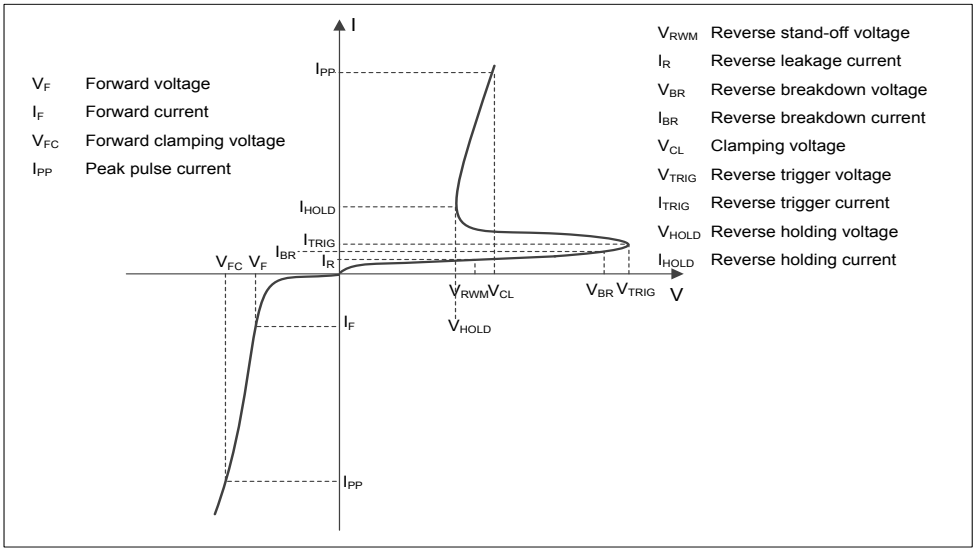
Order information

Device	Package	Shipping
ESD5485E-6/TR	SOT-23-6L	3000/Tape&Reel

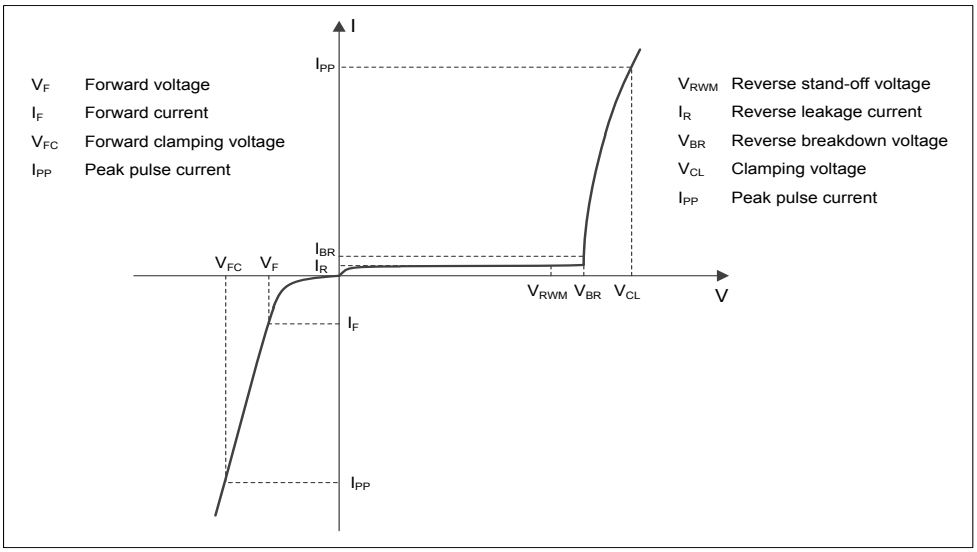
Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Peak pulse current (t_p = 8/20μs)	I_{PP}	10	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±30	kV
ESD according to IEC61000-4-2 contact discharge		±30	kV
Junction temperature	T_J	125	°C
Operation temperature	T_{OP}	-40 to 85	°C
Storage temperature	T_{STG}	-55 to 150	°C
Lead temperature	T_L	260	°C

Electrical characteristics (T_A = 25°C, unless otherwise noted)



Definitions of electrical characteristics (Any I/O Pin)



Definitions of electrical characteristics (VDD Pin)

Electrical characteristics (T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Any I/O Pin						
Reverse stand-off voltage	V_{RWM}				3.3	V
Reverse leakage current	I_R	V_{RWM} = 3.3V		<10	100	nA
Reverse breakdown voltage	V_{BR}	I_{BR} = 1mA	8.0	9.0	10.0	V
Forward voltage	V_F	I_F = 20mA	0.6	0.9	1.1	V
Clamping voltage [1]	V_{CL}	I_{PP} = 16A, t_p = 100ns(I/O - GND)		5.3		V
		I_{PP} = 16A, t_p = 100ns(GND – I/O)		2.9		V
Dynamic resistance [1]	R_{DYN}	t_p = 100ns		0.15		Ω
Clamping voltage [2]	V_{CL}	V_{ESD} = 8kV		5.5		V
Clamping voltage [3]	V_{CL}	I_{PP} = 1A, t_p = 8/20μs			3.5	V
		I_{PP} = 10A, t_p = 8/20μs			6	V
Junction capacitance	$C_{I/O - GND}$	V_R = 1.65V, f = 1MHz, VDD = floated, any I/O to GND		1.45	1.8	pF
	$C_{I/O - I/O}$	V_R = 1.65V, f = 1MHz, any I/O to I/O		0.65	0.90	pF
VDD Pin						
Reverse stand-off voltage	V_{RWM}				5.5	V
Reverse leakage current	I_R	V_{RWM} = 5.5V		<10	100	nA
Reverse breakdown voltage	V_{BR}	I_{BR} = 1mA	8.0	9.0	10.0	V
Forward voltage	V_F	I_F = 20mA	0.6	0.9	1.1	V
Clamping voltage [3]	V_{CL}	I_{PP} = 1A, t_p = 8/20μs			11	V
		I_{PP} = 10A, t_p = 8/20μs			15	V

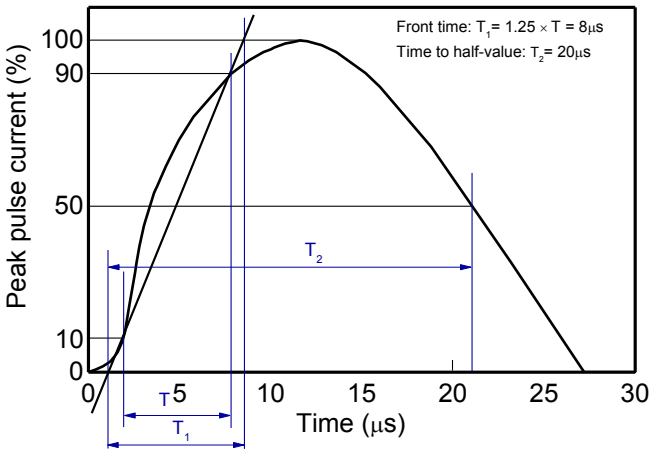
Notes:

1) *TLP parameter: Z_0 = 50Ω, t_p = 100ns, t_r = 2ns, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.*

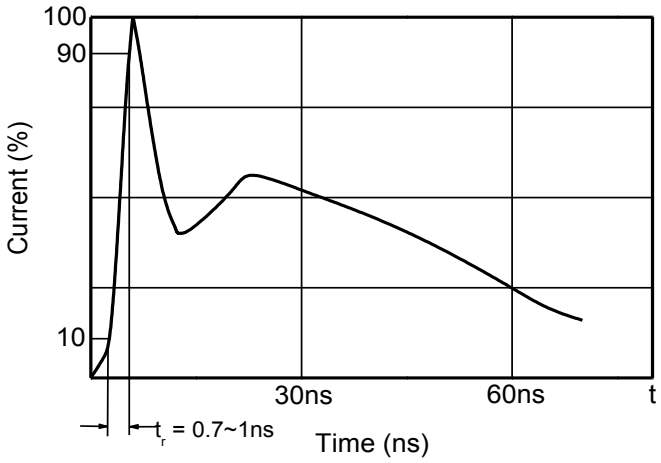
2) *Contact discharge mode, according to IEC61000-4-2.*

3) *Non-repetitive current pulse, according to IEC61000-4-5.*

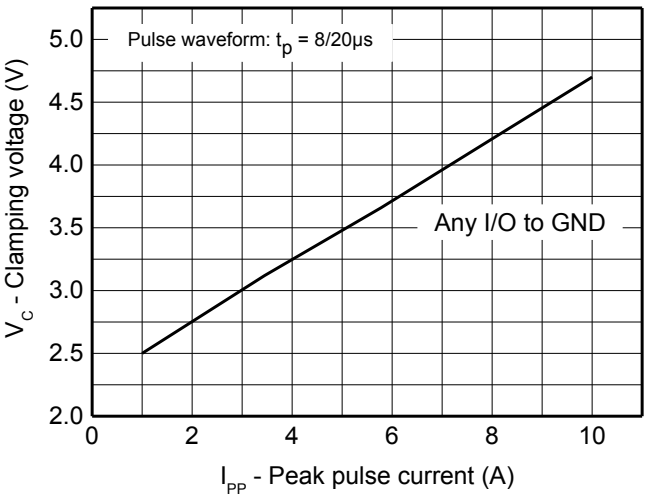
Typical characteristics (T_A = 25°C, unless otherwise noted)



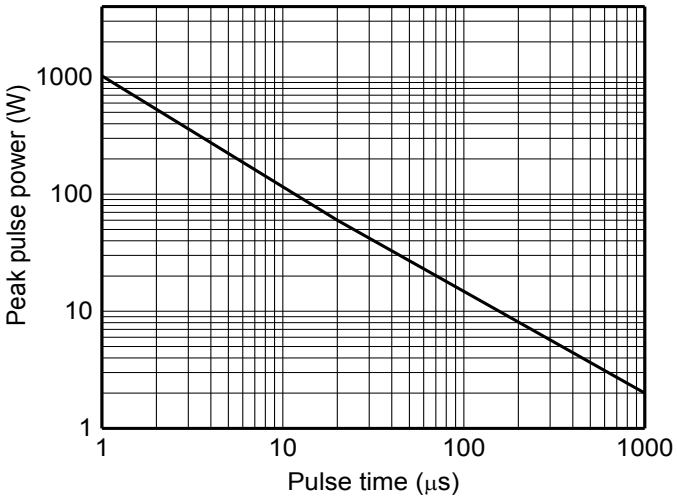
8/20μs waveform per IEC61000-4-5



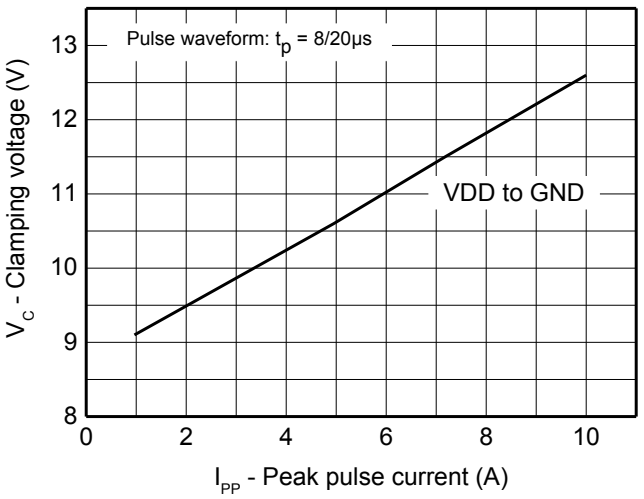
Contact discharge current waveform per IEC61000-4-2



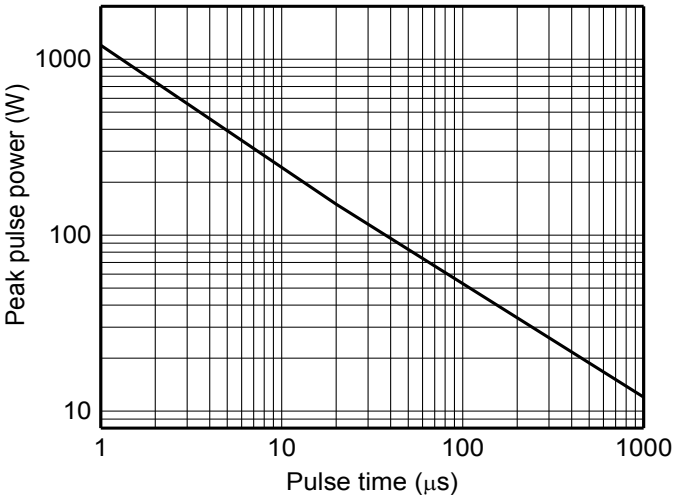
Clamping voltage vs. Peak pulse current (Any I/O Pin)



Non-repetitive peak pulse power vs. Pulse time (Any I/O Pin)

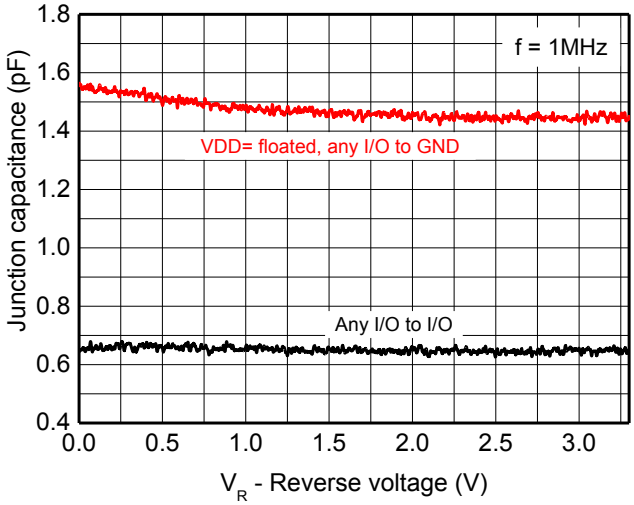


Clamping voltage vs. Peak pulse current (VDD Pin)

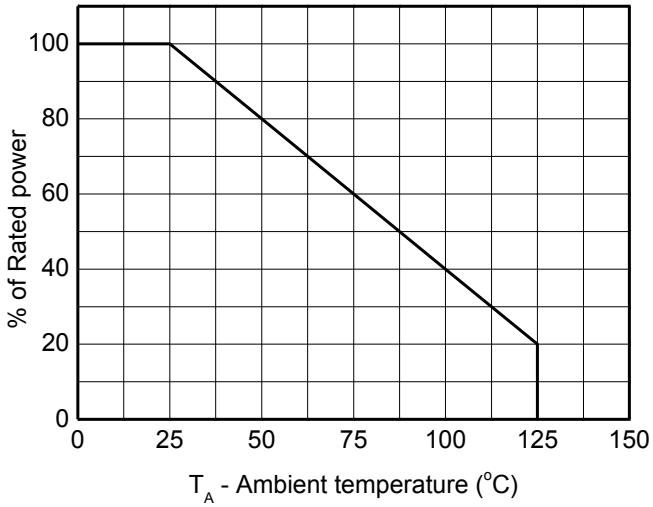


Non-repetitive peak pulse power vs. Pulse time (VDD Pin)

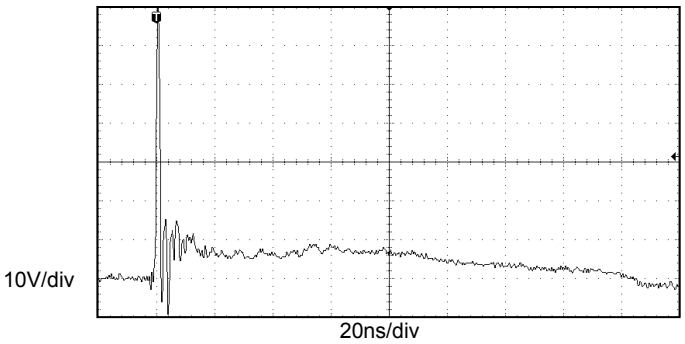
Typical characteristics (T_A = 25°C, unless otherwise noted)



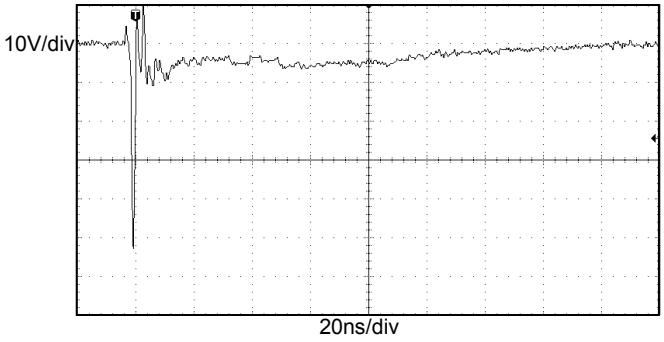
Capacitance vs. Reverse voltage
(Any IO Pin)



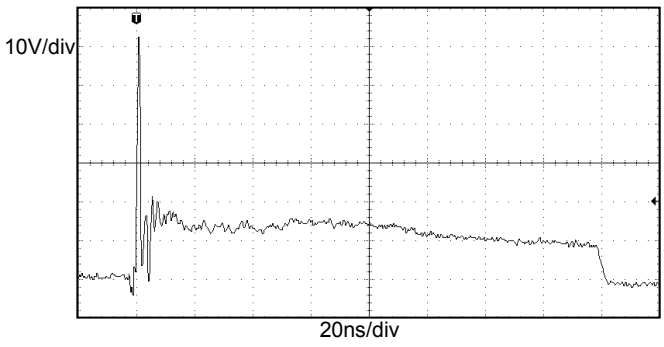
Power derating vs. Ambient temperature



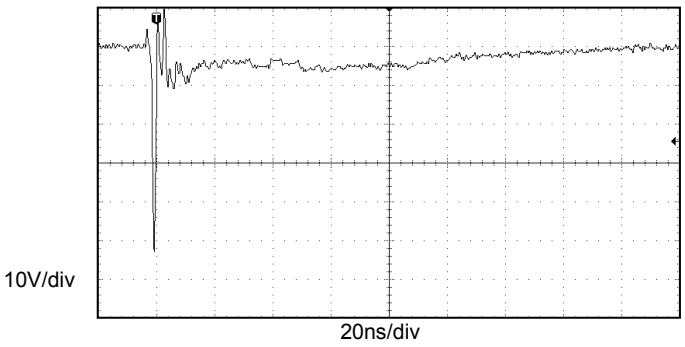
ESD clamping
(+8kV contact discharge per IEC61000-4-2)
(Any I/O Pin)



ESD clamping
(-8kV contact discharge per IEC61000-4-2)
(Any I/O Pin)

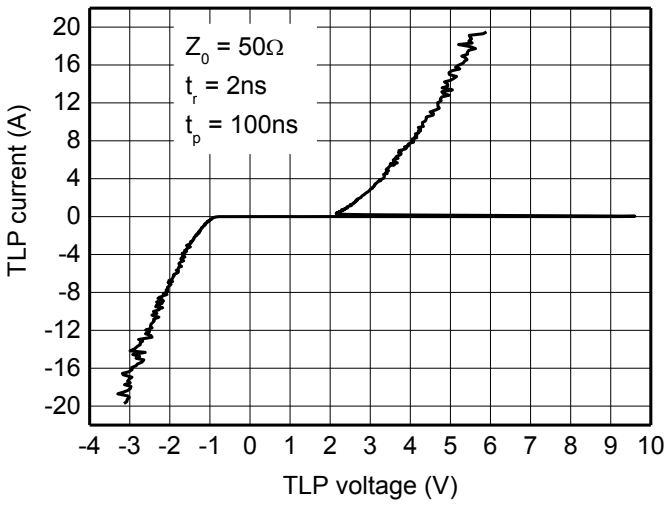


(+8kV contact discharge per IEC61000-4-2)
(VDD Pin)

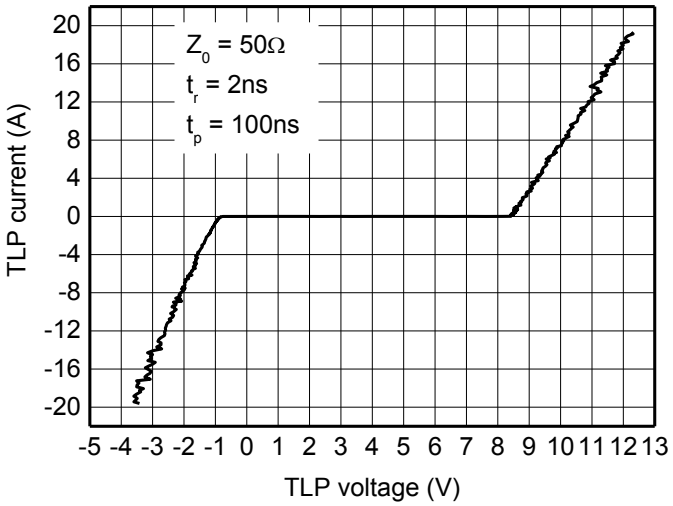


(-8kV contact discharge per IEC61000-4-2)
(VDD Pin)

Typical characteristics (T_A = 25°C, unless otherwise noted)



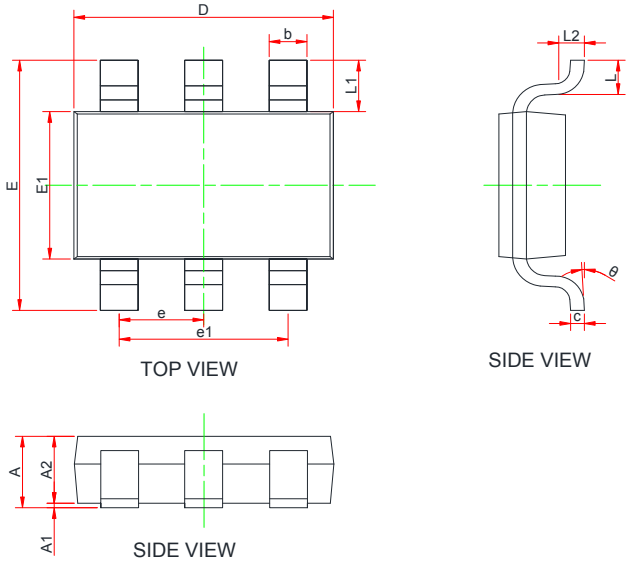
TLP Measurement
(Any I/O Pin)



TLP Measurement
(VDD Pin)

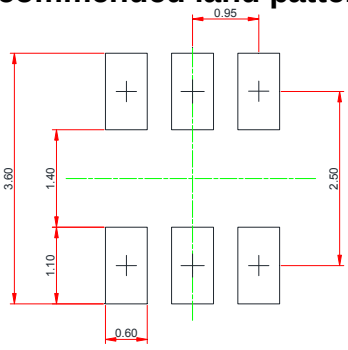
PACKAGE OUTLINE DIMENSIONS

SOT-23-6L



Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	1.05	-	1.45
A1	0	-	0.15
A2	0.90	1.10	1.30
b	0.30	0.40	0.50
c	0.10	-	0.21
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.85	0.95	1.05
e1	1.80	1.90	2.00
L	0.30	-	0.60
L1	0.59Ref		
L2	0.25Ref		
θ	0 °	-	8 °

Recommended land pattern (Unit: mm)

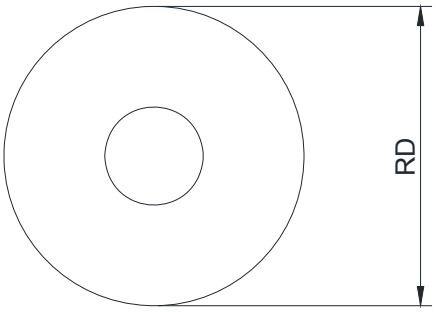


Notes:

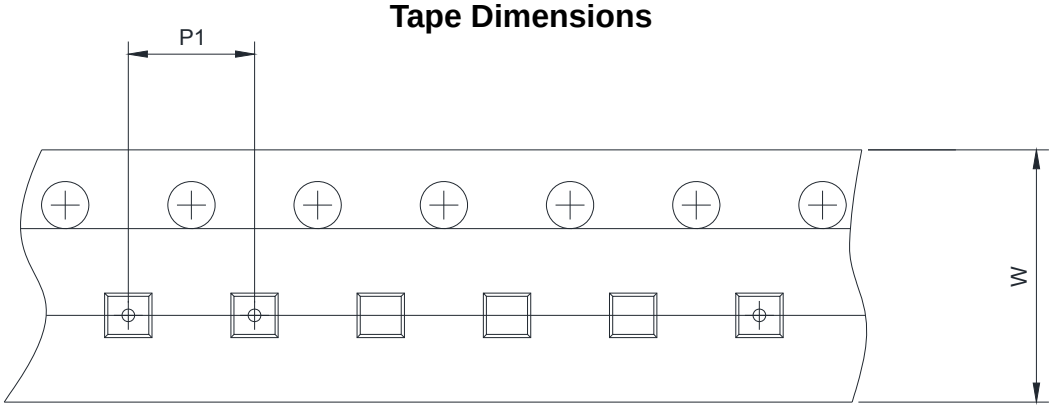
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

TAPE AND REEL INFORMATION

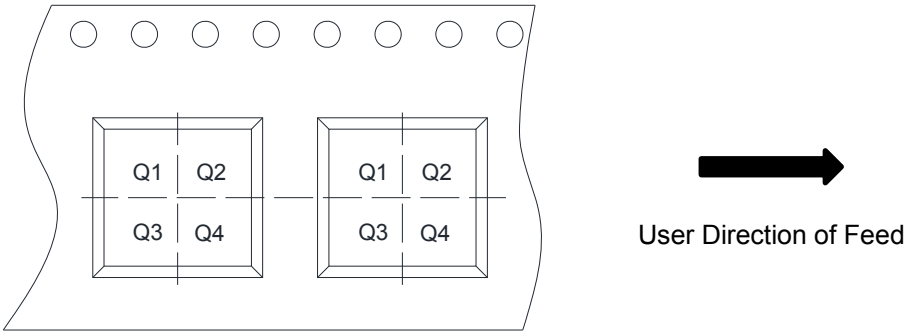
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑7inch	☐13inch		
W	Overall width of the carrier tape	☑8mm	☐12mm	☐16mm	
P	Pitch between successive cavity centers	☐2mm	☑4mm	☐8mm	
Pin1	Pin1 Quadrant	☐Q1	☐Q2	☑Q3	☐Q4