MAXIM

I²C, 8-Channel Gamma Buffer with EEPROM

General Description

The DS3508 is a programmable 8-channel gamma voltage generator with one byte of on-chip EEPROM and one byte of SRAM memory per channel. Each channel is composed of an independent 8-bit DAC with an associated EEPROM/SRAM pair. At power-up, nonvolatile (NV) EEPROM gamma data is loaded into its corresponding SRAM register that drives the associated 8-bit DAC. An on-chip control register allows selectable control of writing to SRAM/EEPROM or SRAM only.

The DS3508 is designed for low-power operation and draws less than 2mA (typ) from the V_{DD} supply. Programming occurs through an I²C-compatible serial interface with support for speeds up to 400kHz.

Features

- **8-Bit Gamma DACs, 8 Channels**
- **1 Byte EEPROM and 1 Byte SRAM per Channel**
- **Ultra-Low Power (2mA I_{DD}, typ)**
- **400kbps I²C Interface**
- **9.0V to 15.5V Analog Supply**
- **2.7V to 5.5V Digital Supply**
- **20-Pin TSSOP Package**
- **Address Pin Allows Two DS3508s to Reside on the Same I²C Bus**

Applications

TFT-LCD Gamma Buffer

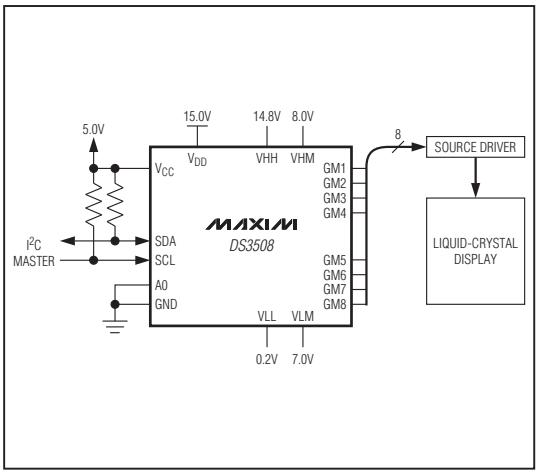
Industrial Controls

Ordering Information

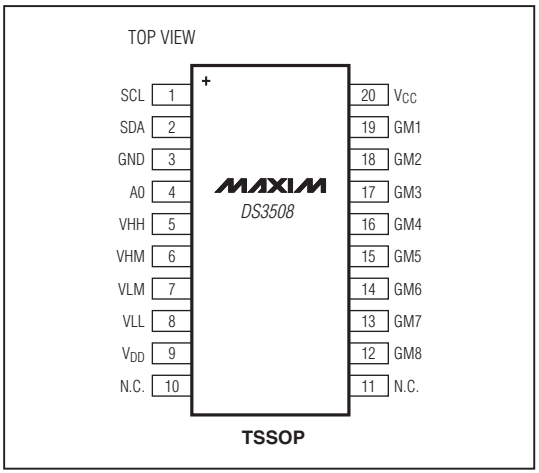
PART	TEMP RANGE	PIN-PACKAGE
DS3508E+	-45°C to +95°C	20 TSSOP
DS3508E+T&R	-45°C to +95°C	20 TSSOP

+Denotes a lead-free package.
T&R = Tape and reel.

Typical Operating Circuit



Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{DD} and VHH Relative to GND .....-0.5V to +16V
Voltage Range on VHM, VLM, and VLL Relative to GND.....-0.5V to +12V
Voltage Range on V_{CC}, SDA, SCL, and A0 Relative to GND .....-0.5V to +6.0V

Junction Temperature .....+125°C
Operating Temperature Range .....-45°C to +95°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature .....55°C to +125°C
Soldering Temperature .....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -45°C to +95°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Voltage	V_{DD}	(Note 1)	+9.0		+15.5	V
VHH, VHM		Applies to GM1–GM4	V_{DD}/2 - 1		V_{DD} - 0.2	V
VLM, VLL		Applies to GM5–GM8	0.2		V_{DD}/2 + 1	V
VHH–VHM and VLM–VLL	$V_{REF}\Delta$		3.0			V
Digital Voltage Supply	V_{CC}	(Note 1)	2.7		5.5	V
Input Logic 0 (A0, SDA, SCL)	V_{IL}				0.3 x V_{CC}	V
Input Logic 1 (A0, SDA, SCL)	V_{IH}		0.7 x V_{CC}			V

INPUT ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -45°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Current	I_{DD}	V_{DD} = 15.5V (Note 2)		2	4	mA
Digital Supply Current, NV Read or Write	I_{CC}	f_{SCL} = 400kHz		0.2	1.0	mA
Digital Supply Standby Current	I_{STBY}	V_{CC} = 5.5V (Note 3)		2	10	µA
Input Leakage (SDA, SCL, A0)	I_{IL}	V_{CC} = 5.5V	-1		+1	µA
Input Resistance at VHH, VHM, VLM, VLL	R_{IN}		1			MΩ

OUTPUT ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V; V_{DD} = 15.5V, T_A = -45°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gamma DAC Resolution			8			Bits
Integral Nonlinearity Error		T_A = +25°C (Note 4)	-1.25		+1.25	LSB
Differential Nonlinearity Error		T_A = +25°C (Note 5)	-0.5		+0.5	LSB
Output Voltage Range: GM1–GM4			VHM		VHH	V
Output Voltage Range: GM5–GM8			VLL		VLM	V
R_{OUT} (GM1–GM8)	R_{OUT}	(Notes 6, 7)		20		kΩ
Amplifier Offset		T_A = +25°C (Note 8)	-35		+35	mV

I²C ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -45°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (Figure 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 9)	0		400	kHz
Low Period of SCL	t_{LOW}	Measured at V_{IL}	1.3			µs
High Period of SCL	t_{HIGH}	Measured at V_{IH}	0.6			µs
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Setup Time	$t_{SU:STA}$	SCL rising through V_{IH} to SDA falling through V_{IH}	0.6			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	SDA falling through V_{IL} to SCL falling through V_{IH}	0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
A0 Setup Time	$t_{SU:A}$	Before START	0.6			µs
A0 Hold Time	$t_{HD:A}$	After STOP	0.6			µs
SDA and SCL Rise Time	t_R	(Note 10)	20 + (0.1 x C_B)		300	ns
SDA and SCL Fall Time	t_F	(Note 10)	20 + (0.1 x C_B)		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 10)			400	pF
EEPROM Write Time	t_W	(Note 11)			20	ms
SCL Falling Edge to SDA Output Data Valid	t_{AA}	SCL falling through V_{IL} to SDA exit 0.3–0.7 x V_{CC} window			900	ns
Output Data Hold	t_{DH}	SCL falling through V_{IL} until SDA in 0.3–0.7 x V_{CC} window	0			ns

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I²C ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -45°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (Figure 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA Output Low Voltage	V_{OL}	4mA sink current			0.4	V
		6mA sink current			0.6	
Input Capacitance on A0, SDA, or SCL	C_I			5	10	pF

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V)

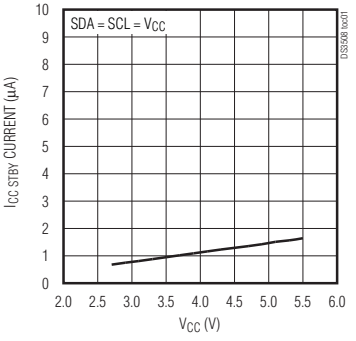
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		T_A = +70°C	50,000			Writes

Note 1: All voltages referenced to ground.
Note 2: Analog supply current specified with no load on GMx outputs.
Note 3: ISTBY specified for the inactive state measured with SDA = SCL = V_{CC}.
Note 4: INL = $[V(GMx)_i - (V(GMx)_0]$/LSB(ideal) - i, for i = 0 to 254.
Note 5: DNL = $[V(GMx)_{i+1} - (V(GMx)_i]$/LSB(ideal) - 1, for i = 0 to 255.
Note 6: DAC code = 80h.
Note 7: Outputs unloaded.
Note 8: VHH = 12.0V, VHM = 8.75V, VLM = 6.75V, VLL = 0.5V.
Note 9: Timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard mode.
Note 10: C_B—Total capacitance of one bus line in picofarads.
Note 11: EEPROM write begins after a STOP condition occurs.

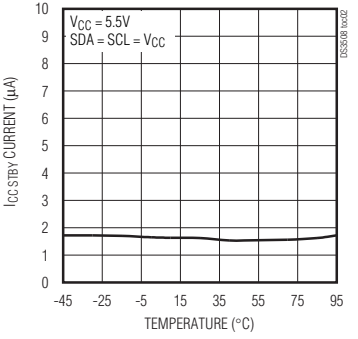
Typical Operating Characteristics

(V_{DD} = 15.0V, V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

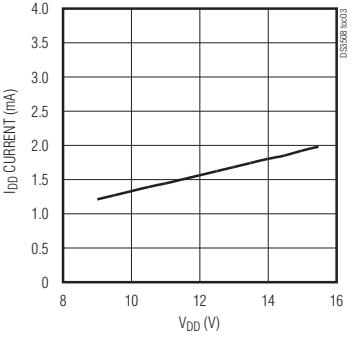
DIGITAL SUPPLY STANDBY CURRENT vs. DIGITAL SUPPLY VOLTAGE



DIGITAL SUPPLY STANDBY CURRENT vs. TEMPERATURE



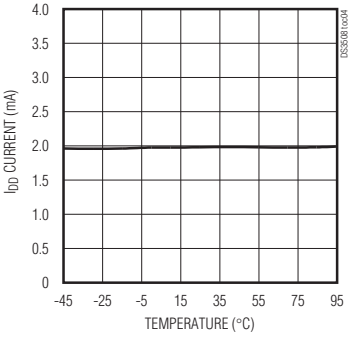
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



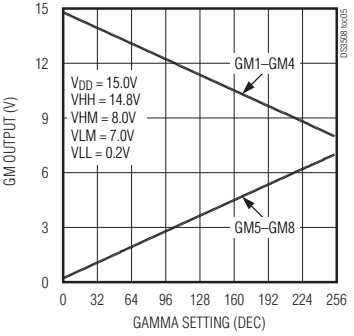
Typical Operating Characteristics (continued)

(V_{DD} = 15.0V, V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

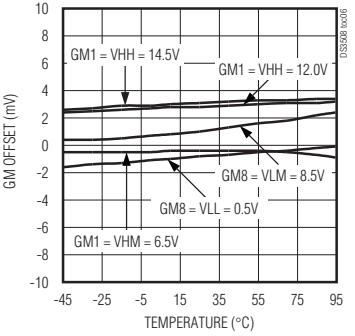
ANALOG SUPPLY CURRENT vs. TEMPERATURE



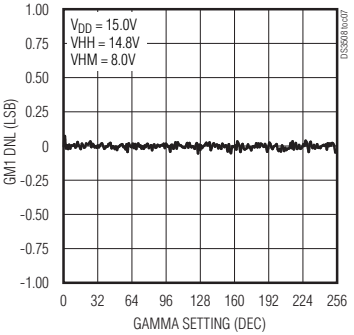
GAMMA OUTPUT vs. SETTING



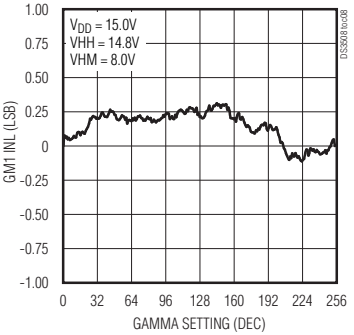
GAMMA OFFSET vs. TEMPERATURE



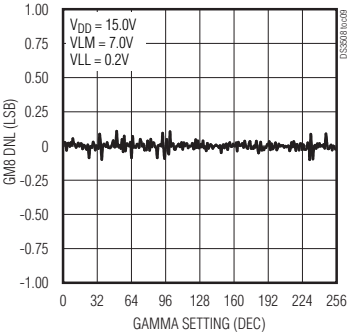
GM1 DNL



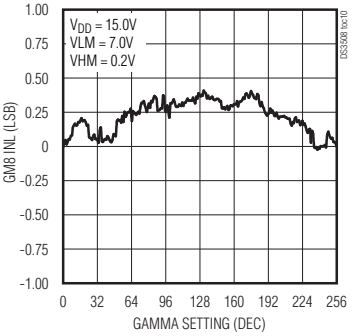
GM1 INL



GM8 DNL

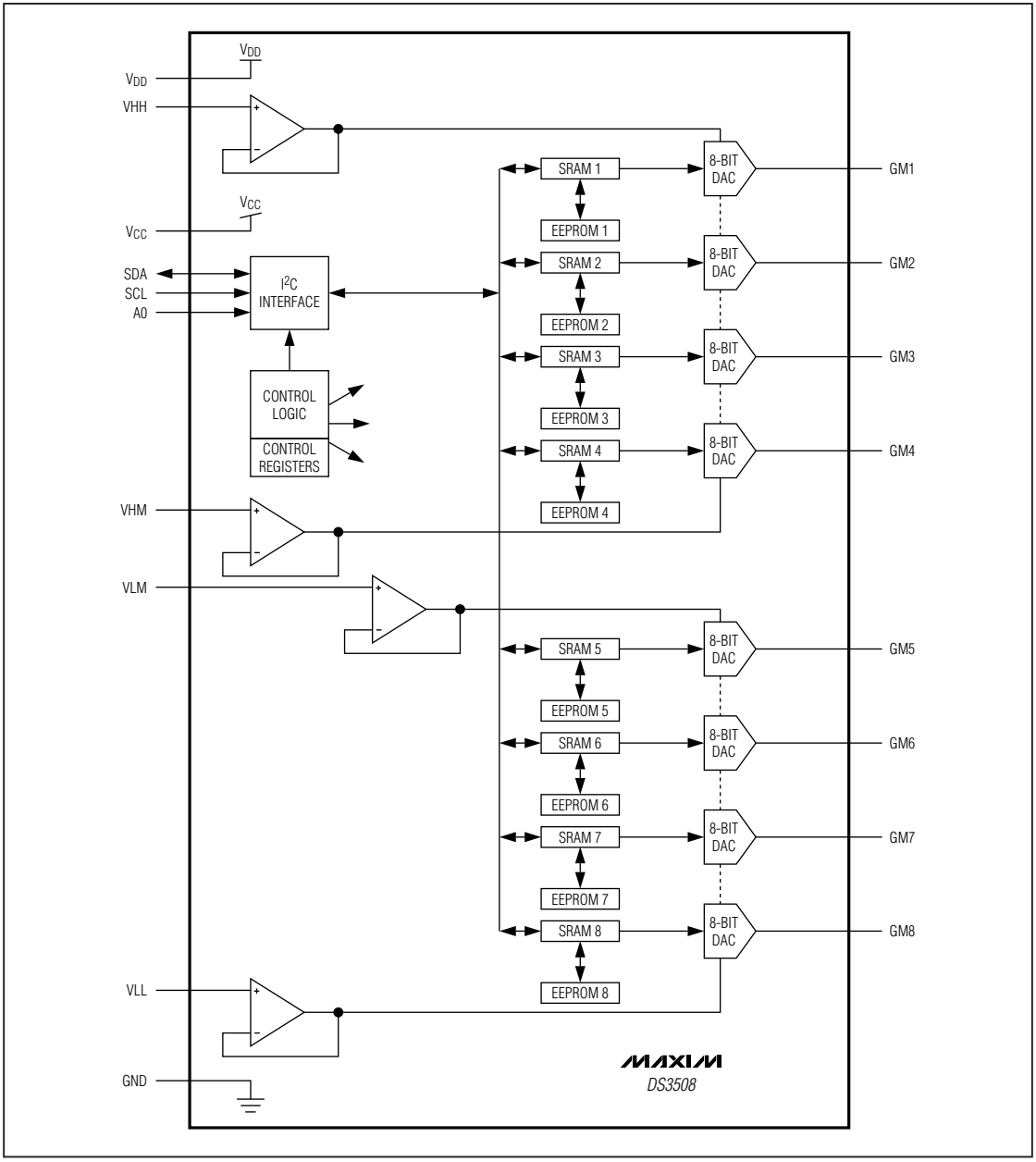


GM8 INL



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Functional Diagram



Pin Description

PIN	NAME	TYPE	FUNCTION
1	SCL	Input	Serial Clock Input. I²C clock input.
2	SDA	Input/ Output	Serial Data Input/Output (Open Drain). I²C bidirectional data pin that requires a pullup resistor to realize high logic levels.
3	GND	Ground	Ground
4	A0	Input	Address Input. Determines I²C slave address.
5	VHH	Reference Input	High-Voltage DAC, Upper Reference
6	VHM	Reference Input	High-Voltage DAC, Lower Reference
7	VLM	Reference Input	Low-Voltage DAC, Upper Reference
8	VLL	Reference Input	Low-Voltage DAC, Lower Reference
9	V_{DD}	Power	Analog Supply
10, 11	N.C.	—	No Connection
12	GM8	Output	Gamma Analog Outputs 5–8. These pins are the low-voltage gamma outputs referenced to VLL and VLM.
13	GM7		
14	GM6		
15	GM5		
16	GM4	Output	Gamma Analog Outputs 1–4. These pins are the high-voltage gamma outputs referenced to VHH and VHM.
17	GM3		
18	GM2		
19	GM1		
20	V_{CC}	Power	Digital Supply

Detailed Description

The DS3508 provides eight independent DACs that allow precise and repeatable setting of gamma curves. The DS3508 provides four high-voltage DACs (GM1–GM4) that operate between VHH and VHM and four low-voltage DACs (GM5–GM8) that operate between VLM and VLL. Each of the DACs provides 8 bits of resolution.

The DS3508 DAC output voltages are independently controlled by the data stored in that channel's SRAM register. The MODE bit in the volatile control register (CR bit 7) determines how I²C data is written to the SRAM and EEPROM gamma data registers. Reading and writing to the SRAM/EEPROM gamma data registers is based on the state of the MODE bit as follows:

MODE = 0: I²C writes to memory addresses 00h–07h write to both SRAM 1–8 and EEPROM 1–8.

I²C reads from addresses 00h–07h read from SRAM 1–8.

MODE = 1: I²C writes to addresses 00h–07h write to SRAM 1–8.

I²C reads from addresses 00h–07h read from SRAM 1–8.

Regardless of the MODE bit setting, all I²C reads of address 00–07h return the contents of the SRAM registers. Setting MODE = 1 allows for quick writing of SRAM without the added delay of writing to the associated EEPROM register. The data that is stored in EEPROM and SRAM remains unchanged if the MODE bit is toggled.

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On power-up, the gamma data that is stored in each channel's EEPROM register is loaded into the corresponding SRAM registers. The volatile CR register powers up as 00h, setting the device into mode 0.

DAC Description

The DACs are composed of a resistor string array and a switching network per channel. A high-voltage array with end points VHH and VHM controls outputs GM1–GM4, and a low-voltage array with end points VLM and VLL controls outputs GM5–GM8. The resistor string arrays are composed of 255 identical resistors. The switching networks can select any tap point between adjacent resistors as well as either end point (VHH/VHM or VLM/VLL pins). Table 1 shows the relationship between the 8-bit data and the DAC voltage.

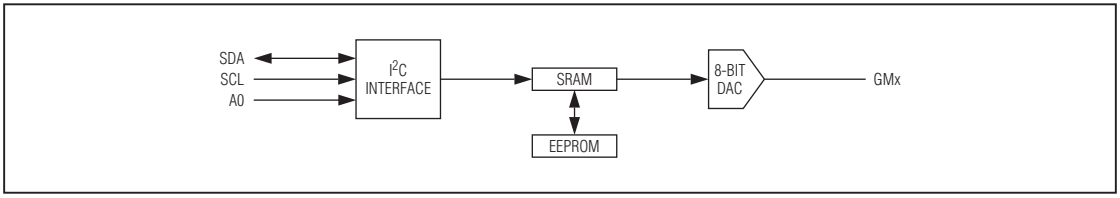


Figure 1. Single-Channel Block Diagram

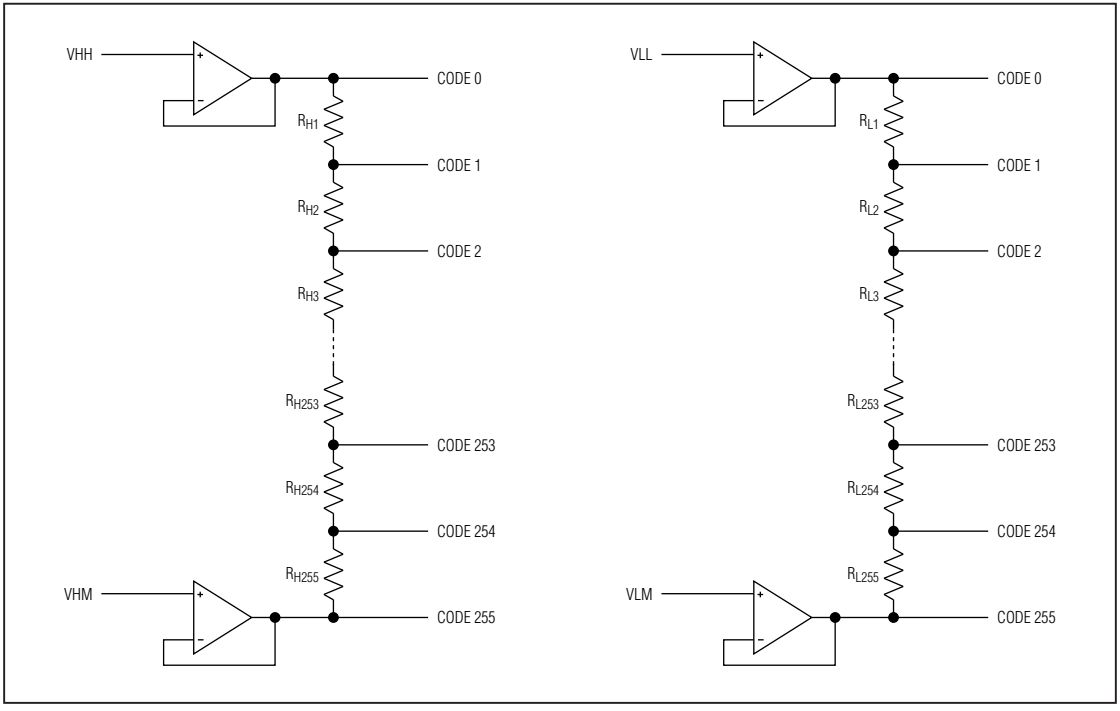


Figure 2. DAC Block Diagram

Table 1. DAC Voltage/Data Relationship for Selected Codes

DATA (BINARY)	OUTPUT VOLTAGE	
	GM1–GM4	GM5–GM8
0000 0000	VHH	VLL
0000 0001	VHH + 1 x (VHM - VHH)/255	VLL+ 1 x (VLM - VLL)/255
0000 0010	VHH + 2 x (VHM - VHH)/255	VLL + 2 x (VLM - VLL)/255
0000 0011	VHH + 3 x (VHM - VHH)/255	VLL + 3 x (VLM - VLL)/255
0000 1111	VHH + 15 x (VHM - VHH)/255	VLL + 15 x (VLM - VLL)/255
0011 1111	VHH + 63 x (VHM - VHH)/255	VLL + 63 x (VLM - VLL)/255
0111 1111	VHH + 127 x (VHM - VHH)/255	VLL + 127 x (VLM - VLL)/255
1111 1101	VHH + 253 x (VHM - VHH)/255	VLL + 253 x (VLM - VLL)/255
1111 1110	VHH + 254 x (VHM - VHH)/255	VLL + 254 x (VLM - VLL)/255
1111 1111	VHM	VLM



Figure 3. DS3508 Slave Address Byte

Slave Address Byte and Address Pin

The slave address byte consists of a 7-bit slave address plus a R/$\overline{W}$ bit (see Figure 3). The DS3508's slave address is determined by the state of the A0 pin. This pin allows up to two devices to reside on the same I²C bus. Connecting A0 to GND results in a 0 in the corresponding bit position in the slave address. Conversely, connecting A0 to V_{CC} results in a 1 in the corresponding bit position. For example, the DS3508's slave address byte is E8h when A0 is grounded. I²C communication is described in detail in the *I²C Serial Interface Description* section.

I²C, 8-Channel Gamma Buffer with EEPROM

Memory Organization

Memory Description

The list of registers/memory contained in the DS3508 is shown in the memory map (Table 2). Each of the GMx registers also has a corresponding NV EEPROM register. Additional information regarding reading and writing the memory is located in the *I²C Serial Interface Description* section.

Table 2. Memory Map

NAME	ADDRESS (HEX)	SRAM	EEPROM
GM1	00	SRAM1 (8 bits)	EEPROM1 (8 bits)
GM2	01	SRAM2 (8 bits)	EEPROM2 (8 bits)
GM3	02	SRAM3 (8 bits)	EEPROM3 (8 bits)
GM4	03	SRAM4 (8 bits)	EEPROM4 (8 bits)
GM5	04	SRAM5 (8 bits)	EEPROM5 (8 bits)
GM6	05	SRAM6 (8 bits)	EEPROM6 (8 bits)
GM7	06	SRAM7 (8 bits)	EEPROM7 (8 bits)
GM8	07	SRAM8 (8 bits)	EEPROM8 (8 bits)
Control Register	08	Volatile Control Register	N/A
Reserved	09–FF	Reserved	Reserved

**All EEPROM1–8 is factory-programmed to 80h.*

Detailed Register Description

Register 08h: Control Register (CR)

POWER-UP DEFAULT 00h
MEMORY TYPE Volatile

08h	MODE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Bit 7							Bit 0

Bit 7	MODE 0 = (Default) I²C writes to both SRAM and EEPROM. MODE 1 = I²C writes to SRAM only.
Bits 6 to 0	Reserved.

This bit determines if data is written to EEPROM and SRAM or only SRAM.

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. (See Figure 4 and the I²C Electrical Characteristics table for additional information.)

Master device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave devices: Slave devices send and receive data at the master's request.

Bus idle or not busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition.

STOP condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

Repeated START condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTS are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition.

Bit write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements. Data is shifted into the device during the rising edge of the SCL.

Bit read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledge (ACK and NACK): An Acknowledge (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a 0 during the 9th bit. A device performs a NACK by transmitting a 1 during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or indicates that the device is not receiving data.

Byte write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgment from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgment is read using the bit read definition.

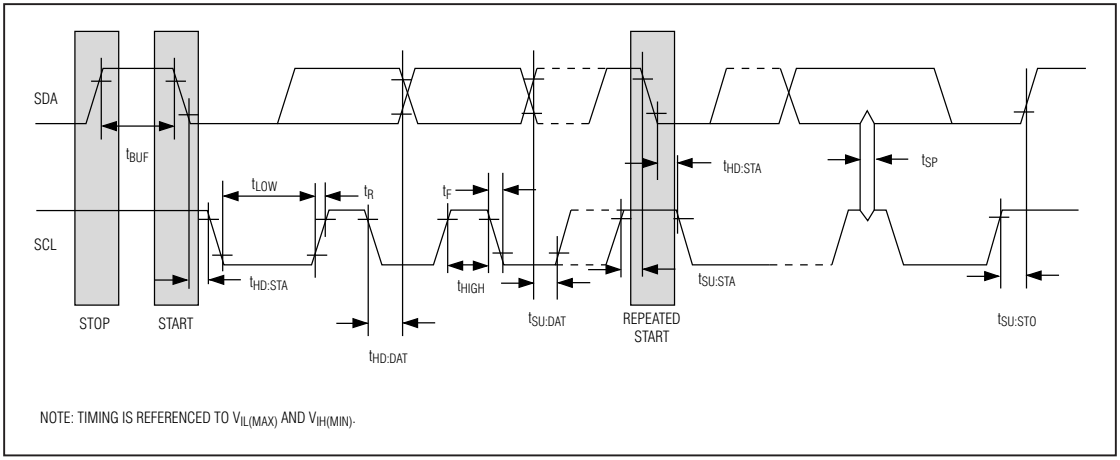


Figure 4. I²C Timing Diagram

I²C, 8-Channel Gamma Buffer with EEPROM

Byte read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave address byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS3508's slave address is determined by the state of the A0 address pin as shown in Figure 3. An address pin connected to GND results in a 0 in the corresponding bit position in the slave address. Conversely, an address pin connected to V_{CC} results in a 1 in the corresponding bit positions.

When the R/$\overline{W}$ bit is 0 (such as in E8h), the master is indicating that it will write data to the slave. If R/$\overline{W}$ = 1 (E9h in this case), the master is indicating that it wants to read from the slave.

If an incorrect slave address is written, the DS3508 assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

Memory address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

See Figure 5 for I²C communication examples.

Writing a single byte to a slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgment during all byte write operations.

When writing to the DS3508, the DAC adjusts to the new setting following a STOP. The EEPROM (used to make the setting NV) is written following the STOP condition at the end of the write command if the MODE bit is set to 0.

Writing multiple bytes to a slave: To write multiple bytes to a slave in one transaction, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the starting memory address, writes up to 4 data bytes, and generates a STOP condition. The DS3508 can write 1 to 4 bytes (1 page or row) in a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 4-byte page. The first page begins at address 00h and the second page begins at 04h. Attempts to write to additional pages of memory without sending a STOP condition between pages results in the address counter wrapping around to the beginning of the present row. To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM-write time to elapse. Then the master can generate a new START condition, and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge polling: Any time a EEPROM byte is written, the DS3508 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the byte to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS3508, which allows communication to continue as soon as the DS3508 is ready. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to access the device.

Reading a single byte from a slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

Reading multiple bytes from a slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another

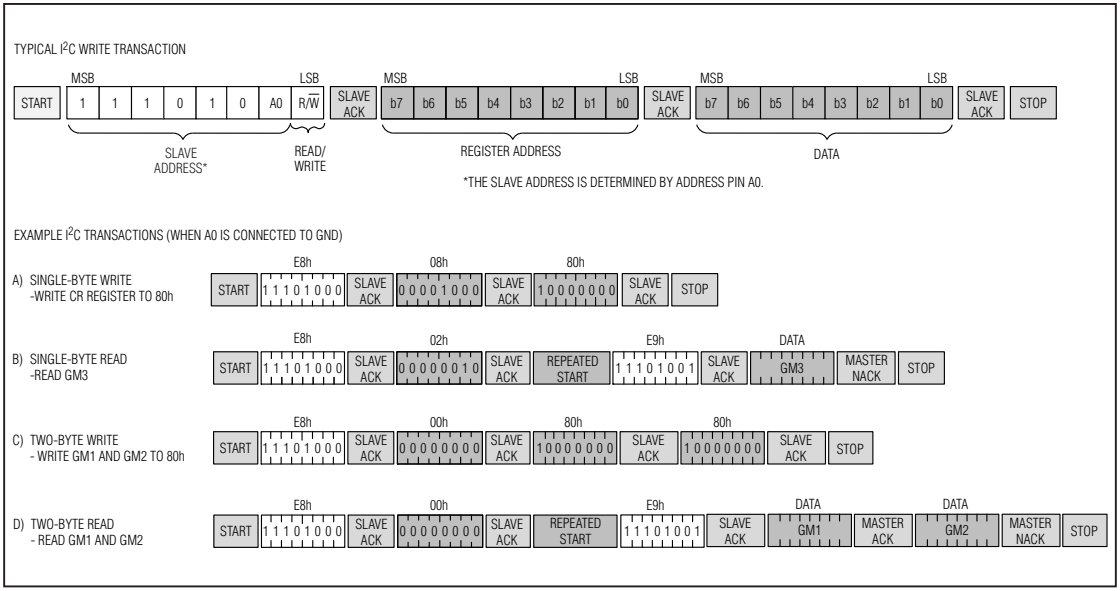


Figure 5. I²C Communication Examples

byte before terminating the transaction. After the master reads the last byte it must NACK to indicate the end of the transfer and generates a STOP condition.

Manipulating the address counter for reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition. The master must NACK the last byte to inform the slave that no additional bytes are to be read.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS3508, decouple both power-supply pins (V_{CC} and V_{DD}) with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

SDA and SCL Pullup Resistors

SDA is an I/O with an open-collector output that requires a pullup resistor to realize high-logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver can be used for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the electrical characteristics are within specification. A typical value for the pullup resistors is 4.7kΩ.

Package Information

(For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 TSSOP	—	56-G2010-000

I²C, 8-Channel Gamma Buffer with EEPROM

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/08	Initial release.	—
1	3/08	In the Nonvolatile Memory Characteristics table, removed T_A = +25°C 200,000 write cycle specification for EEPROM write cycles.	4

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