Low Noise, 90 MHz Variable Gain Amplifier

Data Sheet **AD603**

FEATURES

Linear-in-dB gain control
Pin-programmable gain ranges
−11 dB to +31 dB with 90 MHz bandwidth
9 dB to 51 dB with 9 MHz bandwidth
Any intermediate range, for example −1 dB to +41 dB with 30 MHz bandwidth
Bandwidth independent of variable gain
1.3 nV/√Hz input noise spectral density
±0.5 dB typical gain accuracy

APPLICATIONS

RF/IF AGC amplifiers
Video gain controls
A/D range extensions
Signal measurements

GENERAL DESCRIPTION

The AD603 is a low noise, voltage-controlled amplifier for use in RF and IF AGC systems. It provides accurate, pin-selectable gains of −11 dB to +31 dB with a bandwidth of 90 MHz or +9 dB to 51+ dB with a bandwidth of 9 MHz. Any intermediate gain range may be arranged using one external resistor. The input referred noise spectral density is only 1.3 nV/√Hz, and power consumption is 125 mW at the recommended ±5 V supplies.

The decibel gain is linear in dB, accurately calibrated, and stable over temperature and supply. The gain is controlled at a high impedance (50 MΩ), low bias (200 nA) differential input; the scaling is 25 mV/dB, requiring a gain control voltage of only 1 V to span the central 40 dB of the gain range. An overrange and underrange of 1 dB is provided whatever the selected range. The gain control response time is less than 1 µs for a 40 dB change.

The differential gain control interface allows the use of either differential or single-ended positive or negative control voltages. Several of these amplifiers may be cascaded and their gain control gains offset to optimize the system SNR.

The AD603 can drive a load impedance as low as 100 Ω with low distortion. For a 500 Ω load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically −60 dBc. The peak specified output is ±2.5 V minimum into a 500 Ω load.

The AD603 uses a patented proprietary circuit topology—the X-AMP®. The X-AMP comprises a variable attenuator of 0 dB to −42.14 dB followed by a fixed-gain amplifier. Because of the attenuator, the amplifier never has to cope with large inputs and can use negative feedback to define its (fixed) gain and dynamic performance. The attenuator has an input resistance of 100 Ω, laser trimmed to ±3%, and comprises a 7-stage R-2R ladder network, resulting in an attenuation between tap points of 6.021 dB. A proprietary interpolation technique provides a continuous gain control function that is linear in dB.

The AD603 is specified for operation from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

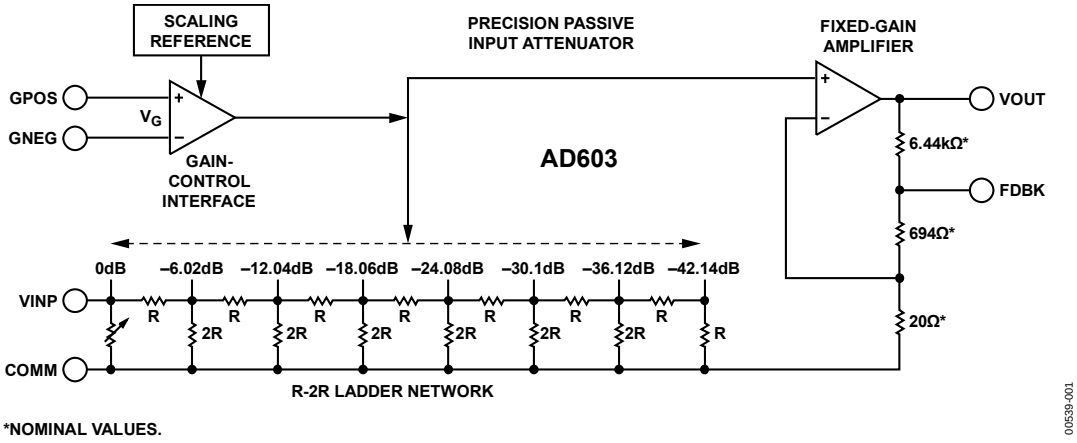


Figure 1.

Rev. K
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AD603* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD603 Evaluation Board

DOCUMENTATION

Application Notes

- AN-214: Ground Rules for High Speed Circuits

Data Sheet

- AD603: Military Data Sheet
- AD603: Low Noise, 90 MHz Variable Gain Amplifier Data Sheet

TOOLS AND SIMULATIONS

- AD603 SPICE Macro-Model

REFERENCE MATERIALS

Product Selection Guide

- Variable Gain Amplifier Selection Table

Tutorials

- Design and Operation of Automatic Gain Control Loops for Receivers in Modern Communication Systems

DESIGN RESOURCES

- AD603 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD603 EngineerZone Discussions.

SAMPLE AND BUY

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REVISION HISTORY

4/12—Rev. J to Rev. K

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Added Figure 10 and Figure 11; Renumbered Sequentially ... 7
Added Test Circuits Section ... 11
Moved Figure 29 and Figure 30 ... 11

12/11—Rev. I to Rev. J

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5/07—Rev. G to Rev. H

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3/05—Rev. F to Rev. G

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4/04—Rev. E to Rev. F

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8/03—Rev. D to Rev E

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SPECIFICATIONS

@ T_A = 25°C, V_S = ±5 V, –500 mV ≤ V_G ≤ +500 mV, GNEG = 0 V, –10 dB to +30 dB gain range, R_L = 500 Ω, and C_L = 5 pF, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Resistance	Pin 3 to Pin 4	97	100	103	Ω
Input Capacitance			2		pF
Input Noise Spectral Density[1]	Input short-circuited		1.3		nV/√Hz
Noise Figure	f = 10 MHz, gain = maximum, R_S = 10 Ω		8.8		dB
1 dB Compression Point	f = 10 MHz, gain = maximum, R_S = 10 Ω		−11		dBm
Peak Input Voltage			±1.4	±2	V
OUTPUT CHARACTERISTICS					
−3 dB Bandwidth	V_{OUT} = 100 mV rms		90		MHz
Slew Rate	R_L ≥ 500 Ω		275		V/µs
Peak Output[2]	R_L ≥ 500 Ω	±2.5	±3.0		V
Output Impedance	f ≤ 10 MHz		2		Ω
Output Short-Circuit Current			50		mA
Group Delay Change vs. Gain	f = 3 MHz; full gain range		±2		ns
Group Delay Change vs. Frequency	V_G = 0 V; f = 1 MHz to 10 MHz		±2		ns
Differential Gain			0.2		%
Differential Phase			0.2		Degree
Total Harmonic Distortion	f = 10 MHz, V_{OUT} = 1 V rms		−60		dBc
Third-Order Intercept	f = 40 MHz, gain = maximum, R_S = 50 Ω		15		dBm
ACCURACY					
Gain Accuracy, f = 100 kHz; Gain (dB) = (40 V_G + 10) dB	−500 mV ≤ V_G ≤ +500 mV	−1	±0.5	+1	dB
T_{MIN} to T_{MAX}		−1.5		+1.5	dB
Gain, f = 10.7 MHz	V_G = -0.5 V	−10.3	−9.0	−8.0	dB
	V_G = 0.0 V	+9.5	+10.5	+11.5	dB
	V_G = 0.5 V	+29.3	+30.3	+31.3	dB
Output Offset Voltage[3]	V_G = 0 V			20	mV
T_{MIN} to T_{MAX}				30	mV
Output Offset Variation vs. V_G	−500 mV ≤ V_G ≤ +500 mV			20	mV
T_{MIN} to T_{MAX}				30	mV
GAIN CONTROL INTERFACE					
Gain Scaling Factor	100 kHz	39.4	40	40.6	dB/V
T_{MIN} to T_{MAX}		38		42	dB/V
	10.7 MHz	38.7	39.3	39.9	dB/V
GNEG, GPOS Voltage Range[4]		−1.2		+2.0	V
Input Bias Current		50	100	250	nA
Input Offset Current			10		nA
Differential Input Resistance	Pin 1 to Pin 2		50		MΩ
Response Rate	Full 40 dB gain change		80		dB/µs
POWER SUPPLY					
Specified Operating Range		±4.75		±6.3	V
Quiescent Current			12.5	17	mA
T_{MIN} to T_{MAX}				20	mA

[1] Typical open or short-circuited input; noise is lower when system is set to maximum gain and input is short-circuited. This figure includes the effects of both voltage and current noise sources.
[2] Using resistive loads of 500 Ω or greater or with the addition of a 1 kΩ pull-down resistor when driving lower loads.
[3] The dc gain of the main amplifier in the AD603 is ×35.7; therefore, an input offset of 100 µV becomes a 3.57 mV output offset.
[4] GNEG and GPOS, gain control, and voltage range are guaranteed to be within the range of $-V_S$ + 4.2 V to $+V_S$ – 3.4 V over the full temperature range of –40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage $\pm V_S$	±7.5 V
Internal Voltage VINP (Pin 3)	±2 V Continuous
	$\pm V_S$ for 10 ms
GPOS, GNEG (Pin 1 and Pin2)	$\pm V_S$
Internal Power Dissipation	400 mW
Operating Temperature Range	
AD603A	−40°C to +85°C
AD603S	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	155	33	°C/W
8-Lead CERDIP	140	15	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

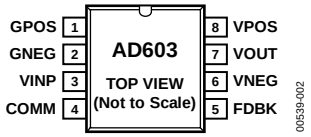


Figure 2. 8-Lead SOIC Pin Configuration

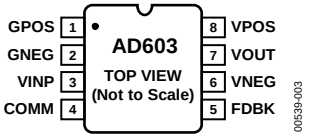


Figure 3. 8-Lead CERDIP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GPOS	Gain Control Input High (Positive Voltage Increases Gain).
2	GNEG	Gain Control Input Low (Negative Voltage Increases Gain).
3	VINP	Amplifier Input.
4	COMM	Amplifier Ground.
5	FDBK	Connection to Feedback Network.
6	VNEG	Negative Supply Input.
7	VOUT	Amplifier Output.
8	VPOS	Positive Supply Input.

TYPICAL PERFORMANCE CHARACTERISTICS

@ T_A = 25°C, V_S = ±5 V, −500 mV ≤ V_G ≤ +500 mV, GNEG = 0 V, −10 dB to +30 dB gain range, R_L = 500 Ω, and C_L = 5 pF, unless otherwise noted.

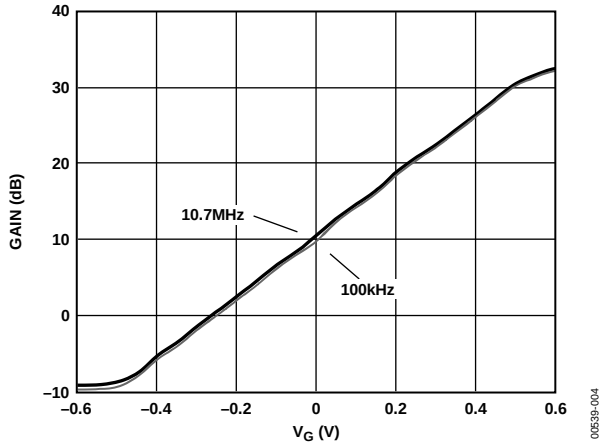


Figure 4. Gain vs. V_G at 100 kHz and 10.7 MHz

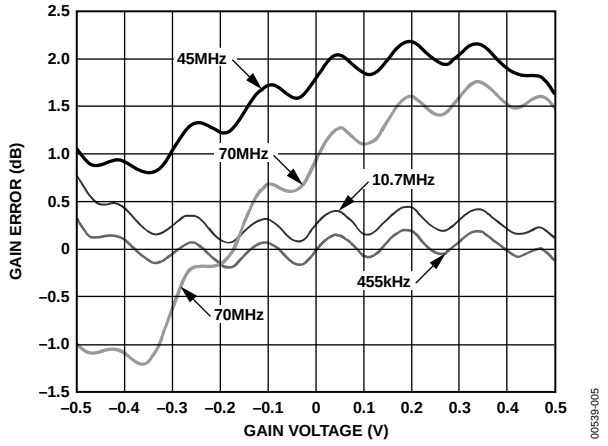


Figure 5. Gain Error vs. Gain Control Voltage at 455 kHz, 10.7 MHz, 45 MHz, 70 MHz

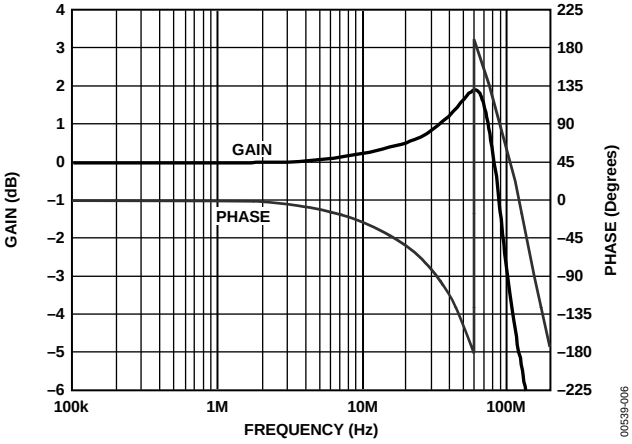


Figure 6. Frequency and Phase Response vs. Gain (Gain = −10 dB, P_{IN} = −30 dBm)

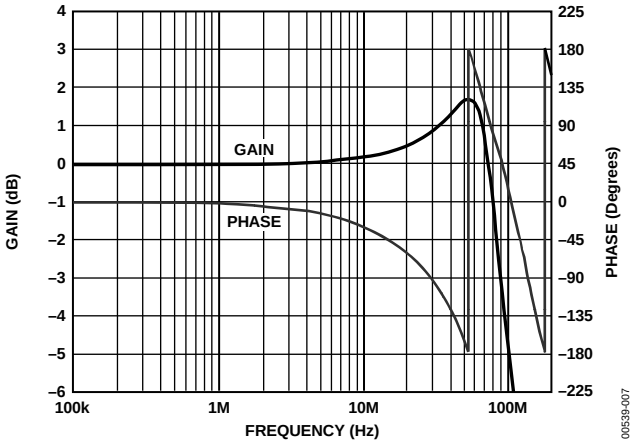


Figure 7. Frequency and Phase Response vs. Gain (Gain = 10 dB, P_{IN} = −30 dBm)

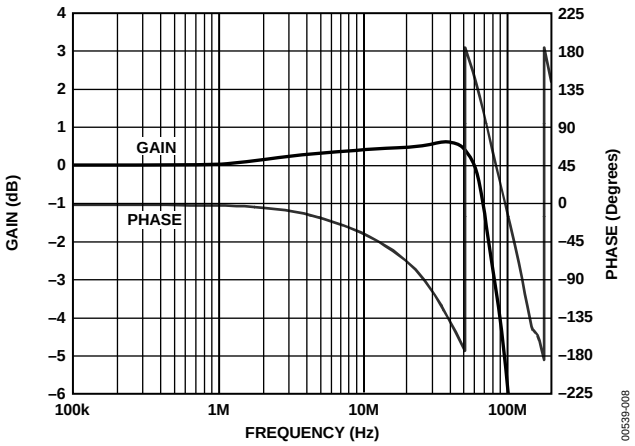


Figure 8. Frequency and Phase Response vs. Gain (Gain = 30 dB, P_{IN} = −30 dBm)

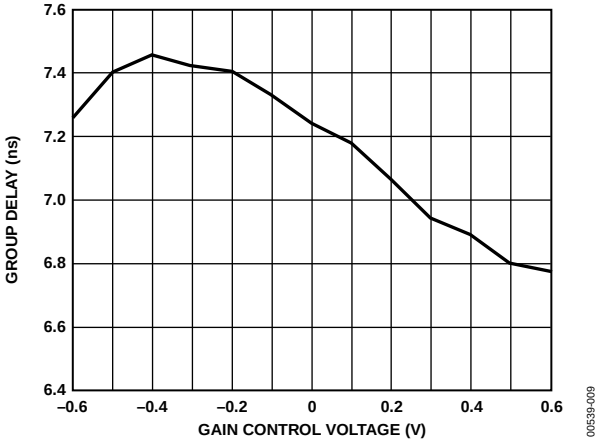


Figure 9. Group Delay vs. Gain Control Voltage

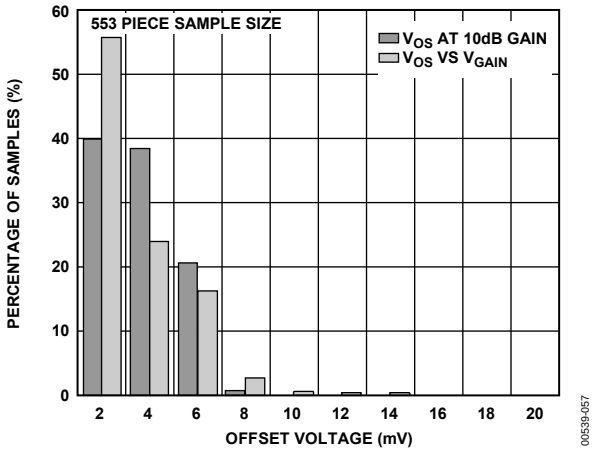


Figure 10. Histogram of V_{OS} at 10 dB Gain and V_{OS} vs. V_{GAIN}

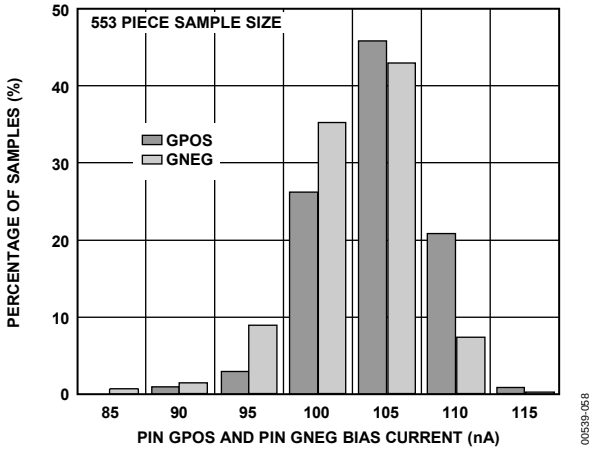


Figure 11. Histogram of GPOS and GNEG Bias Current

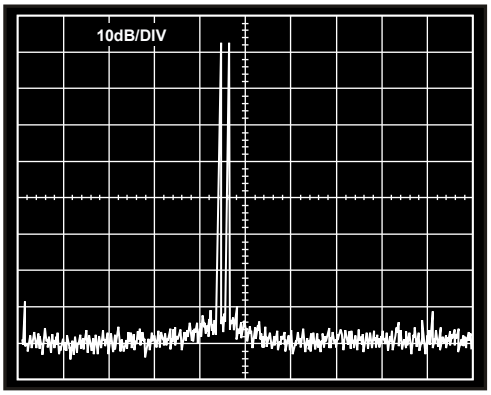


Figure 12. Third-Order Intermodulation Distortion at 455 kHz
(10× Probe Used to HP3585A Spectrum Analyzer, Gain = 0 dB, P_{IN} = 0 dBm)

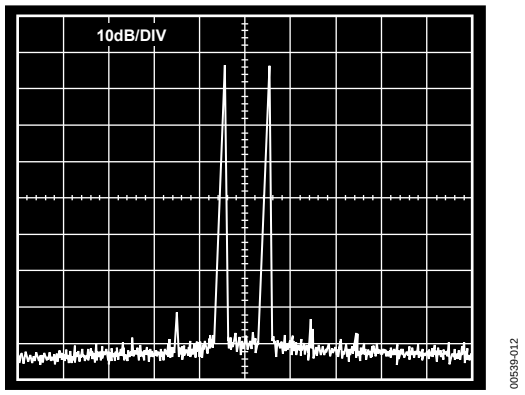


Figure 13. Third-Order Intermodulation Distortion at 10.7 MHz
(10× Probe Used to HP3585A Spectrum Analyzer, Gain = 0 dB, P_{IN} = 0 dBm)

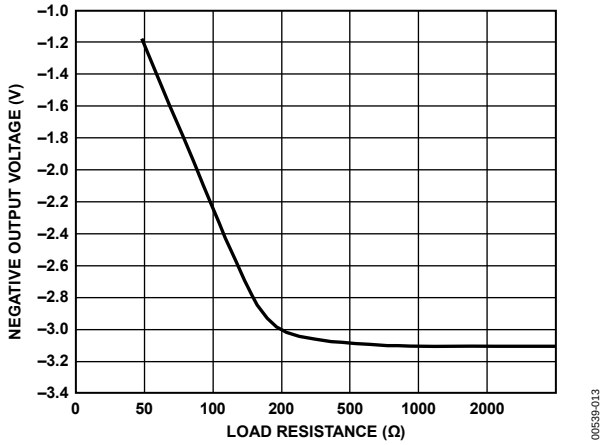


Figure 14. Typical Output Voltage Swing vs. Load Resistance
(Negative Output Swing Limits First)

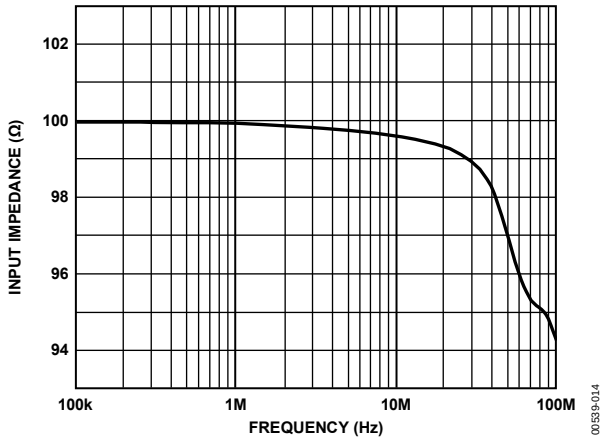


Figure 15. Input Impedance vs. Frequency (Gain = −10 dB)

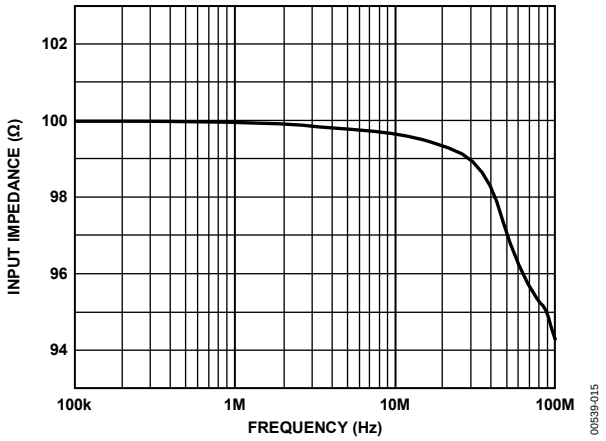


Figure 16. Input Impedance vs. Frequency (Gain = 10 dB)

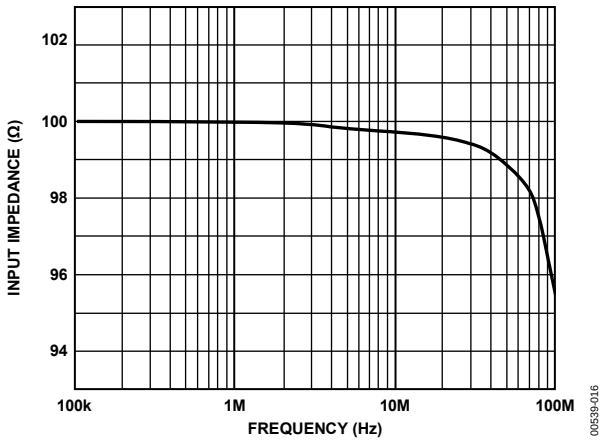


Figure 17. Input Impedance vs. Frequency (Gain = 30 dB)

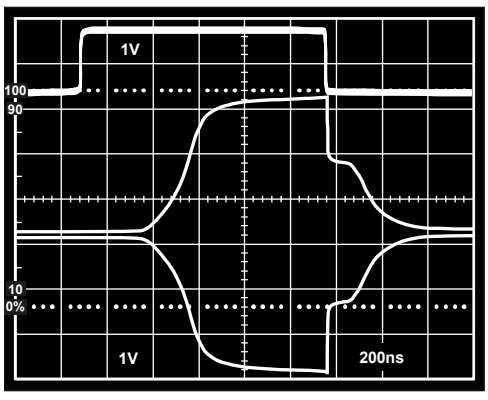


Figure 18. Gain Control Channel Response Time

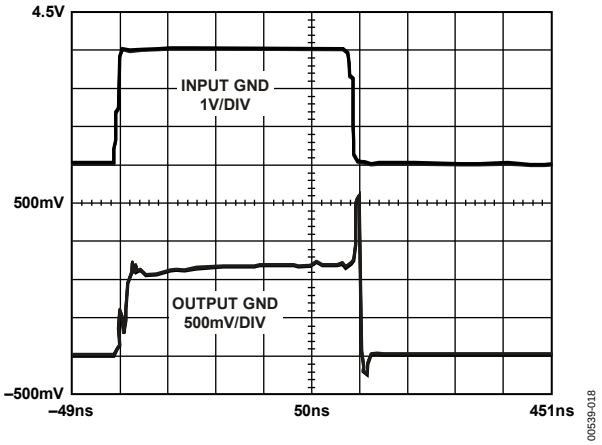


Figure 19. Input Stage Overload Recovery Time
(Input Is 500 ns Period, 50% Duty-Cycle Square Wave,
Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

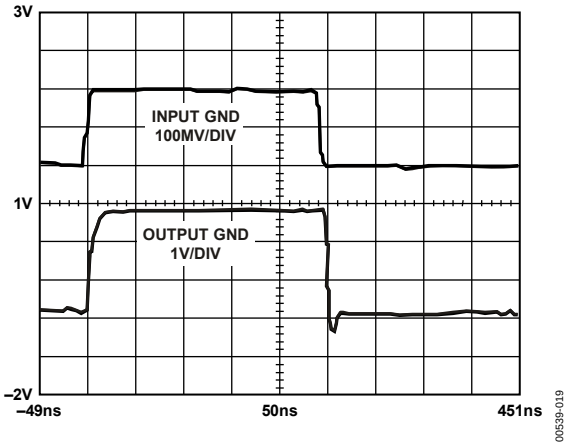


Figure 20. Output Stage Overload Recovery Time
(Input Is 500 ns Period, 50% Duty-Cycle Square Wave,
Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

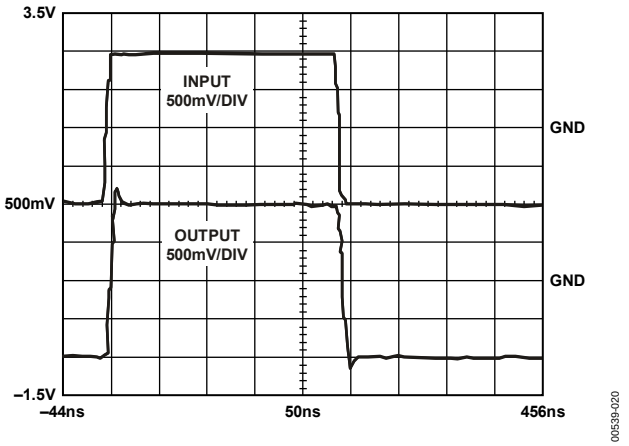


Figure 21. Transient Response, G = 0 dB
(Input Is 500 ns Period, 50% Duty-Cycle Square Wave,
Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

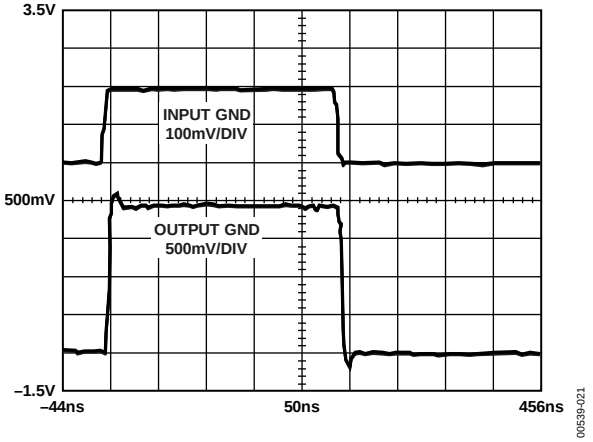


Figure 22. Transient Response, G = 20 dB (Input Is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)

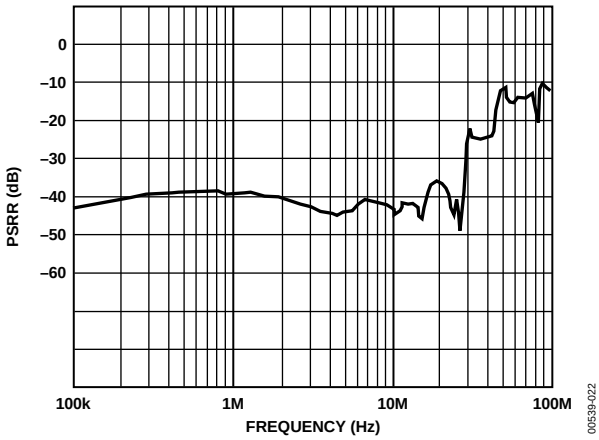


Figure 23. PSRR vs. Frequency (Worst Case Is Negative Supply PSRR, Shown Here)

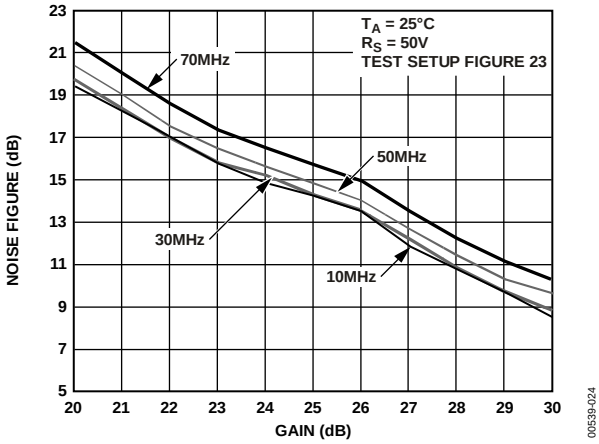


Figure 24. Noise Figure in –10 dB/+30 dB Mode

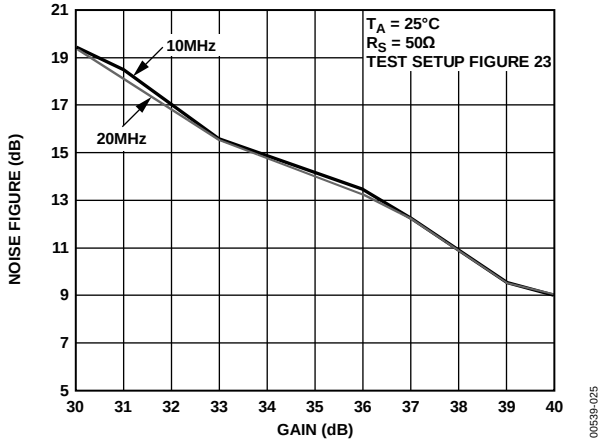


Figure 25. Noise Figure in 0 dB/40 dB Mode

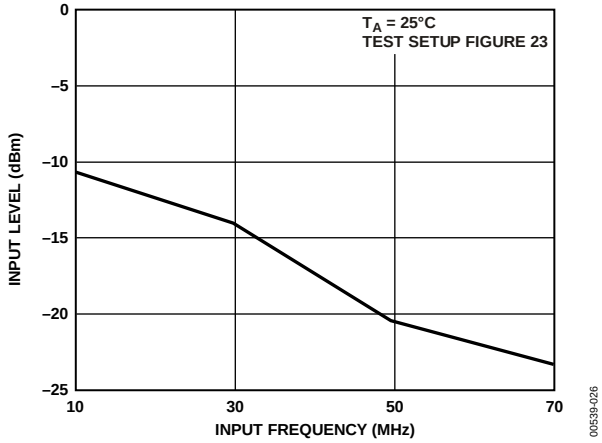


Figure 26. 1 dB Compression Point, –10 dB/+30 dB Mode, Gain = 30 dB

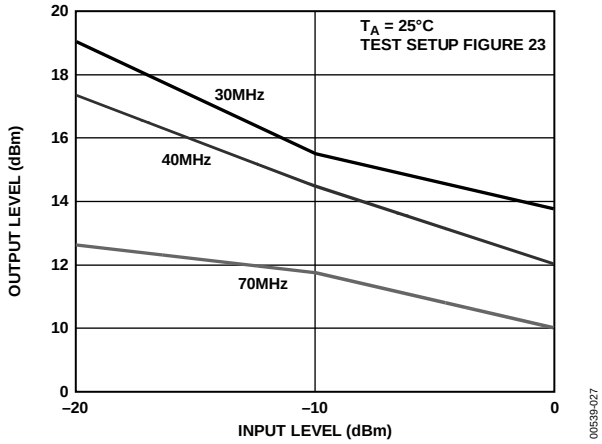


Figure 27. Third-Order Intercept –10 dB/+30 dB Mode, Gain = 10 dB

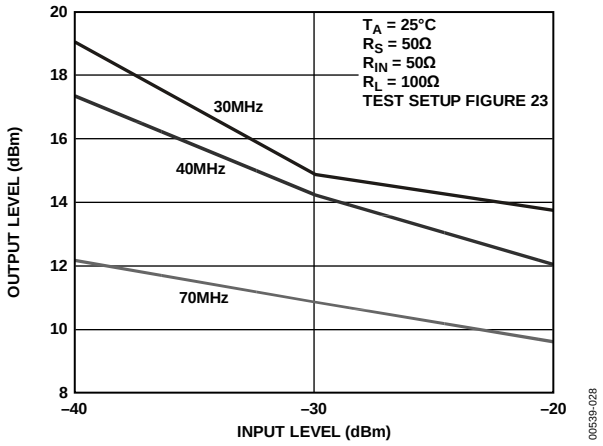


Figure 28. Third-Order Intercept −10 dB/+30 dB Mode, Gain = 30 dB

TEST CIRCUITS

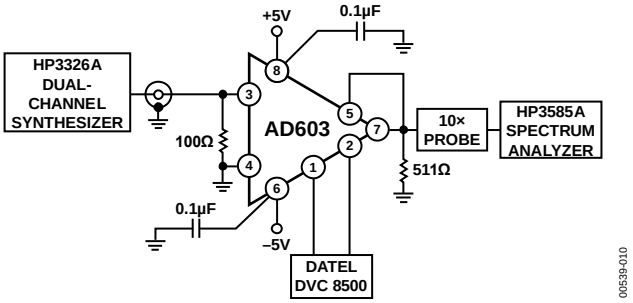


Figure 29. Third-Order Intermodulation Distortion Test Setup

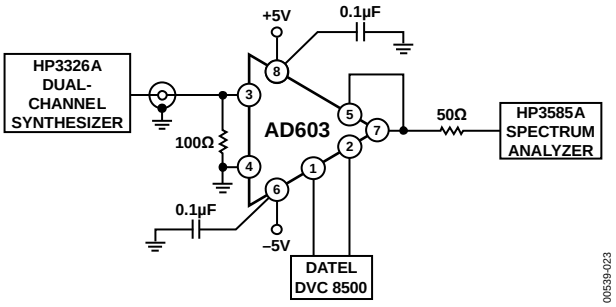


Figure 30. Test Setup Used for: Noise Figure, Third-Order Intercept, and 1 dB Compression Point Measurements

THEORY OF OPERATION

The AD603 comprises a fixed-gain amplifier, preceded by a broadband passive attenuator of 0 dB to 42.14 dB, having a gain control scaling factor of 40 dB per volt. The fixed gain is laser-trimmed in two ranges, to either 31.07 dB (×35.8) or 50 dB (×358), or it may be set to any range in between using one external resistor between Pin 5 and Pin 7. Somewhat higher gain can be obtained by connecting the resistor from Pin 5 to common, but the increase in output offset voltage limits the maximum gain to about 60 dB. For any given range, the bandwidth is independent of the voltage-controlled gain. This system provides an underrange and overrange of 1.07 dB in all cases; for example, the overall gain is −11.07 dB to +31.07 dB in the maximum bandwidth mode (Pin 5 and Pin 7 strapped).

This X-AMP structure has many advantages over former methods of gain control based on nonlinear elements. Most importantly, the fixed-gain amplifier can use negative feedback to increase its accuracy. Because large inputs are first attenuated, the amplifier input is always small. For example, to deliver a ±1 V output in the −1 dB/+41 dB mode (that is, using a fixed amplifier gain of 41.07 dB), its input is only 8.84 mV; therefore, the distortion can be very low. Equally important, the small-signal gain and phase response, and thus the pulse response, are essentially independent of gain.

Figure 31 is a simplified schematic. The input attenuator is a 7-section R-2R ladder network, using untrimmed resistors of nominally R = 62.5 Ω, which results in a characteristic resistance of 125 Ω ± 20%. A shunt resistor is included at the input and laser trimmed to establish a more exact input resistance of 100 Ω ± 3%, which ensures accurate operation (gain and HP corner frequency) when used in conjunction with external resistors or capacitors.

The nominal maximum signal at input VINP is 1 V rms (±1.4 V peak) when using the recommended ±5 V supplies, although operation to ±2 V peak is permissible with some increase in HF distortion and feedthrough. Pin 4 (COMM) must be connected directly to the input ground; significant impedance in this connection reduces the gain accuracy.

The signal applied at the input of the ladder network is attenuated by 6.02 dB by each section; therefore, the attenuation to each of the taps is progressively 0 dB, 6.02 dB, 12.04 dB, 18.06 dB, 24.08 dB, 30.1 dB, 36.12 dB, and 42.14 dB. A unique circuit technique is employed to interpolate between these tap points, indicated by the slider in Figure 31, thus providing continuous attenuation from 0 dB to 42.14 dB. It helps in understanding the AD603 to think in terms of a mechanical means for moving this slider from left to right; in fact, its position is controlled by the voltage between Pin 1 and Pin 2. The details of the gain control interface are in the The Gain Control Interface section.

The gain is at all times very exactly determined, and a linear-in-dB relationship is automatically guaranteed by the exponential nature of the attenuation in the ladder network (the X-AMP principle). In practice, the gain deviates slightly from the ideal law, by about ±0.2 dB peak (see, for example, Figure 5).

NOISE PERFORMANCE

An important advantage of the X-AMP is its superior noise performance. The nominal resistance seen at inner tap points is 41.7 Ω (one third of 125 Ω), which exhibits a Johnson noise spectral density (NSD) of 0.83 nV/√Hz (that is, √4kTR) at 27°C, which is a large fraction of the total input noise. The first stage of the amplifier contributes a further 1 nV/√Hz, for a total input noise of 1.3 nV/√Hz. It is apparent that it is essential to use a low resistance in the ladder network to achieve the very low specified noise level. The source impedance of the signal forms a voltage divider with the 100 Ω input resistance of the AD603. In some applications, the resulting attenuation may be unacceptable, requiring the use of an external buffer or preamplifier to match a high impedance source to the low impedance AD603.

The noise at maximum gain (that is, at the 0 dB tap) depends on whether the input is short-circuited or open-circuited. When short-circuited, the minimum NSD of slightly over 1 nV/√Hz is achieved. When open-circuited, the resistance of 100 Ω looking into the first tap generates 1.29 nV/√Hz, so the noise increases to 1.63 nV/√Hz. (This last calculation would be important if the AD603 were preceded by, for example, a 900 Ω resistor to allow operation from inputs up to 10 V rms.) As the selected tap moves away from the input, the dependence of the noise on source impedance quickly diminishes.

Apart from the small variations just discussed, the signal-to-noise (SNR) at the output is essentially independent of the attenuator setting. For example, on the −11 dB/+31 dB range, the fixed gain of ×35.8 raises the output NSD to 46.5 nV/√Hz. Therefore, for the maximum undistorted output of 1 V rms and a 1 MHz bandwidth, the output SNR would be 86.6 dB, that is, 20 log(1 V/46.5 μV).

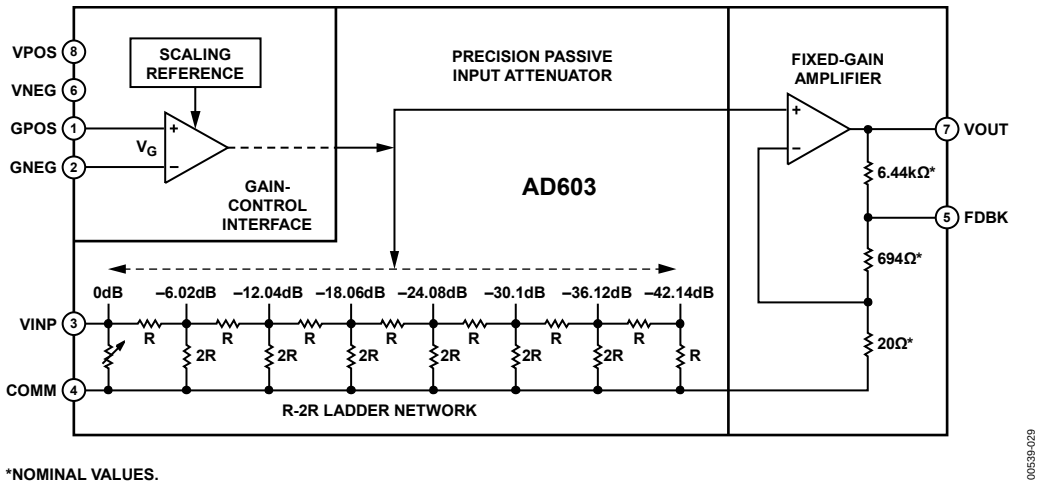


Figure 31. Simplified Block Diagram

THE GAIN CONTROL INTERFACE

The attenuation is controlled through a differential, high impedance (50 MΩ) input, with a scaling factor that is laser-trimmed to 40 dB per volt, that is, 25 mV/dB. An internal band gap reference ensures stability of the scaling with respect to supply and temperature variations.

When the differential input voltage V_G = 0 V, the attenuator slider is centered, providing an attenuation of 21.07 dB. For the maximum bandwidth range, this results in an overall gain of 10 dB (= −21.07 dB + 31.07 dB). When the control input is −500 mV, the gain is lowered by +20 dB (= 0.500 V × 40 dB/V) to −10 dB; when set to +500 mV, the gain is increased by +20 dB to +30 dB. When this interface is overdriven in either direction, the gain approaches either −11.07 dB (= − 42.14 dB + +31.07 dB) or 31.07 dB (= 0 + 31.07 dB), respectively. The only constraint on the gain control voltage is that it be kept within the common-mode range (−1.2 V to +2.0 V assuming +5 V supplies) of the gain control interface.

The basic gain of the AD603 can therefore be calculated by

$$Gain\ (\text{dB}) = 40\ V_G + 10 \quad (1)$$

where V_G is in volts. When Pin 5 and Pin 7 are strapped (see the Programming the Fixed-Gain Amplifier Using Pin Strapping section), the gain becomes

$$Gain\ (\text{dB}) = 40\ V_G + 20\ for\ 0\ to\ +40\ \text{dB}$$

and

$$Gain\ (\text{dB}) = 40\ V_G + 30\ for\ +10\ to\ +50\ \text{dB} \quad (2)$$

The high impedance gain control input ensures minimal loading when driving many amplifiers in multiple channel or cascaded applications. The differential capability provides flexibility in choosing the appropriate signal levels and polarities for various control schemes.

For example, if the gain is to be controlled by a DAC providing a positive-only, ground-referenced output, the gain control low (GNEG) pin should be biased to a fixed offset of 500 mV to set the gain to −10 dB when gain control high (GPOS) is at zero, and to 30 dB when at 1.00 V.

It is a simple matter to include a voltage divider to achieve other scaling factors. When using an 8-bit DAC having an FS output of 2.55 V (10 mV/bit), a divider ratio of 2 (generating 5 mV/bit) results in a gain-setting resolution of 0.2 dB/bit. The use of such offsets is valuable when two AD603s are cascaded, when various options exist for optimizing the signal-to-noise profile, as is shown in the Sequential Mode (Optimal SNR) section,

PROGRAMMING THE FIXED-GAIN AMPLIFIER USING PIN STRAPPING

Access to the feedback network is provided at Pin 5 (FDBK). The user may program the gain of the output amplifier of the AD603 using this pin, as shown in Figure 32, Figure 33, and Figure 34. There are three modes: in the default mode, FDBK is unconnected, providing the range +9 dB/+51 dB; when V_{OUT} and FDBK are shorted, the gain is lowered to −11 dB/+31 dB; and, when an external resistor is placed between V_{OUT} and FDBK, any intermediate gain can be achieved, for example, −1 dB/+41 dB. Figure 35 shows the nominal maximum gain vs. external resistor for this mode.

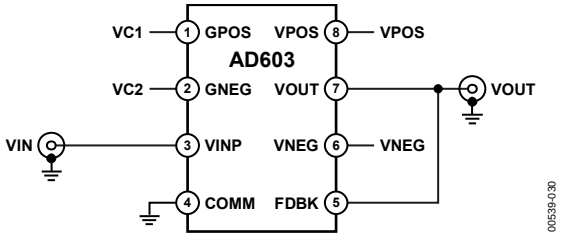


Figure 32. −10 dB to +30 dB; 90 MHz Bandwidth

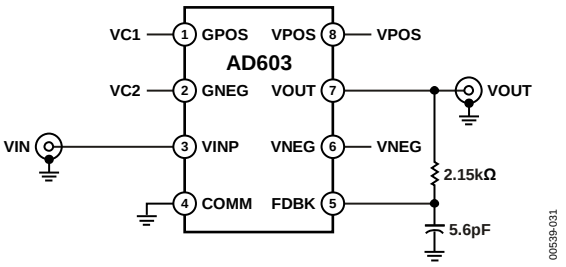


Figure 33. 0 dB to 40 dB; 30 MHz Bandwidth

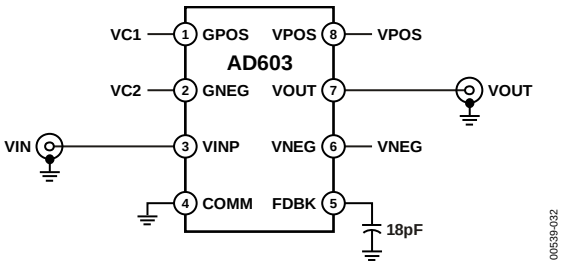


Figure 34. 10 dB to 50 dB; 9 MHz to Set Gain

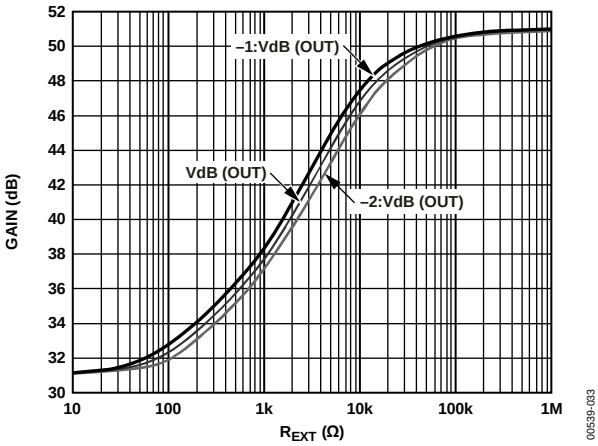


Figure 35. Gain vs. R_{EXT}, Showing Worst-Case Limits Assuming Internal Resistors Have a Maximum Tolerance of 20%

Optionally, when a resistor is placed from FDBK to COMM, higher gains can be achieved. This fourth mode is of limited value because of the low bandwidth and the elevated output offsets; it is thus not included in Figure 32, Figure 33, or Figure 34.

The gain of this amplifier in the first two modes is set by the ratio of on-chip laser-trimmed resistors. While the ratio of these resistors is very accurate, the absolute value of these resistors can vary by as much as ±20%. Therefore, when an external resistor is connected in parallel with the nominal 6.44 kΩ ± 20% internal resistor, the overall gain accuracy is somewhat poorer. The worst-case error occurs at about 2 kΩ (see Figure 36).

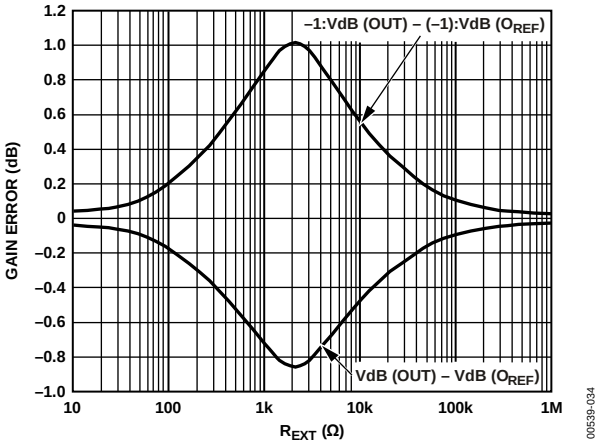


Figure 36. Worst-Case Gain Error, Assuming Internal Resistors Have a Maximum Tolerance of –20% (Top Curve) or = 20% (Bottom Curve)

While the gain bandwidth product of the fixed-gain amplifier is about 4 GHz, the actual bandwidth is not exactly related to the maximum gain. This is because there is a slight enhancing of the ac response magnitude on the maximum bandwidth range, due to higher order poles in the open-loop gain function; this mild peaking is not present on the higher gain ranges. Figure 32, Figure 33, and Figure 34 show how an optional capacitor may be added to extend the frequency response in high gain modes.

USING THE AD603 IN CASCADE

Two or more AD603s can be connected in series to achieve higher gain. Invariably, ac coupling must be used to prevent the dc offset voltage at the output of each amplifier from overloading the following amplifier at maximum gain. The required high-pass coupling network is usually just a capacitor, chosen to set the desired corner frequency in conjunction with the well-defined 100 Ω input resistance of the following amplifier.

For two AD603s, the total gain control range becomes 84 dB (2 × 42.14 dB); the overall −3 dB bandwidth of cascaded stages is somewhat reduced. Depending on the pin strapping, the gain and bandwidth for two cascaded amplifiers can range from −22 dB to +62 dB (with a bandwidth of about 70 MHz) to +22 dB to +102 dB (with a bandwidth of about 6 MHz).

There are several ways of connecting the gain control inputs in cascaded operation. The choice depends on whether it is important to achieve the highest possible instantaneous signal-to-noise ratio (ISNR), or, alternatively, to minimize the ripple in the gain error. The following examples feature the AD603 programmed for maximum bandwidth; the explanations apply to other gain/bandwidth combinations with appropriate changes to the arrangements for setting the maximum gain.

SEQUENTIAL MODE (OPTIMAL SNR)

In the sequential mode of operation, the ISNR is maintained at its highest level for as much of the gain control range as possible. Figure 37 shows the SNR over a gain range of −22 dB to +62 dB, assuming an output of 1 V rms and a 1 MHz bandwidth. Figure 38, Figure 39, and Figure 40 show the general connections to accomplish this. Here, both the positive gain control inputs (GPOS) are driven in parallel by a positive-only, ground-referenced source with a range of 0 V to 2 V, while the negative gain control inputs (GNEG) are biased by stable voltages to provide the needed gain offsets. These voltages may be provided by resistive dividers operating from a common voltage reference.

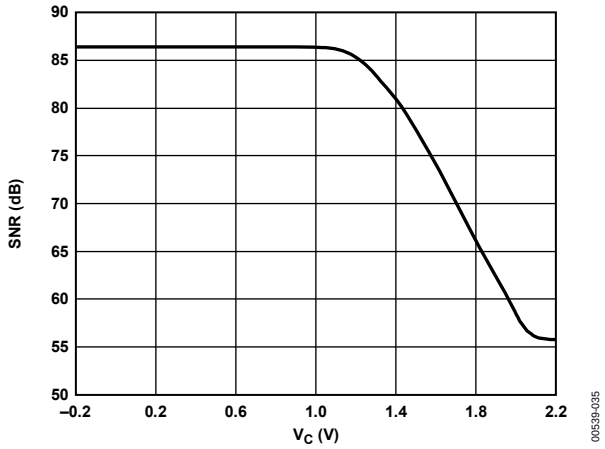


Figure 37. SNR vs. Control Voltage, Sequential Control (1 MHz Bandwidth)

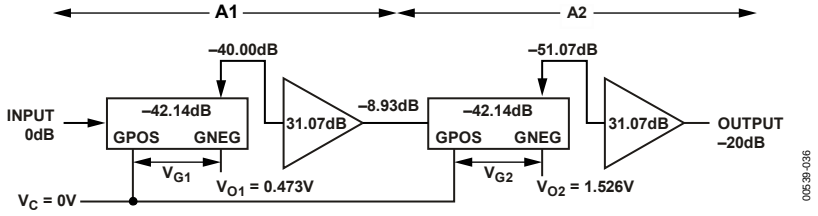


Figure 38. AD603 Gain Control Input Calculations for Sequential Control Operation V_C = 0 V

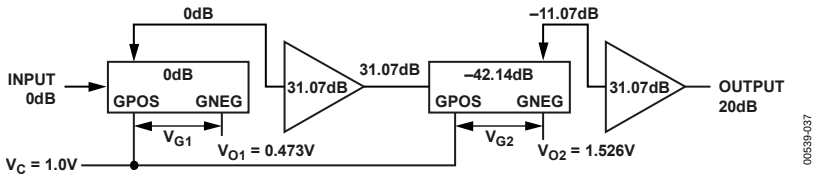


Figure 39. AD603 Gain Control Calculations for Sequential Control Operation V_C = 1.0 V

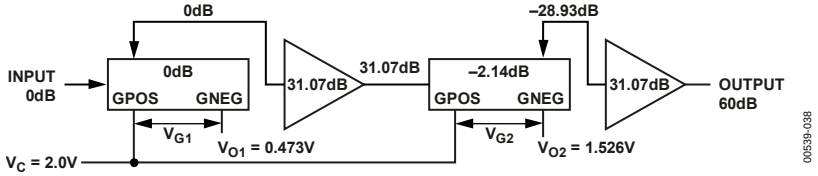


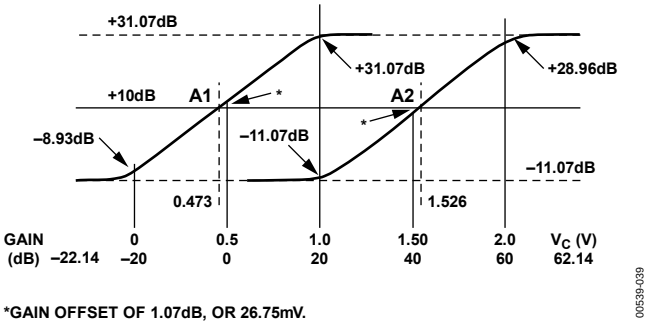
Figure 40. AD603 Gain Control Input Calculations for Sequential Operation V_C = 2.0 V

The gains are offset (Figure 41) such that the gain of A2 is increased only after the gain of A1 has reached its maximum value. Note that for a differential input of −600 mV or less, the gain of a single amplifier (A1 or A2) is at its minimum value of −11.07 dB; for a differential input of 600 mV or more, the gain is at its maximum value of 31.07 dB. Control inputs beyond these limits do not affect the gain and can be tolerated without damage or foldover in the response. This is an important aspect of the gain control response of the AD603. (See the Specifications section for more details on the allowable voltage range.) The gain is now

$$Gain\ (\text{dB}) = 40\ V_G + G_O \quad (3)$$

where:
V_G is the applied control voltage.
G_O is determined by the gain range chosen.

In the explanatory notes that follow, it is assumed that the maximum bandwidth connections are used, for which G_O is −20 dB.



*GAIN OFFSET OF 1.07dB, OR 26.75mV.

Figure 41. Explanation of Offset Calibration for Sequential Control

With reference to Figure 38, Figure 39, and Figure 40, note that V_{G1} refers to the differential gain control input to A1, and V_{G2} refers to the differential gain control input to A2. When V_G is 0 V, V_{G1} = −473 mV and thus the gain of A1 is −8.93 dB (recall that the gain of each individual amplifier in the maximum bandwidth mode is –10 dB for V_G = −500 mV and 10 dB for V_G = 0 V); meanwhile, V_{G2} = −1.908 V so the gain of A2 is pinned at −11.07 dB. The overall gain is therefore –20 dB (see Figure 38).

When V_G = 1.00 V, V_{G1} = 1.00 V − 0.473 V = 0.526 V, which sets the gain of A1 to nearly its maximum value of +31.07 dB, while V_{G2} = 1.00 V − 1.526 V = 0.526 V, which sets the gain of A2 to nearly its minimum value of −11.07 dB. Close analysis shows that the degree to which neither AD603 is completely pushed to its maximum nor minimum gain exactly cancels in the overall gain, which is now 20 dB (see Figure 39).

When V_G = 2.0 V, the gain of A1 is pinned at 31.07 dB and that of A2 is near its maximum value of 28.93 dB, resulting in an overall gain of 60 dB (see Figure 40). This mode of operation is further clarified in Figure 42, which is a plot of the separate gains of A1 and A2 and the overall gain vs. the control voltage.

Figure 43 is a plot of the SNR of the cascaded amplifiers vs. the control voltage. Figure 44 is a plot of the gain error of the cascaded stages vs. the control voltages.

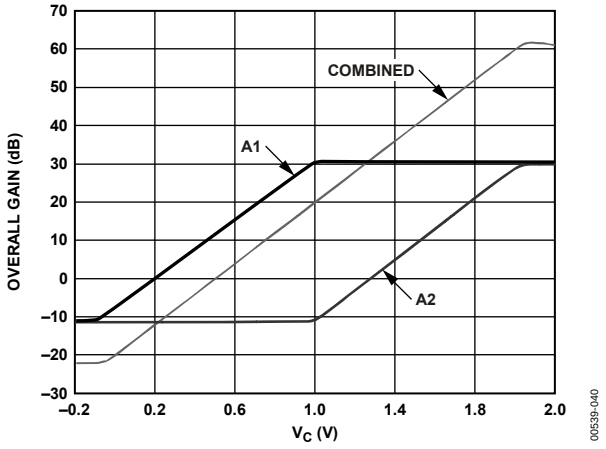


Figure 42. Plot of Separate and Overall Gains in Sequential Control

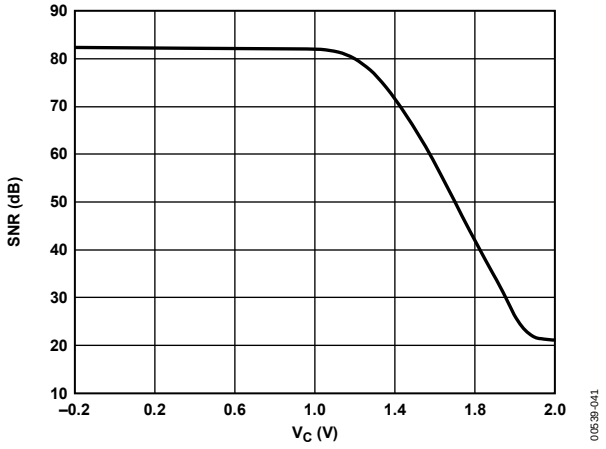


Figure 43. SNR for Cascaded Stages—Sequential Control

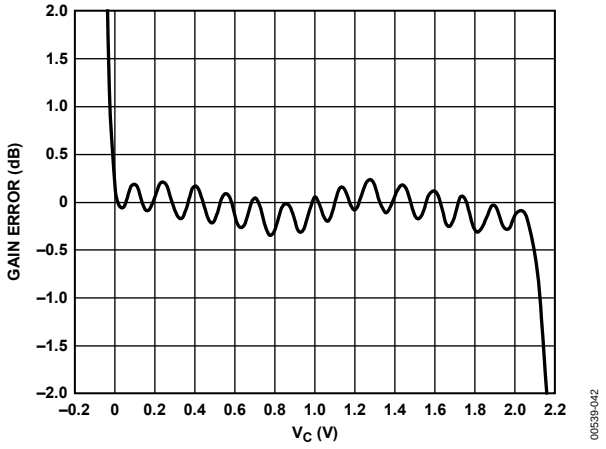


Figure 44. Gain Error for Cascaded Stages–Sequential Control

PARALLEL MODE (SIMPLEST GAIN CONTROL INTERFACE)

In this mode, the gain control of voltage is applied to both inputs in parallel: the GPOS pins of both A1 and A2 are

connected to the control voltage and the GNEW inputs are grounded. The gain scaling is then doubled to 80 dB/V, requiring only a 1.00 V change for an 80 dB change of gain

$$Gain = (\text{dB}) = 80\ V_G + G_O \quad (4)$$

where, as before, G_O depends on the range selected; for example, in the maximum bandwidth mode, G_O is 20 dB. Alternatively, the GNEG pins may be connected to an offset voltage of 0.500 V, in which case G_O is −20 dB.

The amplitude of the gain ripple in this case is also doubled, as shown in Figure 45, while the ISNR at the output of A2 now decreases linearly as the gain increases, as shown in Figure 46.

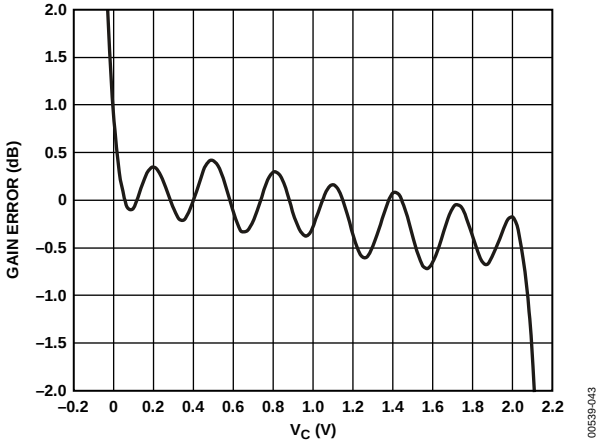


Figure 45. Gain Error for Cascaded Stages—Parallel Control

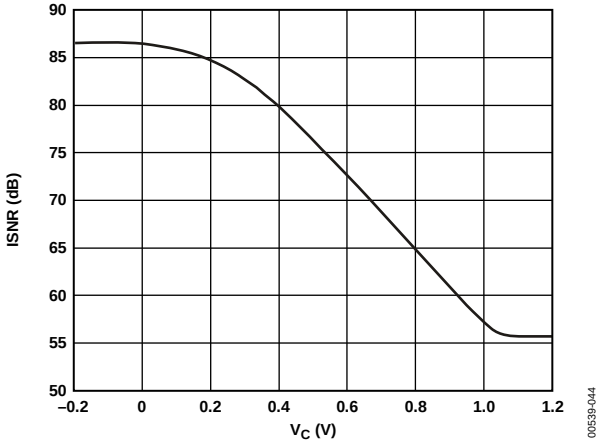


Figure 46. ISNR for Cascaded Stages—Parallel Control

LOW GAIN RIPPLE MODE (MINIMUM GAIN ERROR)

As can be seen in Figure 44 and Figure 45, the error in the gain is periodic, that is, it shows a small ripple. (Note that there is also a variation in the output offset voltage, which is due to the gain interpolation, but this is not exact in amplitude.) By offsetting the gains of A1 and A2 by half the period of the ripple, that is, by 3 dB, the residual gain errors of the two amplifiers can be made to cancel. Figure 47 shows much lower gain ripple when configured in this manner. Figure 48 plots the ISNR as a function of gain; it is very similar to that in the parallel mode.

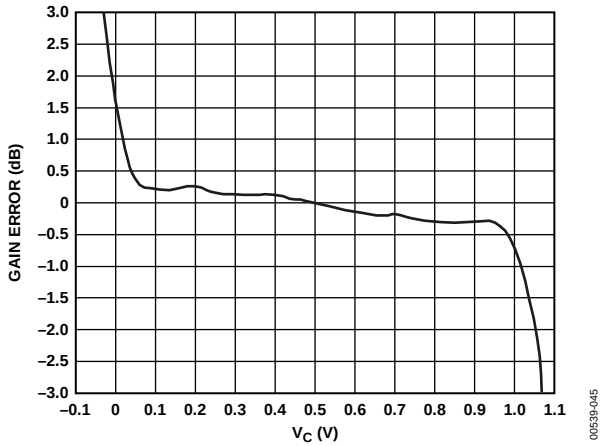


Figure 47. Gain Error for Cascaded Stages—Low Ripple Mode

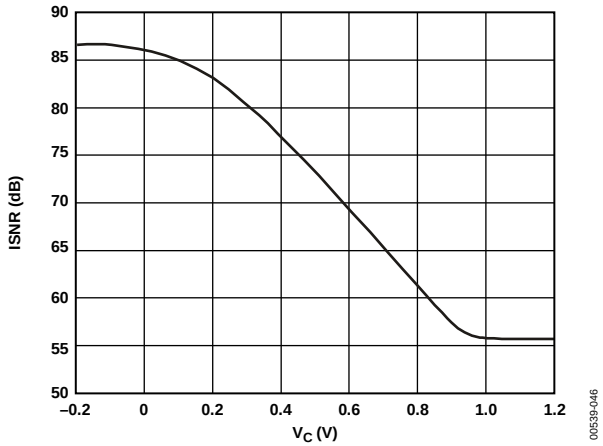


Figure 48. ISNR vs. Control Voltage—Low Ripple Mode

APPLICATIONS INFORMATION

A LOW NOISE AGC AMPLIFIER

Figure 49 shows the ease with which the AD603 can be connected as an AGC amplifier. The circuit illustrates many of the points previously discussed: it uses few parts, has linear-in-dB gain, operates from a single supply, uses two cascaded amplifiers in sequential gain mode for maximum SNR, and an external resistor programs each gain of the amplifier. It also uses a simple temperature-compensated detector.

The circuit operates from a single 10 V supply. Resistors R1, R2, R3, and R4 bias the common pins of A1 and A2 at 5 V. The common pin is a low impedance point and must have a low impedance path to ground, provided here by the 100 µF tantalum capacitors and the 0.1 µF ceramic capacitors.

The cascaded amplifiers operate in sequential gain. Here, the offset voltage between Pin 2 (GNEG) of A1 and A2 is 1.05 V (42.14 dB × 25 mV/dB), provided by a voltage divider consisting of Resistors R5, R6, and R7. Using standard values, the offset is not exact, but it is not critical for this application.

The gain of both A1 and A2 is programmed by Resistors R13 and R14, respectively, to be about 42 dB; therefore, the maximum gain of the circuit is twice that, or 84 dB. The gain control range can be shifted up by as much as 20 dB by appropriate choices of R13 and R14.

The circuit operates as follows:

- A1 and A2 are cascaded.
- Capacitor C1 and the 100 Ω of resistance at the input of A1 form a time constant of 10 µs.
- C2 blocks the small dc offset voltage at the output of A1 (which might otherwise saturate A2 at its maximum gain) and introduces a high-pass corner at about 16 kHz, eliminating low frequency noise.

A half-wave detector is used, based on Q1 and R8. The current into capacitor, C_{AV}, is the difference between the collector current of Q2 (biased to be 300 µA at 300 K, 27°C) and the collector current of Q1, which increases with the amplitude of the output signal.

The automatic gain control voltage, V_{AGC}, is the time integral of this error current. For V_{AGC} (and thus the gain) to remain insensitive to short-term amplitude fluctuations in the output signal, the rectified current in Q1 must, on average, exactly balance the current in Q2. If the output of A2 is too small to do this, V_{AGC} increases, causing the gain to increase until Q1 conducts sufficiently.

Consider the case where R8 is zero and the output voltage V_{OUT} is a square wave at, for example, 455 kHz, which is well above the corner frequency of the control loop.

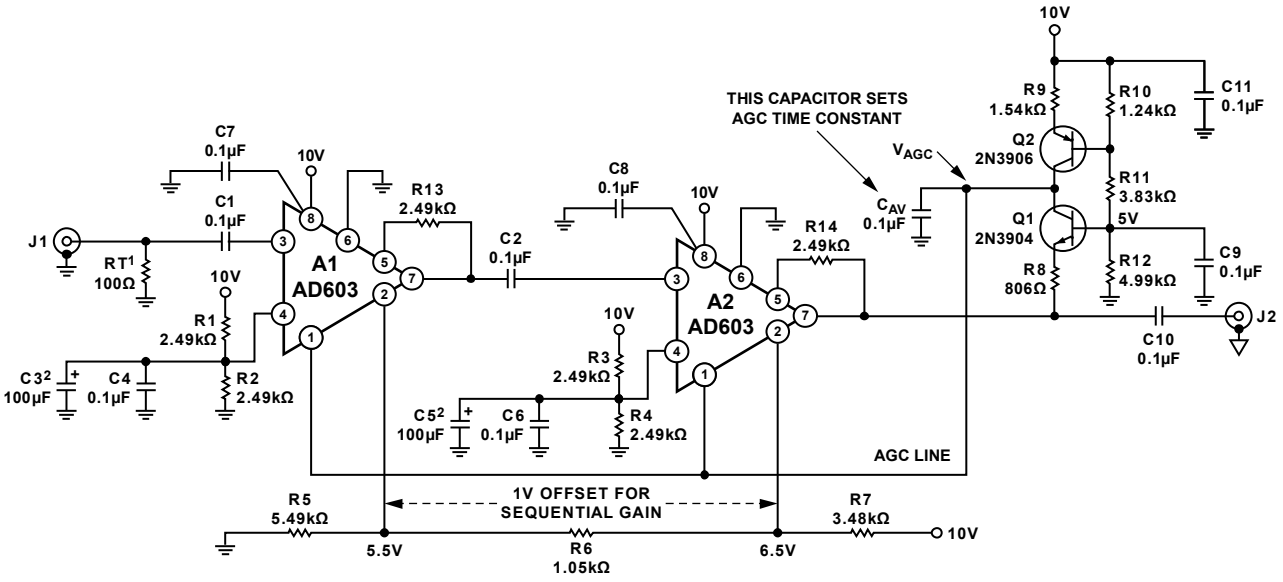


Figure 49. A Low Noise AGC Amplifier

During the time V_{OUT} is negative with respect to the base voltage of Q1, Q1 conducts; when V_{OUT} is positive, it is cut off. Because the average collector current of Q1 is forced to be 300 μA, and the square wave has a duty cycle of 1:1, Q1's collector current when conducting must be 600 μA. With R8 omitted, the peak amplitude of V_{OUT} is forced to be just the V_{BE} of Q1 at 600 μA, typically about 700 mV, or 2 V_{BE} peak-to-peak. This voltage, the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically −1.7 mV/°C. Although this may not be troublesome in some applications, the correct value of R8 renders the output stable with temperature.

To understand this, note that the current in Q2 is made to be proportional to absolute temperature (PTAT). For the moment, continue to assume that the signal is a square wave.

When Q1 is conducting, V_{OUT} is now the sum of V_{BE} and a voltage that is PTAT and that can be chosen to have an equal but opposite TC to that of the V_{BE}. This is actually nothing more than an application of the band gap voltage reference principle. When R8 is chosen such that the sum of the voltage across it and the V_{BE} of Q1 is close to the band gap voltage of about 1.2 V, V_{OUT} is stable over a wide range of temperatures, provided, of course, that Q1 and Q2 share the same thermal environment.

Because the average emitter current is 600 μA during each half cycle of the square wave, a resistor of 833 Ω adds a PTAT voltage of 500 mV at 300 K, increasing by 1.66 mV/°C. In practice, the optimum value depends on the type of transistor used and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the inexpensive 2N3904/2N3906 pair and sine wave signals, the recommended value is 806 Ω.

This resistor also serves to lower the peak current in Q1 when more typical signals (usually sinusoidal) are involved, and the 1.8 kHz LP filter it forms with C_{AV} helps to minimize distortion due to ripple in V_{AGC}. Note that the output amplitude under sine wave conditions is higher than for a square wave because the average value of the current for an ideal rectifier is 0.637 times as large, causing the output amplitude to be 1.88 (= 1.2/0.637) V, or 1.33 V rms. In practice, the somewhat nonideal rectifier results in the sine-wave output being regulated to about 1.4 V rms, or 3.6 V p-p.

The bandwidth of the circuit exceeds 40 MHz. At 10.7 MHz, the AGC threshold is 100 μV (−67 dBm) and its maximum gain is 83 dB (20 log 1.4 V/100 μV). The circuit holds its output at 1.4 V rms for inputs as low as −67 dBm to +15 dBm (82 dB), where the input signal exceeds the maximum input rating of the AD603. For a 30 dBm input at 10.7 MHz, the second harmonic is 34 dB down from the fundamental, and the third harmonic is 35 dB down from the fundamental.

CAUTION

Careful component selection, circuit layout, power supply decoupling, and shielding are needed to minimize the susceptibility of the AD603 to interference from signals such as those from radio and TV stations. In bench evaluation, it is recommended to place all of the components into a shielded box and use feedthrough decoupling networks for the supply voltage. Circuit layout and construction are also critical because stray capacitances and lead inductances can form resonant circuits and are a potential source of circuit peaking, oscillation, or both.

EVALUATION BOARD

The evaluation board of the AD603 enables simple bench-top experimenting to be performed with easy control of the AD603. Built-in flexibility allows convenient configuration to accommodate most operating configurations. Figure 50 is a photograph of the AD603 evaluation board.

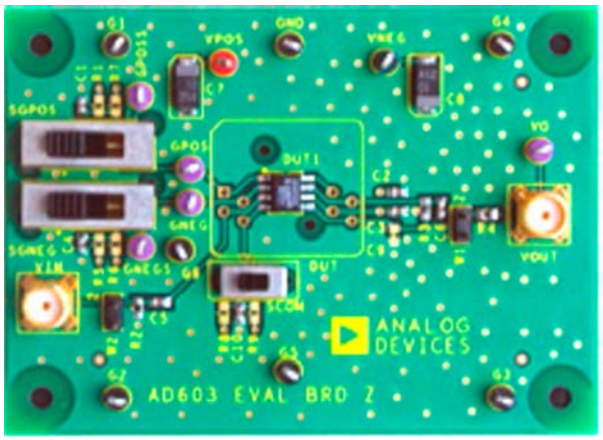


Figure 50. AD603 Evaluation Board

Any dual-polarity power supply capable of providing 20 mA is all that is required, in addition to whatever test equipment the user wishes to perform the intended tests.

Referring to the schematic in Figure 51, the input to the VGA is single-ended, ac-coupled, and terminated in 50 Ω to accommodate most commonly available signal generators.

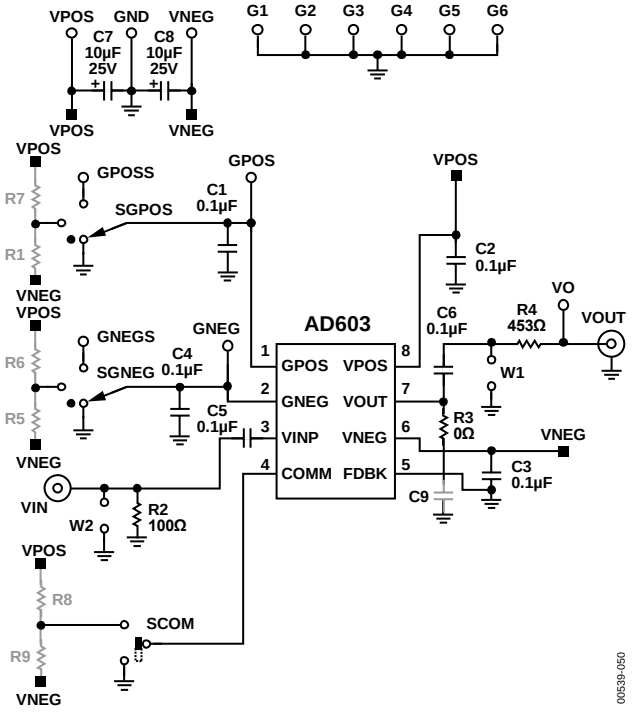


Figure 51. Schematic of the AD603 Evaluation Board

The output is also ac-coupled and includes a 453 Ω series resistor. Set the AD603 gain by connecting a voltage source between the GNEG and GPOS test loops. The two slide switches SGPOS and SGNEG provide three connections for GPOS and the GNEG. Either pin can be ground referenced, or biased with a user selected voltage established by R1 and R5 to R7. A signal generator can be connected to the GPOS or GNEG test loops, or the GNEG can be driven to either polarity within the common-mode limits of −1.2 V to +2.0 V; to invert the gain slope, simply reverse the polarity of the voltage source connected to GPOS and GNEG. For bias current measurements, the third switch option disconnects the bias voltage source and permits connection of a microammeter between the GPOS and GNEG pins to ground.

The AD603 includes built-in gain resistors selectable at the FDBK pin. The board is shipped with the gain at minimum, with a 0 Ω resistor installed in R3. For maximum gain, simply remove R3. Because of the architecture of the AD603, the bandwidth decreases by 10, but the gain range remains at 40 dB. Intermediate gain values may be selected by installing a resistor between the VOUT and FDBK pins.

Figure 52, Figure 53, and Figure 56 show the component and circuit side copper patterns and silkscreen.

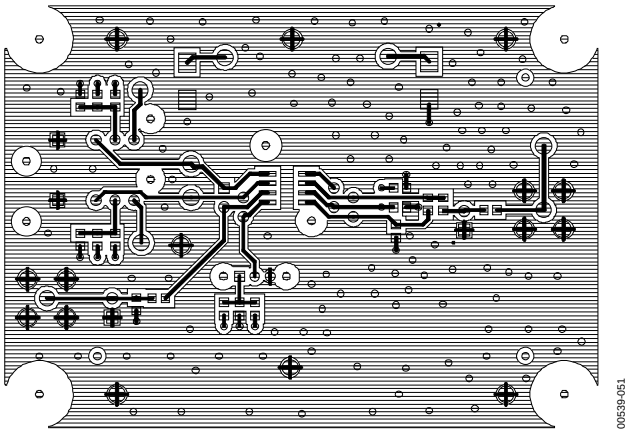


Figure 52. Component Side Copper

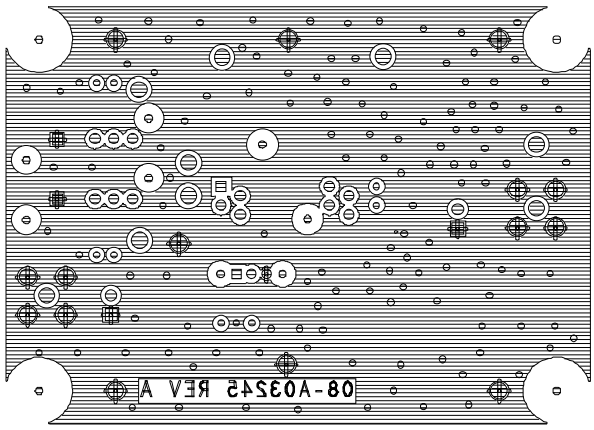


Figure 53. Secondary Side Copper

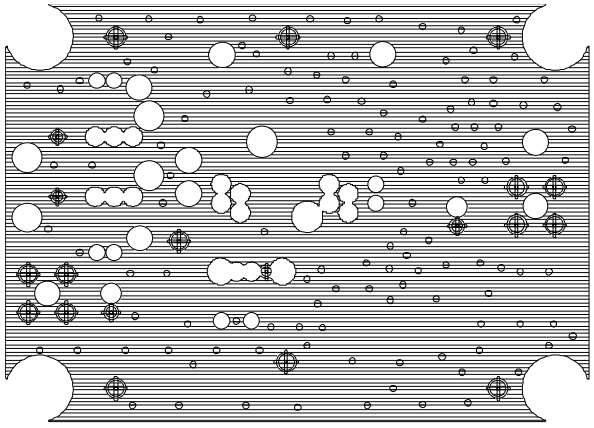


Figure 54. Inner Layer Ground Plane

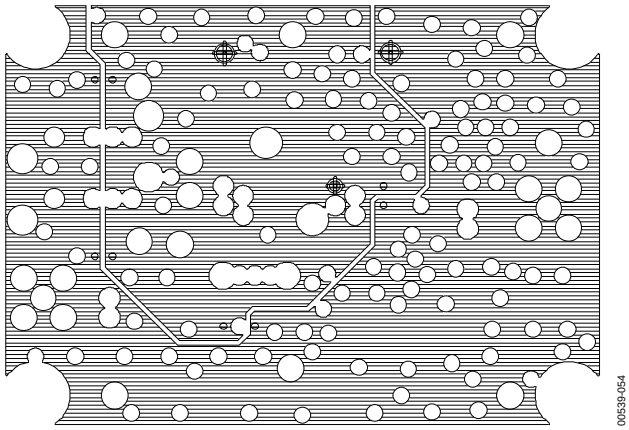


Figure 55. Inner Layer Power Plane

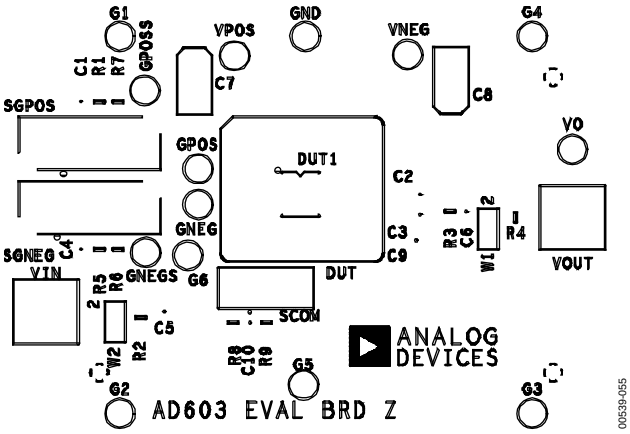
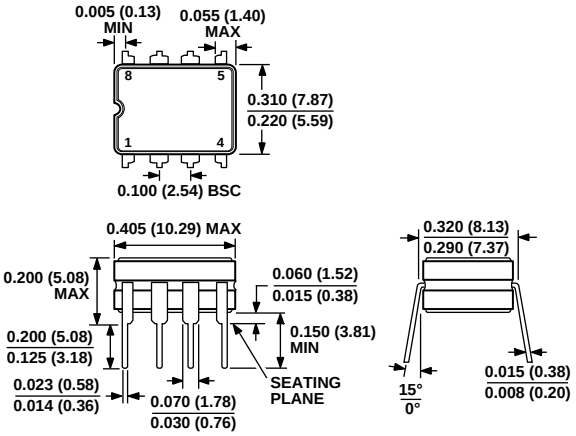


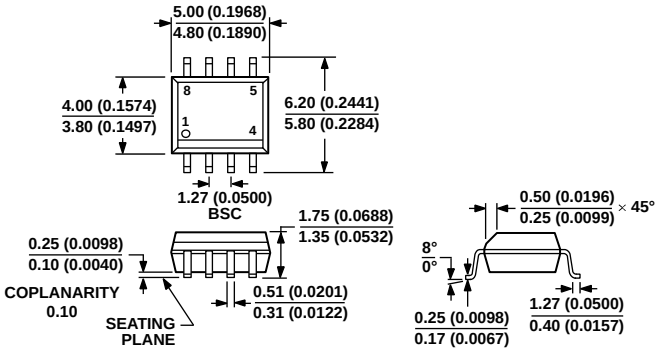
Figure 56. Component Side Silk Screen

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 57. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 58. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

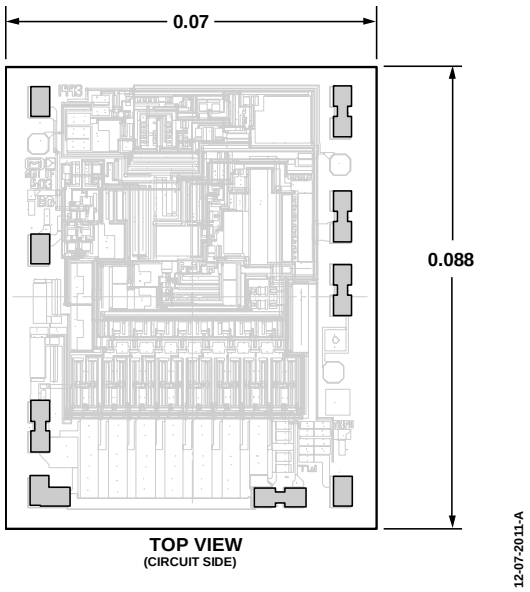


Figure 59. 9-Pad Bare Die [CHIP]
(C-9-1)
Dimensions Shown in Inches

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD603AR	−40°C to +85°C	8-Lead SOIC_N	R-8
AD603AR-REEL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD603AR-REEL7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD603ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD603ARZ-REEL	−40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD603ARZ-REEL7	−40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD603AQ	−40°C to +85°C	8-Lead CERDIP	Q-8
AD603SQ/883B	−55°C to +125°C	8-Lead CERDIP	Q-8
AD603-EVALZ		Evaluation Board	
AD603ACHIPS		DIE	C-9-1

[1] Z = RoHS Compliant Part.
[2] For AD603SQ/883B, refer to AD603 Military data sheet. Also available as 5962-9457203MPA.

NOTES

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