DATASHEET

ISL23710

Volatile Digitally Controlled Potentiometer (XDCP™) Terminal Voltage ±3V or ±5V, 128 Taps Up/Down Interface

FN6126
Rev 0.00
August 22, 2005

The Intersil ISL23710 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, and a control section. The wiper position is controlled by a Up/Down interface.

The potentiometer is implemented by a resistor array composed of 127 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The wiper register is volatile and is reset to midscale on power up. The wiper position can be locked while powered up to prevent inadvertent changes.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

- Industrial and Automotive Control
- Parameter and Bias Adjustments
- Amplifier Bias and Control

Ordering Information

PART NUMBER (BRAND)	RESISTANCE OPTION (Ω)	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL23710WIU10Z (AOG) (Notes 1, 2)	10K	-40 to +85	10 Ld MSOP (Pb-Free)	M10.118
ISL23710UIU10Z (AOF) (Notes 1, 2)	50K	-40 to +85	10 Ld MSOP (Pb-Free)	M10.118

NOTES:

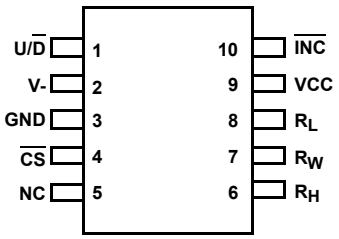
1. Add “-T” suffix for tape and reel.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

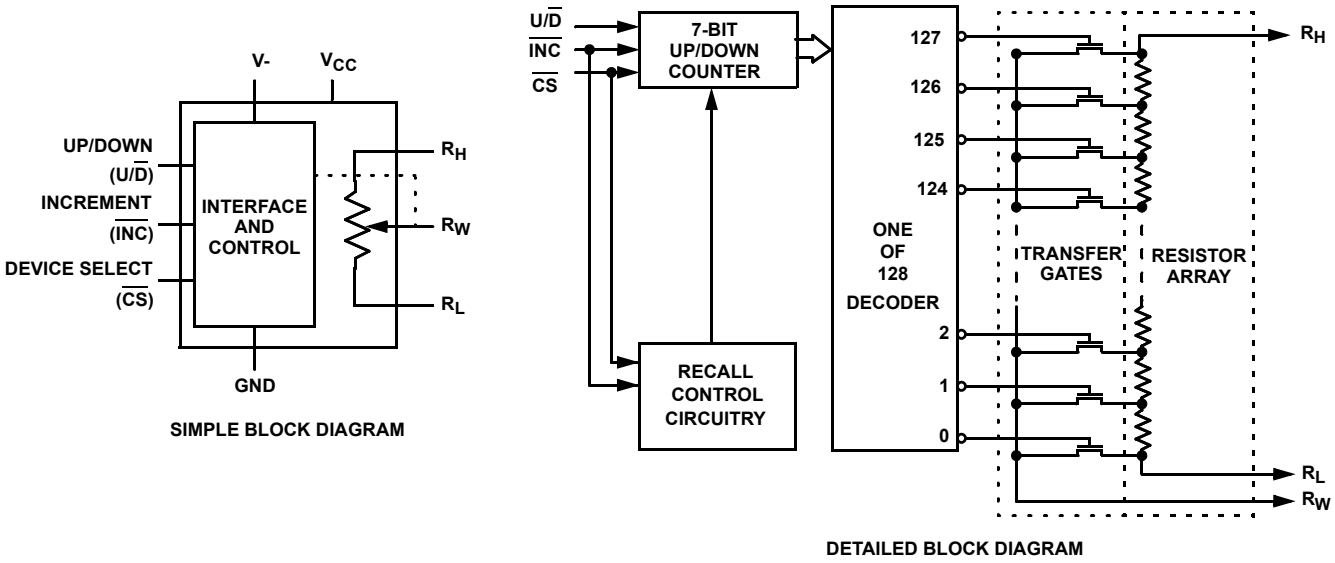
- Up/Down Interface with Chip Select Enable
- DCP Terminal Voltage from ±2.7V to ±5V
- 127 Resistive Elements
  - Typical R_{TOTAL} tempco ±50ppm/°C
  - Ratiometric tempco ±4ppm/°C
  - End to end resistance range ±20%
  - Wiper resistance = 70Ω typ at V_{CC} = 3.3V
- Low Power CMOS
  - V- = -2.7V to -5.5V
  - V_{CC} = 2.7V to 5.5V
  - Active current, 1mA max
  - Standby current, 500nA max
- R_{TOTAL} Values = 10kΩ, 50kΩ
- Volatile Wiper Storage with Wiper Locking
- Packages
  - 10 Ld MSOP
- Pb-Free Plus Anneal Available (RoHS Compliant)

Pinout

ISL23710
(10 LD MSOP)
TOP VIEW



Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	U/$\overline{D}$	Controls the direction of wiper movement and whether the counter is incremented or decremented.
2	V-	Negative supply voltage for the potentiometer wiper control.
3	GND	Ground. Should be connected to a digital ground.
4	$\overline{CS}$	Chip Select. The device is selected when the $\overline{CS}$ input is LOW.
5	NC	No Connect. Pin is to be left unconnected.
6	R_H	A fixed terminal for one end of the potentiometer resistor.
7	R_W	The wiper terminal which is equivalent to the movable terminal of a potentiometer.
8	R_L	A fixed terminal for one end of the potentiometer resistor.
9	VCC	Positive logic supply voltage.
10	$\overline{INC}$	Increment input; negative edge triggered.

Absolute Maximum Ratings

Temperature Under Bias . . . . . -65°C to +135°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC}
with Respect to GND . . . . . -0.3V to V_{CC}+0.3V
Voltage on V- (Referenced to GND) . . . . . -6V
$\Delta V = |V(RH)-V(RL)|$ 12V
Lead Temperature (Soldering 10s) . . . . . 300°C
I_W (10s) . . . . . ±6mA
V_{CC} . . . . . -0.3V to 6V
R_H, R_L, R_W . . . . . V- to V_{CC}
ESD Rating (MIL-STD-883, Method 3015.7) . . . . . >2kV

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
MSOP Package	170

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to +85°C
V_{CC} . . . . . 2.7V to 5.5V
V- . . . . . -2.7V to -5.5V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
R_{TOTAL}	R_H to R_L Resistance	W option		10		kΩ
		U option		50		kΩ
	R_H to R_L Resistance Tolerance		-20		+20	%
V_{RH},V_{RL}	R_H, R_l Terminal Voltage		V-		V_{CC}	V
R_W	Wiper Resistance	V- = -5.5V; V_{CC} = +5.5V, wiper current = (V_{CC} - V-)/R_{TOTAL}		70	200	Ω
C_H/C_L/C_W	Potentiometer Capacitance (Note 13)			10/10/25		pF
I_{LkgDCP}	Leakage on DCP Pins	Voltage at pin from V- to V_{CC}	-1	0.1	1	µA
VOLTAGE DIVIDER MODE (0V @ RL; V+ @ RH; measured at RW, unloaded)						
INL (Note 6)	Integral Non-linearity		-1		1	LSB (Note 2)
DNL (Note 5)	Differential Non-linearity	W, U options	-0.5		0.5	LSB (Note 2)
ZSerror (Note 3)	Zero-Scale Error	W option	0	1	4	LSB (Note 2)
		U option	0	0.5	2	
FSerror (Note 4)	Full-Scale Error	W option	-4	-1	0	LSB (Note 2)
		U option	-2	-0.5	0	
TC_V (Note 7,13)	Ratiometric Temperature Coefficient	DCP register set to i = 16 to 120d, T = -40°C to 85°C		±4		ppm/°C
RESISTOR MODE (Measurements between RW and RL with RH not connected, or between RW and RH with RL not connected)						
RINL (Note 11)	Integral Non-linearity	DCP register set between 16 and 127d Monotonic over all tap positions	-1		1	MI (Note 8)
RDNL (Note 10)	Differential Non-linearity		-0.5		0.5	MI (Note 8)
Roffset (Note 9)	Offset	DCP register set to 0d, W option	0	2	5	MI (Note 8)
		DCP register set to 0d, U option	0	0.5	2	MI (Note 8)
TC_R (Notes 12,13)	Resistance Temperature Coefficient	DCP register set to i = 16 to 127d, T = -40°C to +85°C		±50		ppm/°C

Operating Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
I_{CC1}	V_{CC} Supply Current, Volatile Write/Read	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and INC = 0.4V/2.4V min. t_{CYC} R_L, R_H, R_W not connected			500	µA
I_{V-}	V- Supply Current, Volatile Write/Read	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and INC = 0.4V/2.4V min. t_{CYC} R_L, R_H, R_W not connected	-100			µA
I_{SB}	V_{CC} Current (Standby)	V_{CC} = +5.5V, 3 Wire Interface in Standby State			500	nA
		V_{CC} = +2.7V, 3 Wire Interface in Standby State			300	nA
I_{V-SB}	V- Current (Standby)	V- = -5.5V, 3 Wire Interface in Standby State	-500			nA
		V- = -2.7V, 3 Wire Interface in Standby State	-300			nA
I_{LkgDig}	Leakage Current, at Pins $\overline{INC}$, $\overline{CS}$, U/$\overline{D}$, A0, and A1	Voltage at pin from GND to V_{CC}	-10		10	µA
Vpor	Power-on Recall Voltage	Minimum V_{CC} at which the wiper is Reset		2.5		V
SERIAL INTERFACE SPECS						
V_{IL}	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$ Input Buffer LOW Voltage		-0.3		0.3*V_{CC}	V
V_{IH}	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$ Input Buffer HIGH Voltage		0.7*V_{CC}		V_{CC}+0.3	V
Hysteresis (Note 13)	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$ Input Buffer Hysteresis			0.15* V_{CC}		V
Cpin (Note 13)	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$ Pin Capacitance			10		pF

AC Electrical Specifications

V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range unless otherwise stated

SYMBOL	PARAMETER	MIN	TYP (Note 1)	MAX	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ Change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	1			µs
t_{IL}	$\overline{INC}$ LOW Period	1			µs
t_{IH}	$\overline{INC}$ HIGH Period	1			µs
t_{ICL}	Lock Setup Time, $\overline{INC}$ High to $\overline{CS}$ High	1			µs
t_{IW} (Note 13)	$\overline{INC}$ to R_W Change		1		µs
t_{CYC}	$\overline{INC}$ Cycle Time	2			µs
t_R, t_F	$\overline{INC}$ Input Rise and Fall Time			500	µs

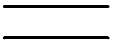
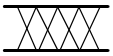
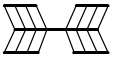
NOTES:

1. Typical values are for T_A = 25°C and 3.3V supply voltage.
2. LSB: $[V(RW)_{127} – V(RW)_0]/127$. $V(RW)_{127}$ and $V(RW)_0$ are V(RW) for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
3. ZS error = $V(RW)_0$/LSB.
4. FS error = $[V(RW)_{127} – V_{CC}]$/LSB.
5. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 127. i is the DCP register setting.
6. INL = $V(RW)_i – (i • LSB – V(RW)_0)$ for i = 1 to 127.
7. $$TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} x \frac{10^6}{125°C}$$

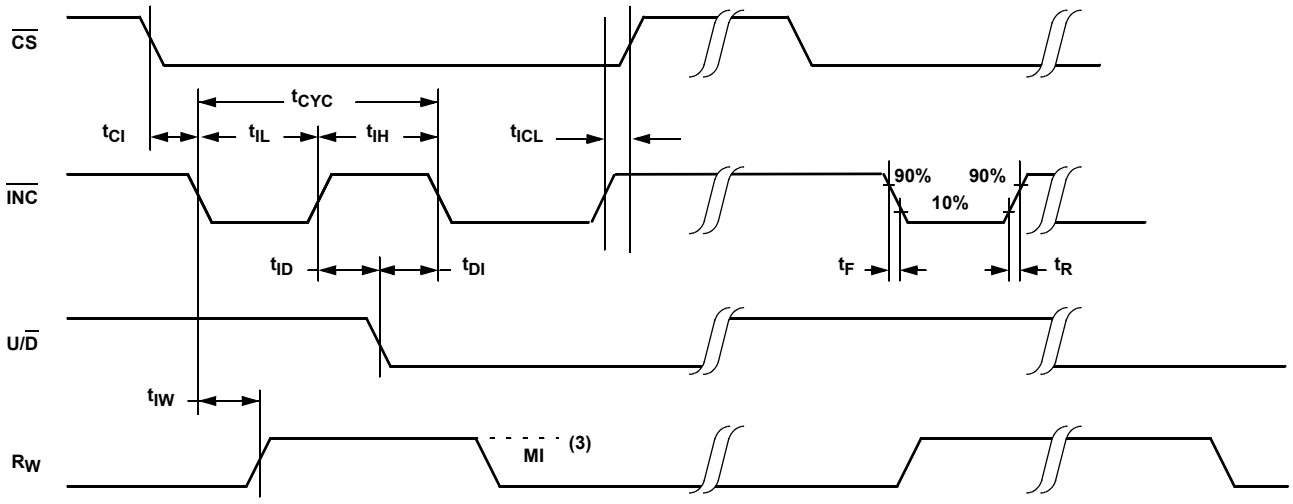
   Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
8. MI = $|R_{127} – R_0|$ /127. R_{127} and R_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
9. Roffset = R_0/MI, when measuring between RW and RL.
   Roffset = R_{127}/MI, when measuring between RW and RH.
10. RDNL = $(R_i – R_{i-1})$/MI, for i = 16 to 127d.
11. RINL = $[R_i – (MI • i) – R_0]$/MI, for i = 16 to 127d.
12. $$TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$$

    Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
13. This parameter is not 100% tested.

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don’t Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

AC Timing



Power Up and Down Requirements

In order to prevent unwanted tap position changes, bring the $\overline{CS}$ and $\overline{INC}$ high before or concurrently with the V_{CC} pin on power-up. The potentiometer voltages must be applied after this sequence is completed. During power-up, the data sheet parameters for the DCP do not fully apply until 1ms after V_{CC} reaches its final value. The wiper will be set to its initial value (64d) once V_{CC} exceeds V_{POR}.

Pin Descriptions

R_H and R_L

The high (R_H) and low (R_L) terminals of the ISL23710 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of R_L and R_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

R_W

R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incriminated or decremented.

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW.

Principles of Operation

There are three sections of the ISL23710: the input control, counter and decode section, and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. The resistor array is comprised of 127 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a seven bit counter. The output of this counter is decoded to select one of one-hundred twenty-eight wiper positions along the resistive array.

Bringing $\overline{CS}$ HIGH after $\overline{INC}$ is HIGH will cause the wiper value to be locked until power down (further changes in $\overline{CS}$ and INC will not change the wiper position). Otherwise, $\overline{INC}$ should be brought HIGH after $\overline{CS}$ to allow continued wiper changes.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained. During initial power-up $\overline{CS}$ must go high along with or before V_{CC} to avoid an accidental tap position change.

TABLE 1. MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↓	H	Wiper Up
L	↓	L	Wiper Down
↑	H	X	Lock Wiper Value
H	↑	X	Standby
↑	L	X	Standby
H	H	X	Standby
↓	L	H	Wiper up One Position (not recommended)
↓	L	L	Wiper Down One Position (not recommended)

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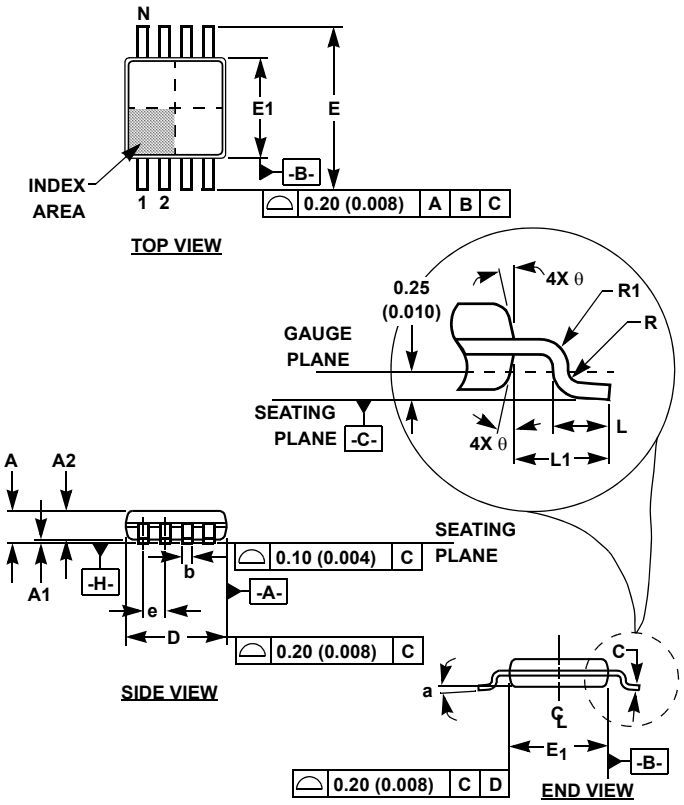
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Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 0 12/02

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only