



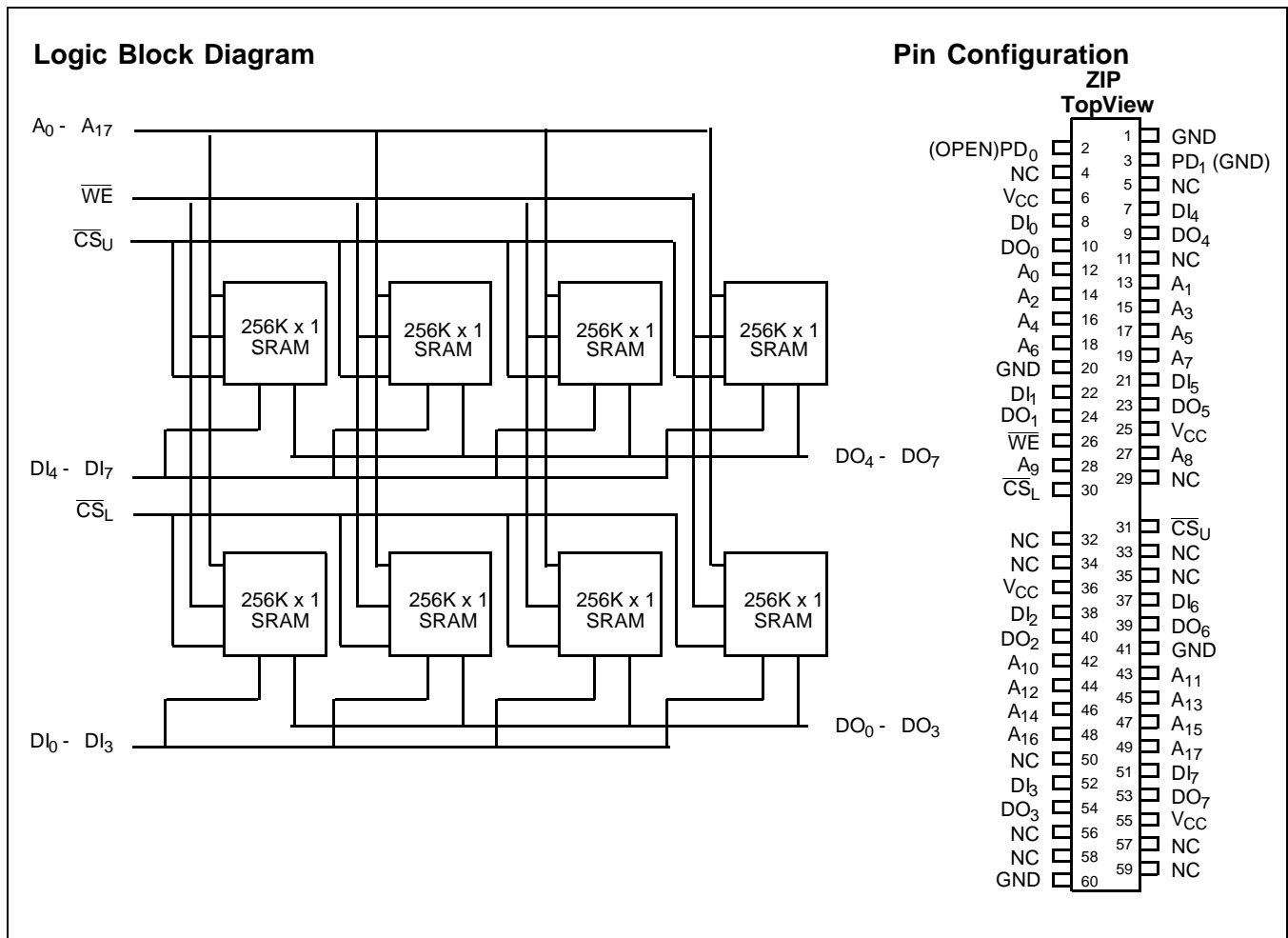
# 256K x 8 Static RAM Module

## Features

- High-density 2-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 20 ns
- Low active power
  - 5.3W (max.)
- SMD technology
- Separate data I/O
- 60-pin ZIP package
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of 0.5 in.
- Small PCB footprint
  - 1.14 sq. in.

## Functional Description

The CYM1441 is a very high performance 2-megabit static RAM module organized as 256K words by 8 bits. The module is constructed using eight 256K x 1 static RAMs in SOJ packages mounted onto an epoxy laminate substrate with pins. Two chip selects ( $\overline{CS}_L$  and  $\overline{CS}_U$ ) are used to independently enable the upper and lower 4 bits of the data word. Writing to the memory module is accomplished when the chip select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the eight input pins ( $DI_0$  through  $DI_7$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{17}$ ). Reading the device is accomplished by taking chip select ( $\overline{CS}$ ) LOW while write enable ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data output pins ( $DO_0$  through  $DO_7$ ). The data output pins remain in a high-impedance state unless the module is selected and write enable ( $\overline{WE}$ ) is HIGH. Two pins ( $PD_0$  and  $PD_1$ ) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.



**Selection Guide**

	1441-20	1441-25	1441-35	1441-45
Maximum Access Time (ns)	20	25	35	45
Maximum Operating Current (mA)	960	960	960	960
Maximum Standby Current (mA)	320	320	320	320

Shaded area contains preliminary information.

**Maximum Ratings**

(Above which the useful life may be impaired.)

Storage Temperature ..... -55°C to +125°C

Ambient Temperature with  
Power Applied..... -10°C to +85°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State..... -0.5V to +7.0V

DC Input Voltage ..... -0.5V to +7.0V

**Operating Range**

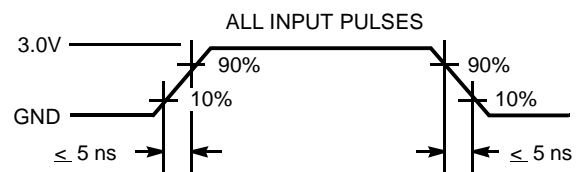
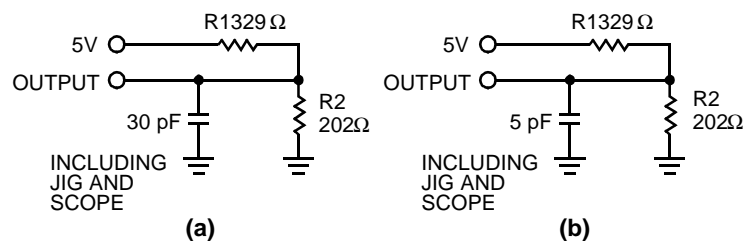
Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

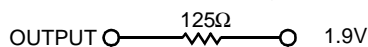
Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 12.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-80	+80	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-50	+50	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, $\overline{CS} \leq V_{IL}$		960	mA
I <sub>SB1</sub>	Automatic $\overline{CS}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CS} \geq V_{IH}$ , Min. Duty Cycle = 100%		320	mA
I <sub>SB2</sub>	Automatic $\overline{CS}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CS} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V		160	mA

**Capacitance<sup>[2]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	60	pF
C <sub>OUT</sub>	Output Capacitance		15	pF

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT

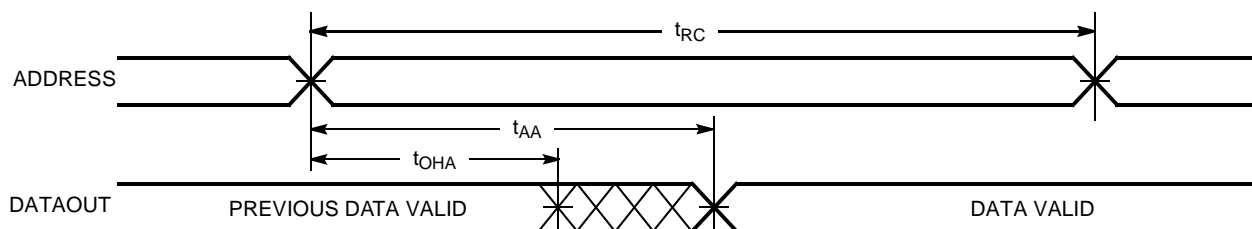

**Notes:**

- V<sub>IN</sub> (min.) = -3.0V for pulse widths less than 20 ns.
- Tested on a sample basis.

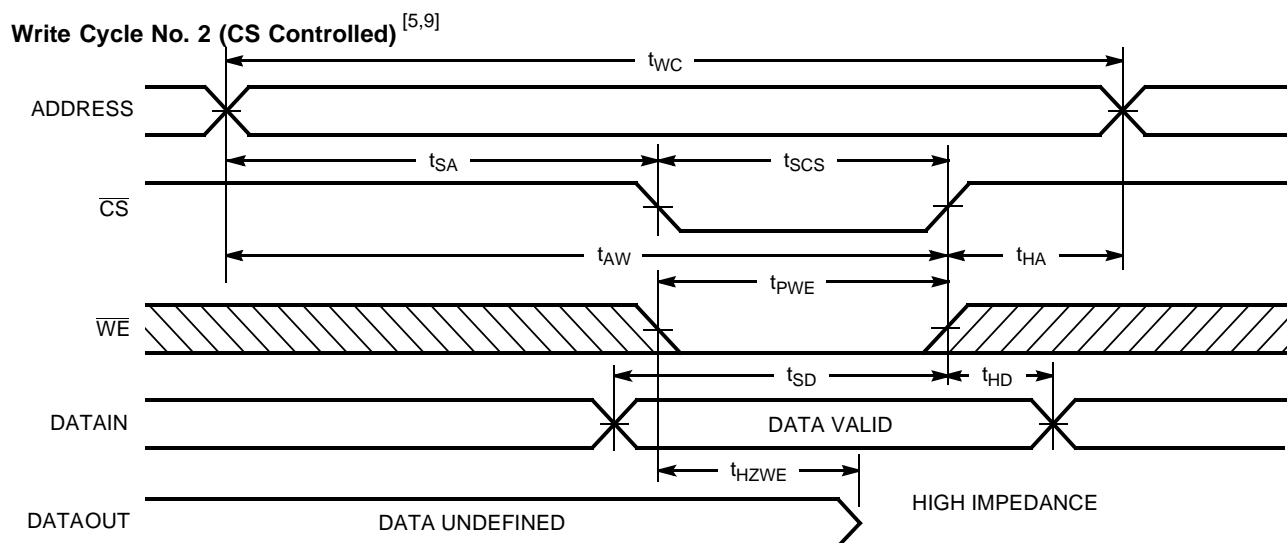
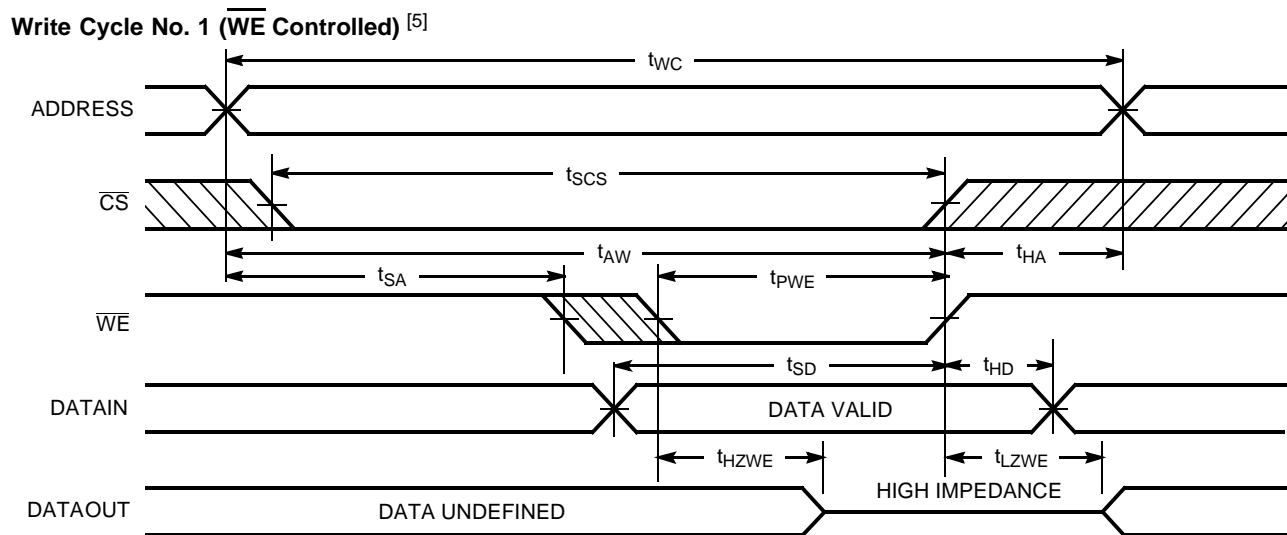
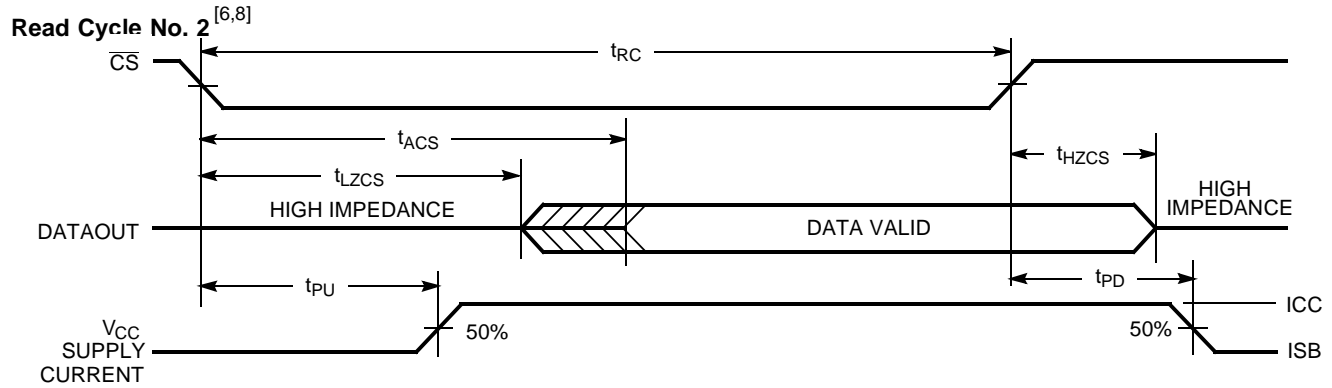
**Switching Characteristics** Over the Operating Range<sup>[3]</sup>

Parameter	Description	1441-20		1441-25		1441-35		1441-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
$t_{RC}$	Read Cycle Time	20		25		35		45		ns
$t_{AA}$	Address to Data Valid		20		25		35		45	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		3		ns
$t_{ACS}$	CS LOW to Data Valid		20		25		35		45	ns
$t_{LZCS}$	CS LOW to Low Z	3		3		3		3		ns
$t_{HZCS}$	CS HIGH to High Z <sup>[4]</sup>		12		15		25		30	ns
$t_{PU}$	CS LOW to Power-Up	0		0		0		0		ns
$t_{PD}$	CS HIGH to Power-Down		20		25		35		45	ns
<b>WRITE CYCLE<sup>[5]</sup></b>										
$t_{WC}$	Write Cycle Time	20		25		35		45		ns
$t_{SCS}$	CS LOW to Write End	15		20		30		35		ns
$t_{AW}$	Address Set-Up to Write End	15		20		30		35		ns
$t_{HA}$	Address Hold from Write End	2		2		2		2		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		2		ns
$t_{PWE}$	WE Pulse Width	15		20		25		30		ns
$t_{SD}$	Data Set-Up to Write End	13		15		20		20		ns
$t_{HD}$	Data Hold from Write End	0		0		0		0		ns
$t_{LZWE}$	WE HIGH to Low Z	3		3		3		3		ns
$t_{HZWE}$	WE LOW to High Z <sup>[4]</sup>	0	13	0	15	0	20	0	25	ns

Shaded area contains preliminary information.

**Switching Waveforms**
**Read Cycle No. 1** <sup>[6,7]</sup>

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZCS}$  and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads and Waveforms. Transition is measured  $\pm 500$  mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- WE is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$ .

**Switching Waveforms (continued)**

**Notes:**

8. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
9. If CS goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

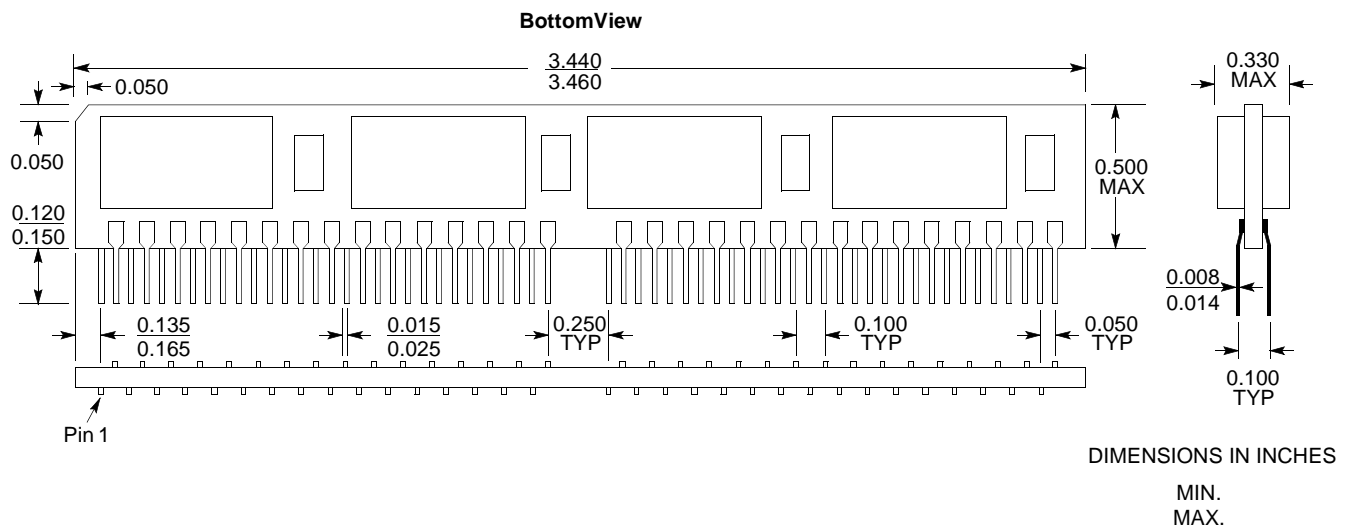
**Truth Table**

CS	WE	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

**Ordering Information**

Speed	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1441PZ-20C	PZ04	60-Pin ZIP Module	Commercial
25	CYM1441PZ-25C	PZ04	60-Pin ZIP Module	Commercial
35	CYM1441PZ-35C	PZ04	60-Pin ZIP Module	Commercial
45	CYM1441PZ-45C	PZ04	60-Pin ZIP Module	Commercial

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**Package Diagrams**
**60-Pin ZIP Module PZ04**


<b>Document Title: CYM1441 256K x 8 Static RAM Module</b> <b>Document Number: 38-05271</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	114172	3/19/02	DSG	Change from Spec number: 38-M-00020 to 38-05271