8 N-Channel Latchable Power MOSFET Array

Ordering Information

V_{DD} (max)	$R_{O(ON)}$ (max)	$I_{O(ON)}$ (min)	$I_{O(OFF)}$ (max)	Order Number/Package	
				SO-16	Die
320V	350Ω	25mA	-1.0nA	AN0332CG	AN0332ND

*Average current per channel, measured with all eight channels connected in parallel.

Features

- ☐ Low drain to source leakage
- ☐ Interfaces directly to TTL and CMOS logic
- ☐ 8 independent channels
- ☐ Low crosstalk between channels
- ☐ Low power dissipation
- ☐ Freedom from secondary breakdown
- ☐ Serial data input
- ☐ On-chip decoder, latch with reset and write disable circuitry

General Description

The Supertex AN0332 is an 8 N-Channel 320V common source power MOSFET array with a CMOS 8 bit addressable latch. The outputs are guaranteed to have very low leakage current. The outputs are addressed by logic inputs A0, A1, and A2. The addressed and unaddressed output can be turned on or off by the data, reset, and write disable inputs.

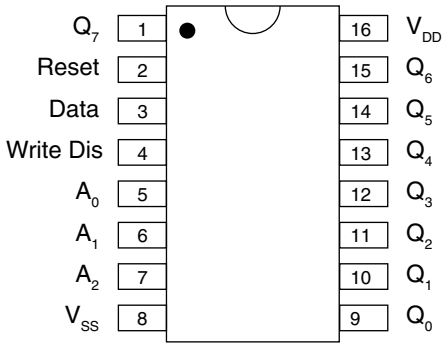
The AN0332 is ideally suited for low leakage/high impedance measurements, providing excellent accuracy as well as resolution for automatic bare board test equipment and other applications.

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Applications

- ☐ High impedance/low leakage measurements for bare board testers
- ☐ High voltage piezoelectric transducer drivers
- ☐ High voltage electroluminescent panel drivers
- ☐ High voltage electrostatic array drivers
- ☐ General multi-channel driver arrays

Pin Configuration



top view
SO-16

Note: See Package Outline section for dimensions.

Absolute Maximum Ratings[1]

Output voltage, V_{DD}	320V
Logic supply voltage, V_{DD}	-0.5V to +15V
Logic input levels, all inputs	-0.5V to V_{DD}
Operating and storage temperature range	-55°C to +150°C
Soldering temperature[2]	300°C
Channel-to-channel crosstalk	10mV/V

Notes:
1. All voltages are referenced to V_{SS}.
2. Distance of 1.6mm from case for 10 seconds.

Electrical Characteristics (@ 25°C and V_{DD} = 12V unless otherwise specified)

DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$I_{O(OFF)}$	Off-State Output Current			8.0	nA	V_O = max. rating, 8 outputs connected in parallel
$I_{O(ON)}$	On-State Output Current	25			mA	V_O = 25V
$R_{O(ON)}$	On-State Output Resistance			350	Ω	I_O = 10mA
$\Delta R_{O(ON)}$	Change in $R_{O(ON)}$ with High Temperature		0.8		%/°C	I_O = 10mA
I_{DDQ}	Quiescent Logic Supply Current		0.05	16.5	μA	
V_{IL}	Input Low Voltage			3.5	V	
V_{IH}	Input High Voltage	12			V	
I_{IN}	Input Current			1.0	μA	

Note:
1. All voltages are referenced to V_{SS}.

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AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Fig. 1*	Conditions
$t_{D(ON)}$	Turn-On Delay Time		800		ns	1a	
$t_{D(OFF)}$	Turn-Off Delay Time		800		ns	1b	
t_r	Rise Time		200		ns	10	
t_f	Fall Time		200		ns	11	
t_{PHL}, t_{PLH}	Propagation Delay Time from Write Disable to Output		87		ns	2	V_O = 25V, I_O = 10mA
t_{PHL}, t_{PLH}	Propagation Delay Time from Reset to Output		87		ns	3	
t_{PHL}, t_{PLH}	Propagation Delay Time from Address to Output		107		ns	9	
t_W	Minimum Pulse Width – Data		50	100	ns	4	
t_W	Minimum Pulse Width – Address		100	200	ns	8	
t_W	Minimum Pulse Width – Reset		40	75	ns	5	
t_S	Setup Time – Data to Write Disable	50			ns	6	
t_H	Hold Time – Data to Write Disable`	75			ns	7	
C_{IN}	Input capacitance – Any Input		5.0	7.5	pF		

*Refer to circled numbers on Timing Diagram (Figure 1).

Note:
1. All voltages are referenced to V_{SS}.

Recommended Operating Conditions

(For maximum reliability, nominal operating conditons should be selected so that operation is always within the following ranges.)

Symbol	Parameter	V_{DD}	Min	Max	Unit
V_{DD}	Logic supply voltage		10.0	13.2	V
V_O	Output Voltage referenced to V_{SS}		0	320	V
V_{IH}	Input High Voltage	12V	V_{DD} - 2	V_{DD}	V
V_{IL}	Input Low Voltage	12V	0	2.0	V
T_A	Operating Free-Air Temperature		0	70	°C

Note:
1. All voltages are referenced to V_{ss}.

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Mode Selection

Data	Write Disable	Reset	Addressed Output	Unaddressed Outputs
H L	L	L	On Off	Holdspriv.
H L	H	L	Holdspriv.	Holdspriv.
H L	L	H	On Off	Off
H L	H	H	Off	Off

Timing Diagram

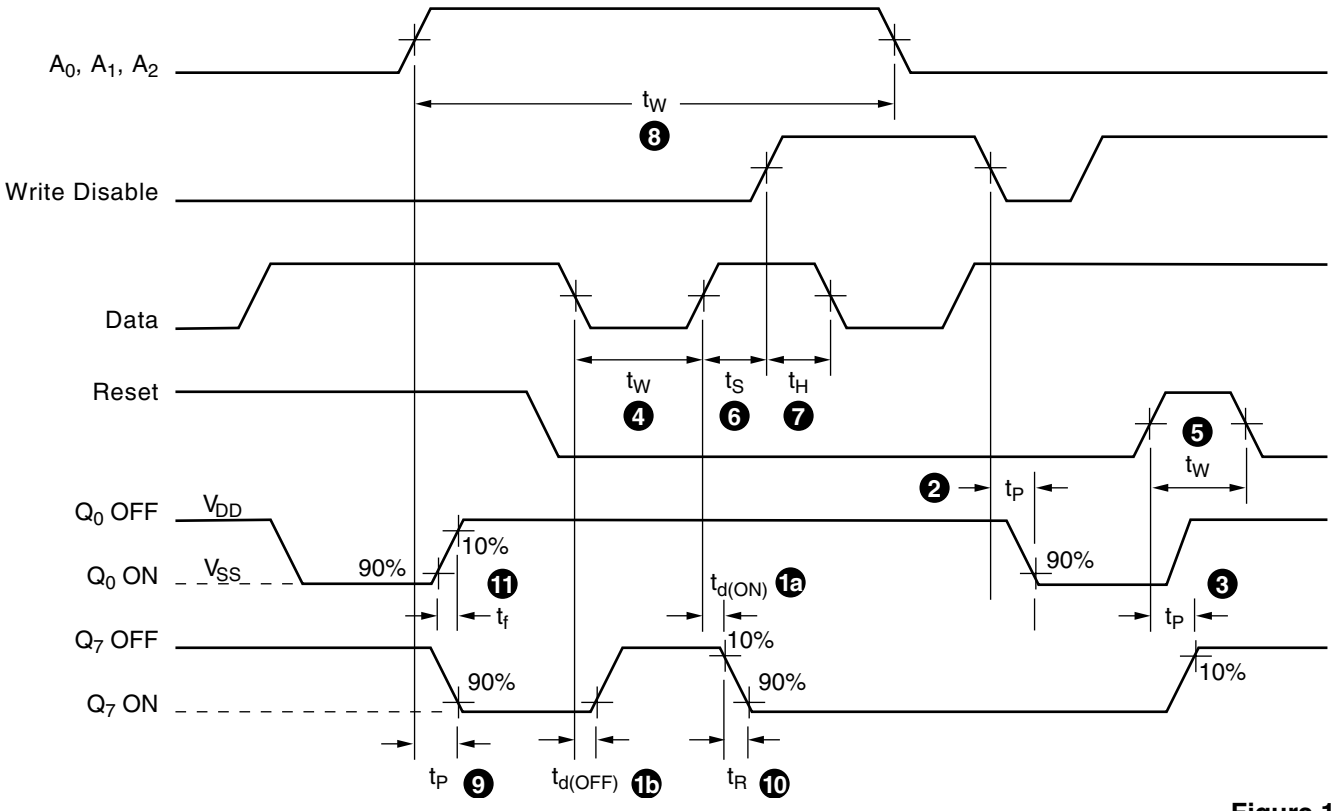


Figure 1

Functional Block Diagram

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