

isc Silicon NPN Power Transistor

KSH340

DESCRIPTION

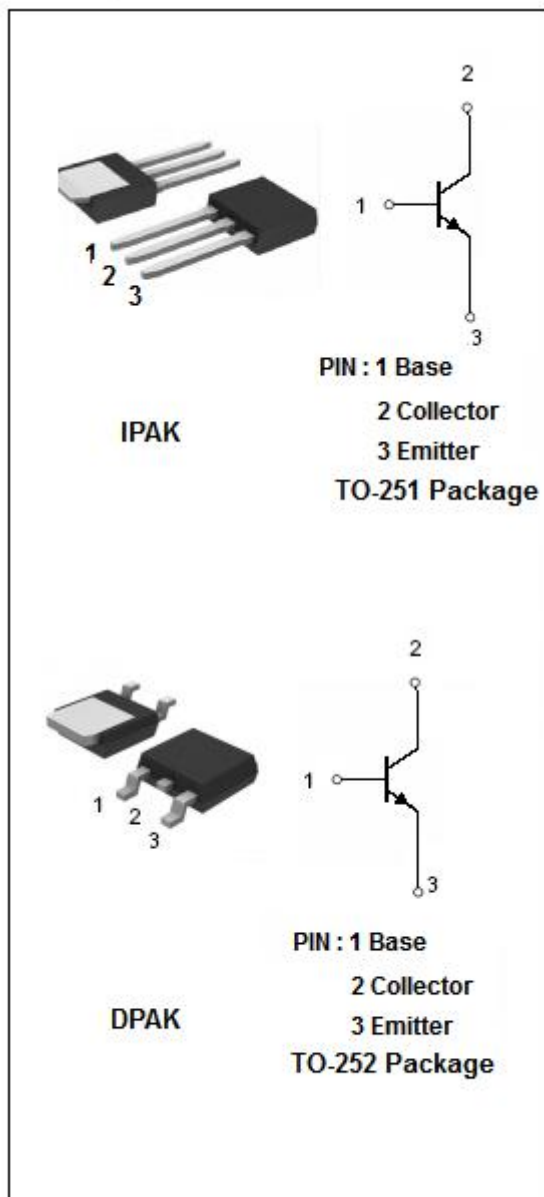
- Lead formed for surface mount applications(NO suffix)
- Straight lead(IPAK, “-I” suffix)
- DPAK for surface mount applications
- 100% avalanche tested
- Minimum Lot-to-Lot variations for robust device performance and reliable operation

APPLICATIONS

- High voltage power transistors

ABSOLUTE MAXIMUM RATINGS($T_a=25^{\circ}\text{C}$)

SYMBOL	PARAMETER	VALUE	UNIT
V_{CBO}	Collector-Base Voltage	300	V
V_{CEO}	Collector-Emitter Voltage	300	V
V_{EBO}	Emitter-Base Voltage	3	V
I_C	Collector Current-Continuous	0.5	A
P_C	Total Power Dissipation @ $T_a=25^{\circ}\text{C}$	1.56	W
P_C	Total Power Dissipation @ $T_c=25^{\circ}\text{C}$	15	W
T_J	Junction Temperature	150	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range	-55~150	$^{\circ}\text{C}$



isc Silicon NPN Power Transistor**KSH340****ELECTRICAL CHARACTERISTICS** $T_c=25^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}^*$	Collector-Emitter Breakdown Voltage	$I_C = 1\text{mA}; I_B = 0$	300			V
I_{CBO}	Collector Cutoff Current	$V_{CB} = 300\text{V}; I_E = 0$			100	μA
I_{EBO}	Emitter Cutoff Current	$V_{EB} = 3\text{V}; I_C = 0$			100	μA
h_{FE1}^*	DC Current Gain	$I_C = 50\text{mA}; V_{CE} = 10\text{V}$	30		240	

*:Pulse test $PW \leq 300\mu\text{s}$, duty cycle $\leq 2\%$

isc Silicon NPN Power Transistor**KSH340****Outline Drawing**